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This is the accepted version of a paper published in *IEEE Transactions on Electron Devices*. This paper has been peer-reviewed but does not include the final publisher proof-corrections or journal pagination.

Citation for the original published paper (version of record):

Lanni, L., Ghandi, R., Malm, B G., Zetterling, C-M. (2012)
Design and Characterization of High-Temperature ECL-Based Bipolar Integrated Circuits in 4H-SiC.
IEEE Transactions on Electron Devices, 59(4): 1076-1083
<http://dx.doi.org/10.1109/TED.2011.2182514>

Access to the published version may require subscription.

N.B. When citing this work, cite the original published paper.

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Design and Characterization of High-Temperature ECL-Based Bipolar Integrated Circuits in 4H-SiC

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Abstract—Operation up to 300 °C of low-voltage 4H-SiC n-p-n bipolar transistors and digital integrated circuits based on emitter-coupled logic is demonstrated. Stable noise margins of about 1 V are reported for a two-input OR–NOR gate operated on –15 V supply voltage from 27 °C up to 300 °C. In the same temperature range, an oscillation frequency of about 2 MHz is also reported for a three-stage ring oscillator.

Index Terms—Bipolar junction transistor (BJT), emitter coupled logic (ECL), high-temperature integrated circuits (ICs), OR–NOR gate, silicon carbide (SiC).

I. INTRODUCTION

SILICON CARBIDE (SiC) is a wide band-gap semiconductor that provides significant advantages for high-power and high-temperature applications because of its high critical field strength and thermal conductivity [1]. In particular, SiC devices are suitable for high-temperature integrated circuits (ICs) due to their capability to work at high temperature and relaxed cooling requirements.

High-temperature operation of ICs has been already reported in SiC with different devices and logics. Long-term stability of JFET ICs, both analog and digital, has been demonstrated in 6H-SiC with circuit operation at 500 °C for thousand hours [2]. CMOS technology has been investigated since early 1990s in 6H-SiC [3] and has been recently reported in 4H-SiC [4]. In both cases, 300 °C operation of digital circuits has been shown. Bipolar ICs have been also demonstrated in 4H-SiC with operation of up to 355 °C of transistor–transistor logic (TTL) and propagation delays comparable with those of silicon TTL circuits (~ 10 ns) [5].

In this paper, we report a bipolar IC technology in 4H-SiC based on emitter-coupled logic (ECL) with transistor current gain of about 45 at room temperature, which is capable of operation at 300 °C. The ECL permits a wide operating range both in terms of temperature and supply voltage since it is based on differential stages and allows an easy implementation of a temperature and supply voltage compensation network. The goal of this first paper is to demonstrate high-temperature

Fig. 1. Fabricated n-p-n transistor. (a) Cross-sectional view. (b) Optical image.

operation of bipolar ECL ICs. A two-input OR–NOR gate and a three-stage ring oscillator (RO) with 300 °C operation are reported.

This paper is organized in three main sections. The first deals with the design of the circuits focusing on bipolar junction transistor (BJT) modeling and integrated resistor sizing; the second briefly describes the fabrication process, whereas the third discusses simulation and measurement results for isolated BJTs and circuits, both OR–NOR gate and RO.

II. CIRCUIT SIMULATION AND DESIGN

In order to design and simulate the OR–NOR gate at different temperatures, SwitcherCAD III/LTspice [6] and appropriate SPICE models for the n-p-n transistor have been used. SPICE model parameters have been extracted at 27 °C and 200 °C from measurements performed on single-finger transistors realized in a high-voltage technology [7] since those designed for this paper have been fabricated for the first time together with the circuits. The cross-sectional view and an optical image of the n-p-n transistors fabricated in this paper are shown in Fig. 1(a) and (b), respectively. All transistor terminals are accessible on the top side, and the p-isolation layer provides isolation between different devices. The transistors have been designed to similarly behave to the single-finger high-voltage BJTs when operated in the low-voltage range. Preliminary 2-D device

Manuscript received November 1, 2011; revised December 22, 2011; accepted December 27, 2011. Date of publication February 10, 2012; date of current version March 23, 2012. The review of this paper was arranged by Editor J. D. Cressler.

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Fig. 2. Circuit diagram of the ECL OR-NOR gate.

simulations performed by using Sentaurus TCAD [8] predicted forward current gains β similar to those measured on the single-finger BJTs. At 27 °C, 100 °C, and 200 °C and $V_{BC} = 0$ V, simulated current gains are equal to 39, 31, and 25, whereas the measured ones are equal to 40, 28, and 21. At 27 °C and 200 °C, SPICE model parameters are the results of a graphical extraction procedure and a successive optimization routine, which provides good agreement between measurements and LTspice simulations of the transistor characteristics (i.e., forward and reverse Gummel plot and output characteristic).

The OR-NOR gate, whose circuit diagram is shown in Fig. 2, has been designed in order to obtain noise margins (NMs) stable with temperature based on well-known solutions available in literature [9]. The negative supply voltage has been increased from -5.2 V, used in silicon ECL, up to -15 V to account for a three times larger voltage drop across a forward-biased p-n junction in SiC compared with that in Si. Resistance values have been designed in order to obtain adequate NMs for both OR and NOR outputs by the means of LTspice simulations. Resistor geometrical dimensions have been derived from measured sheet resistance and specific contact resistance of emitter and base layer of the already mentioned high-voltage technology. The transfer length method (TLM) has been used at different temperatures between 27 °C and 200 °C. Although layer doping concentrations and thicknesses are not the same in the high voltage and in the IC technology, the logic gate was expected to properly work according to LTspice simulations.

The three-stage RO consists of four OR-NOR gates. One is used as the output buffer, and three are connected in chain with the NOR output of one gate connected to one input of the successive gate; the output of the last gate is fed back to the input of the first one. Except for the first stage, all the others act as inverters having one input and one output open. Input A in the first gate acts as the control input. A high logic level applied to it settles a stable logic level at the output of each stage.

III. FABRICATION

All test devices and circuits are fabricated on a six-layer epistructure ($n^{++}/n^{+}/p/n^{-}/n^{+}/p$) grown in a continuous run.

Fig. 3. Optical image of the fabricated two-input ECL OR-NOR gate.

The emitter layer consists of $0.8\text{-}\mu\text{m}$ nitrogen doped to $1 \times 10^{19} \text{ cm}^{-3}$ capped by a $0.2\text{-}\mu\text{m}$ -thick $3 \times 10^{19} \text{ cm}^{-3}$ layer. The base is a 300-nm Al layer doped to $1.4 \times 10^{18} \text{ cm}^{-3}$. The n^{-} collector is $1\text{-}\mu\text{m}$ nitrogen doped to $1 \times 10^{16} \text{ cm}^{-3}$ followed by a $1\text{-}\mu\text{m}$ -thick n^{+} layer (nitrogen doped to $1 \times 10^{19} \text{ cm}^{-3}$) in order to provide high doping for top side ohmic contact to the collector. A further $2\text{-}\mu\text{m}$ -thick p-layer ($1.4 \times 10^{18} \text{ cm}^{-3}$) is used to isolate different devices.

Plasma etching in HBr and Cl_2 with a photoresist mask was used to form emitter, base, and collector mesas. After sacrificial oxidation in N_2O ambient, surface passivation was performed with 50-nm PECVD SiO_2 followed by postoxide anneal in N_2O at 1150 °C for 3 h [10] in order to minimize surface recombination. E-beam evaporation was used to deposit Ni for emitter and collector contacts, and a triple layer of Ni/Ti/Al for base- and isolation-layer contacts. After each metal deposition, a liftoff process was used to pattern the contacts, and an anneal step was performed in order to provide low resistive ohmic contact to the epitaxial layer [7], [10]. A $2\text{-}\mu\text{m}$ -thick PECVD SiO_2 layer was deposited as intermediate dielectric, and a $3\text{-}\mu\text{m}$ -thick Al layer was then sputtered and patterned to realize all the interconnects.

The fabricated OR-NOR gate, whose optical image is shown in Fig. 3, consists of 10 n-p-n transistors (two of them are connected as diodes) and 11 integrated resistors, with a total area of 1.117 mm^2 ($1000 \mu\text{m} \times 1117 \mu\text{m}$). The isolated n-p-n [see Fig. 1(b)] is $162.5 \mu\text{m} \times 105 \mu\text{m}$ with an emitter area of $30 \mu\text{m} \times 90 \mu\text{m}$. All the integrated resistors have been realized in the emitter epilayer except for the input pulldowns (see R_{i1} and R_{i2} in Fig. 2), which have been fabricated in the base epilayer. Different resistor topologies (strip or serpentine) and different widths (8, 26, and $44 \mu\text{m}$) have been used. Concerning the topology, the serpentine has been preferred for high resistance values to get more compact integrated resistors, whereas the medium width has been used to reduce the contribution of the contact resistance to the overall resistance when needed. This way, all resistors, independent of their resistance value, are expected to show similar resistance temperature dependence

Fig. 4. Optical image of fabricated three-stage RO based on the OR-NOR gate.

although contact and sheet resistances show different temperature dependence values. Only for the pull-down resistors that the width has been set to $44 \mu\text{m}$.

The fabricated RO, whose optical image is shown in Fig. 4, contains 40 transistors and 48 integrated resistors with a total area of 4.751 mm^2 ($3700 \mu\text{m} \times 1284 \mu\text{m}$). In order to realize all the needed interconnects with only one metal layer, four integrated resistors, realized in the collector layer, have been inserted in series with the signal path and crossed by a metal line.

The chip contains several test structures, including isolated n-p-n transistors and transfer length measurement structures realized in emitter, base, and high-doped collector layer.

IV. RESULTS AND DISCUSSION

In the reported IC technology, sheet resistance and specific contact resistance have been extracted by using TLM structures in emitter, base, and high-doped collector in eight different dies. The average emitter and collector sheet resistances are 110 and $170 \Omega/\text{sq}$, respectively at 27°C , and they are consistent with layer doping and thickness. The average base sheet resistance, measured as $55 \text{ k}\Omega/\text{sq}$, is higher than what was expected. In all the three layers, a certain variation has been observed in the measured sheet resistance. It varies up to 36% of its mean value in the emitter layer, and up to 14% and 22% in the collector and base layers, respectively. The mean values of the specific contact resistance are 1.7×10^{-5} , 0.8×10^{-5} , and $5.0 \times 10^{-4} \Omega \cdot \text{cm}^2$ for emitter, collector, and base layers, respectively. In the range of 27°C – 300°C , both emitter and collector sheet resistances show nonmonotonous temperature dependence values, whereas the base sheet resistance decreases for increasing temperature. Measurement results for one die are collected in Table I for emitter, collector, and base.

A. Device Performance

Fig. 5(a) depicts the forward Gummel plot and β versus V_{BE} measured at 27°C and $V_{\text{BC}} = 0 \text{ V}$, whereas Fig. 5(b) shows the transistor output characteristic at the same temper-

TABLE I
SHEET RESISTANCE AND SPECIFIC CONTACT RESISTANCE MEASURED IN ONE DIE AT DIFFERENT TEMPERATURES FOR EMITTER (E), COLLECTOR (C), AND BASE (B) LAYERS

		27°C	100°C	200°C	300°C
E	Sheet resistance [Ω/square]	87	82	81	88
	Specific contact resistance [$\Omega \cdot \text{cm}^2$]	2.5×10^{-5}	2.1×10^{-5}	1.9×10^{-5}	1.7×10^{-5}
C	Sheet resistance [Ω/square]	162	147	144	157
	Specific contact resistance [$\Omega \cdot \text{cm}^2$]	1.6×10^{-5}	1.5×10^{-5}	1.2×10^{-5}	0.9×10^{-5}
B	Sheet resistance [$\text{K}\Omega/\text{square}$]	59	32	24	23
	Specific contact resistance [$\Omega \cdot \text{cm}^2$]	8.4×10^{-4}	5.0×10^{-4}	1.8×10^{-4}	1.1×10^{-4}

ature. β reaches its maximum value of 45 at $I_C = 20 \text{ mA}$ and abruptly drops for higher collector current because of high injection in the low-doped collector and forward biasing of the base-collector junction. The latter is the main reason for the gain reduction according to the Gummel plot. When the base-emitter voltage approaches 3.5 V and I_C is about 20 mA , I_B increases while the gain drops. Furthermore, Gummel plots measured at different fixed V_{CE} (6 and 8 V) collected in Fig. 6, together with that measured at $V_{\text{BC}} = 0 \text{ V}$, show a delay in the onset of BJT saturation, and so in the gain drop, proportional to the reverse voltage applied to the base-collector junction. However, no significant variations have been observed in the maximum β , as shown in the inset in Fig. 6. Device saturation is caused by the collector resistance R_C of the n-p-n and, in particular, by the lateral flow of I_C in the heavily doped collector layer, which constitutes the major contribution to R_C . Despite the high doping concentration ($1 \times 10^{19} \text{ cm}^{-3}$), the resistance seen by the collector current is significant because of the relatively small thickness of the layer and the device geometrical dimensions. In fact, the collector resistance, evaluated from the initial slope of the output characteristic depicted in Fig. 5(b), is about 150Ω . It is possible to reduce R_C by rescaling the

Fig. 5. Measured characteristic of the realized n-p-n transistor at 27°C . (a) Forward Gummel plot at $V_{BC} = 0\text{ V}$. (b) Forward output characteristic ($I_C - V_{CE}$) with I_B from 0 to 0.8 mA.

Fig. 6. Forward Gummel plot measured at 27°C on fabricated n-p-n with $V_{BC} = 0\text{ V}$ and different V_{CE} , i.e., 6 and 8 V. (Inset) Forward current gain versus I_C .

device size and, in particular, by reducing the distance between base layer edge and collector contact edge [see Fig. 1(b)], which is $17\text{-}\mu\text{m}$ wide. This distance has been designed responding to circuit layout issues rather than device performance. It is large enough to be crossed by an interconnection line in order to reduce the restrictions deriving from the use of a single metal layer.

Fig. 7 shows β and specific on-resistance R_{on-sp} temperature dependence of the fabricated n-p-n transistor: β drops

Fig. 7. Temperature dependence of forward current gain and specific on-resistance for fabricated n-p-n.

Fig. 8. $V_{IN} - V_{OR}$ characteristic simulated with LTspice and extracted SPICE models at 27°C and 200°C . (Insets) Simulated VTC and estimated NMs.

from 45 at 27°C to 21 at 300°C for a fixed base-collector voltage ($V_{BC} = 0\text{ V}$), whereas R_{on-sp} first decreases from 14 to $11\text{ m}\Omega \cdot \text{cm}^2$ when the temperature rises from 27°C up to 200°C , and then, it increases again to $12\text{ m}\Omega \cdot \text{cm}^2$ at 300°C , following the behavior of the n^+ collector sheet resistance (see Table I). As already noticed, the contribution to R_C coming from the high-doped collector layer, where the current laterally flows, dominates that due to the vertical current flow in the n^- collector layer.

B. Circuit Performance

1) *OR-NOR Gate*: DC simulations have been performed at $V_{EE} = -15\text{ V}$ and different temperatures when one input, i.e., A or B terminal in Fig. 2, is swept from -7 to 0 V and the other input is kept at -15 V . Simulated voltage transfer characteristics (VTCs) are shown in Figs. 8 and 9, together with the related high and low NMs for both the OR and NOR outputs. By increasing the temperature, the output high and low voltage levels (i.e., V_{OH} and V_{OL} , respectively) shift toward positive voltages due to the reduced voltage drop across the

Fig. 9. V_{IN} – V_{NOR} characteristic simulated with LTspice and extracted SPICE models at 27 °C and 200 °C. (Insets) Simulated VTC and estimated NMs.

base-emitter junction of the output transistor (see Q_7 and Q_8 in Fig. 2). Logic threshold V_S , defined as the central intersection point in the VTC, moves toward positive voltages too, as a consequence of shifting of the reference voltage (see V_{REF} in Fig. 2). The increase in V_S avoids the reduction of the NOR high NM by delaying the entrance in saturation of the input transistors (i.e., Q_1 or Q_2). This phenomenon is observed in the simulated VTC at 200 °C. When the input voltage is high enough to lead Q_1 or Q_2 to saturation, the output voltage is no more constant with respect to the input voltage but it starts to increase following the variation of the input voltage. When the temperature goes from 27 °C up to 200 °C, the simulated high NM NM_H goes from 0.7 to 0.8 V for both OR and NOR outputs, whereas NM_L goes from 1 to 0.9 V and from 0.9 to 0.8 V for OR and NOR outputs, respectively.

Measurements have been performed by applying the input signal, swept between -9 and 0 V, at one input (i.e., A or B) leaving the other one open. Due to the connection to V_{EE} through the pull-down resistor (i.e., R_{i1} or R_{i2}), a disconnected input terminal has a low voltage level applied to it. Measured VTCs at 27 °C, 100 °C, 200 °C, and 300 °C, together with estimated NMs, are shown in Figs. 10 and 11 for OR and NOR outputs, respectively, when -15 V supply is applied. Both measured high and low voltage levels, as well as the logic threshold, agree with the simulated ones and exhibit the same temperature behavior. Just as in the simulated characteristics (see Fig. 9), at input voltage close to 0 V, the input transistor saturates and affects the NOR output voltage (see Fig. 11). This phenomenon is more pronounced at higher temperatures. OR and NOR NMs are stable from 27 °C up to 300 °C: OR NM_H and NOR NM_L are about 1.1 V, whereas OR NM_L is about 0.9 V; only NOR NM_H slightly decreases when the temperature increases from 0.9 V at 27 °C to 0.8 V at 300 °C.

The static power dissipated in a single OR–NOR gate has been measured as 0.76 , 0.83 , 0.85 , and 0.82 W at 27 °C, 100 °C, 200 °C, and 300 °C, respectively, when the gate is operated on a -15 V supply.

Fig. 10. Measured V_{IN} – V_{OR} characteristic at 27 °C, 100 °C, 200 °C, and 300 °C. The temperature dependence of low and high NMs is shown in the inset.

Fig. 11. Measured V_{IN} – V_{NOR} characteristic at 27 °C, 100 °C, 200 °C, and 300 °C. The temperature dependence of low and high NMs is shown in the inset.

At 27 °C, the logic gate has been tested with different supply voltages V_{EE} in order to determine the lowest V_{EE} that provides acceptable NMs for the fabricated OR–NOR gate, since by reducing V_{EE} , the static power dissipated in the gate also decreases. Measured VTCs on -7 , -15 , and -20 V are depicted in Figs. 12 and 13. Operated on a -7 V supply voltage, the gate still exhibits low-to-high and high-to-low transitions, as shown in the inset in Fig. 12; however, the logic swing is only 0.1 V and NMs are negative. The lowest supply voltage that provides positive NMs is -9 V, as shown for OR and NOR outputs in Figs. 14 and 15, whose insets depict the variations of the logic levels and thresholds when V_{EE} ranges between -10 and -20 V. By increasing V_{EE} , both logic threshold and low voltage level gradually shift toward negative voltages, whereas the high logic level is almost unchanged. This behavior results in a larger logic swing and NMs for bigger V_{EE} (see Figs. 14 and 15); however, the dissipated power increases with the supply voltage.

Switching waveforms of the OR–NOR gate at room temperature are shown in Fig. 16. The measurements have been performed at $T = 27$ °C and $V_{EE} = -15$ V, with a peak-to-peak

Fig. 12. Measured VTC at 27 °C for the OR output with -7, -15, and -20 V voltage supply. (Inset) Detail of the output transition at $V_{EE} = -7$ V.

Fig. 13. Measured VTC at 27 °C for the NOR output with -7, -15, and -20 V voltage supply.

Fig. 14. Supply voltage dependence of OR output NMs at 27 °C. The logic threshold and the high and low logic levels dependence on V_{EE} are depicted in the inset.

input voltage of about 2.5 V centered about the logic threshold. Both the OR and NOR outputs exhibit asymmetric low-to-high (T_{PLH}) and high-to-low (T_{PHL}) propagation delays. Average propagation delays T_P are about 280 and 320 ns for OR and NOR outputs, respectively. Propagation delays, as well as rise and fall times, for both the outputs are shown in Fig. 16. A better estimation of the propagation delay achievable by the reported ECL technology is the one measured using the fabricated RO.

Fig. 15. Supply voltage dependence of NOR output NMs at 27 °C. The logic threshold and the high and low logic levels dependence on V_{EE} are depicted in the inset.

Fig. 16. Switching waveforms of the SiC ECL OR-NOR gate for both the outputs at 27 °C.

2) *RO*: Although three stages are enough to make the RO oscillate, due to a logic swing of the fundamental gate equal to about 2 V [11], the resulting oscillation period is not long enough to allow each gate to settle the nominal high or low output voltages. This phenomenon is shown in Fig. 17, which collects the output characteristic of the RO at 27 °C, 100 °C, 200 °C, and 300 °C and $V_{EE} = -15$ V. At 27 °C, the measured logic swing of the RO is about 0.7 V, whereas its maximum value, equal to half of the logic swing of the basic gate [11], is about 0.8 V, and the oscillation frequency is about 1.6 MHz, which results in a stage delay of about 105 ns. The reduced logic swing exhibited at 27 °C agrees with the measured rise

Fig. 17. Output characteristic of the three-stage RO at different temperatures, i.e., 27 °C, 100 °C, 200 °C, and 300 °C.

and fall times of the NOR output of the fundamental gate, which are larger than half of the oscillation period. Increasing the temperature, reduction of the logic swing and a nonmonotonous behavior of T_P have been observed (see Fig. 17). Measured propagation delays for the fundamental gate are 76, 60, and 62 ns at 100 °C, 200 °C, and 300 °C, respectively.

V. CONCLUSION

ECL ICs have been fabricated in 4H-SiC and successfully operated up to 300 °C. Stable NMs of about 1 V have been observed in the range of 27 °C–300 °C for the reported OR–NOR gate. An oscillation frequency of about 2 MHz has been observed for the fabricated RO in all the temperature ranges. Smaller propagation delay, as well as smaller circuit area, can be achieved for the OR–NOR gate by optimizing the circuit design. The reported IC technology is a promising candidate for even higher temperature applications.

ACKNOWLEDGMENT

VINNOVA Pioneering ICT program “High temperature electronic systems all in silicon carbide (SiC) for electric vehicles” is acknowledged for funding 2008–2011.

REFERENCES

- [1] C.-M. Zetterling, *Process Technology for Silicon Carbide Devices*. London, U.K.: IEE, 2002.
- [2] P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski, and M. Mehregany, “Extreme temperature 6H-SiC JFET integrated circuit technology,” *Phys. Stat. Sol. (A)*, vol. 206, no. 10, pp. 2329–2345, Oct. 2009.

- [3] S.-H. Ryu, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, “Digital CMOS ICs in 6H-SiC operating on a 5-V power supply,” *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 45–53, Jan. 1998.
- [4] D. Clark, E. P. Ramsay, A. E. Murphy, D. A. Smith, R. F. Thompson, R. A. R. Young, J. D. Cormack, J. McGonigal, C. Zhu, S. Finney, and J. Fletcher, “High temperature silicon carbide CMOS integrated circuits,” *Mater. Sci. Forum*, vol. 679/680, pp. 726–729, 2011.
- [5] S. Singh and J. A. Cooper, “Bipolar integrated circuits in 4H-SiC,” *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1084–1090, Apr. 2011.
- [6] [Online]. Available: <http://www.linear.com/software>
- [7] R. Ghandi, H.-S. Lee, M. Domeij, B. Buono, C.-M. Zetterling, and M. Östling, “Fabrication of 2700-V 12 mΩ · cm² non ion-implanted 4H-SiC BJTs with common-emitter current gain of 50,” *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1135–1137, Oct. 2008.
- [8] *Sentaurus TCAD version 10.0*. [Online]. Available: www.synopsys.com
- [9] W. R. Blood, Jr., *MECL System Design Handbook*. Phoenix, AZ: Motorola, May 1988.
- [10] R. Ghandi, B. Buono, M. Domeij, R. Esteve, A. Schöner, J. Han, S. Dimitrijević, S. A. Reshanov, C.-M. Zetterling, and M. Östling, “Surface-passivation effects on the performance of 4H-SiC BJTs,” *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 259–265, Jan. 2011.
- [11] M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode Logic CML ECL and SCL Digital Circuits*. New York: Springer-Verlag, 2005.

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