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Micromechanical Process Integration and Material Optimization for High Performance Silicon-Germanium Bolometers

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ABSTRACT

Semiconductor-based thermistors are very attractive sensor materials for uncooled thermal infrared (IR) bolometers. Very large scale heterogeneous integration of MEMS is an emerging technology that allows the integration of epitaxially grown, high-performance IR bolometer thermistor materials with pre-processed CMOS-based integrated circuits for the sensor read-out. Thermistor materials based on alternating silicon (Si) and silicon-germanium (SiGe) epitaxial layers have been demonstrated and their performance is continuously increasing. Compared to a single layer of silicon or SiGe, the temperature coefficient of resistance (TCR) can be strongly enhanced to about 3 %/K, by using thin alternating layers. In this paper we report on the optimization of alternating Si/SiGe layers by advanced physically based simulations, including quantum mechanical corrections. Our simulation framework provides reliable predictions for a wide range of SiGe layer compositions, including concentration gradients. Finally, our SiGe thermistor layers have been evaluated in terms of low-frequency noise performance, in order to optimize the bolometer detectivity.

INTRODUCTION

Imaging in the long wavelength infrared (LWIR) range from 8 to 14 μm is an excellent tool for non-contact measurement of temperature and for imaging of temperature patterns in applications such as thermography, surveillance and automotive night-vision [1-4]. IR imaging technology can be separated in two main realms; cooled detectors working with direct photon detection in the infrared wavelength, and uncooled thermal IR detectors that are based on heat absorption and the electrical measurement of the resulting temperature change of the detector membrane. Today, the vast majority of commercially available IR imaging systems utilizes uncooled IR bolometer focal plane array technology [5-17]. Uncooled IR bolometer focal plane arrays consist of matrixes of small suspended bolometer sensor membranes that are placed on top of CMOS-based integrated electronic circuits as depicted in Figure 1a. Figure 1b shows a SEM image of a typical IR bolometer pixel. For IR detection, the incoming IR radiation is absorbed by the bolometer membrane, thereby slightly increasing the temperature of the bolometer membrane. The small temperature increase changes the electrical resistance of the thermistor material that is integrated in the bolometer membrane. The change of electrical resistance of the bolometer thermistor is measured by the underlying electronic read-out integrated circuitry (ROIC) and transformed along with the signals from all arrayed IR bolometer pixels into a video output signal providing the IR images. To achieve a high IR sensitivity, the bolometer pixels have to be thermally isolated from the underlying substrate. This is achieved by implementing long and narrow legs between the bolometer membranes and the underlying substrate and by operating the bolometers in a vacuum atmosphere to provide a very low thermal conductance

between the bolometer membranes and the underlying substrate. Commercially available uncooled IR bolometer arrays are currently available from companies such as Ulis (France), Flir Systems (USA), BAE (USA) and others. These uncooled IR bolometer arrays have typical resolutions of 160x120, 320x240 and 640x480 pixels and bolometer pitches down to $17\text{ }\mu\text{m} \times 17\text{ }\mu\text{m}$ [10]. The bolometer thermistor materials of commercially available bolometer arrays are either vanadium oxide (VOx) [11] (e.g. Flir Systems and BAE) or specially developed amorphous silicon [15] (e.g. Ulis). In both cases, the bolometer material is deposited and patterned on top of pre-fabricated CMOS-based ROIC wafers [2-4]. This integration approach is referred to as monolithic integration. However, monolithic integration on CMOS wafers only allows deposition temperatures of below 400-450°C for the bolometer material. Therefore, the optimization of the bolometer thermistor material is difficult and the quality, uniformity and the yield of conventional bolometer thermistor materials are limited.

Figure 1. (a) Schematic drawing of surface micromachined bolometers after ref. [5] and (b) a typical bolometer design with a pixel pitch of $17\text{ }\mu\text{m} \times 17\text{ }\mu\text{m}$ [9].

Emerging very large scale heterogeneous 3D integration technologies for combining high-performance MEMS (Microelectromechanical System) on top of CMOS-based integrated circuit (IC) wafers provide opportunities to decouple the fabrication of the CMOS circuits and the manufacturing of the MEMS [18-23]. Thus, for IR bolometer applications the thermistor material can be manufactured and optimized using high-quality epitaxial deposition processes at elevated temperatures. Thereafter, the IR thermistor material is integrated on top of the pre-fabricated CMOS-based IC wafer. This allows the thermistor material to be optimized. The two most important performance parameters for IR bolometer thermistor materials are a high temperature coefficient of resistance (TCR) and a minimum low-frequency (LF) noise [10, 11].

This paper is organized in three main sections. In the first section the heterogeneous integration of MEMS based micro-bolometer arrays is briefly discussed. In the next section we address the optimization of TCR in alternating Si/SiGe layers. A physically based modeling scheme including quantum mechanical corrections is outlined. Finally we address the LF noise by studying various layers and also addressing the influence of pixel geometry and process induced degradation on noise performance.

THEORY OF UNCOOLED MICROBOLOMETERS

The noise equivalent temperature difference (NETD) is one of the most important performance parameters for infrared imaging systems and it is defined as the difference in temperature between two side-by-side blackbodies of large lateral extent which, when viewed by the infrared imaging system, gives rise to a difference in signal-to-noise-ratio of 1 in the

electrical outputs of the two halves of the array, viewing the two blackbodies. Infrared imaging systems based on uncooled bolometer arrays can today reach NETDs of as low as 25 mK with a F-number of the infrared optics of $F = 1$ [1, 8-11]. A detailed analysis of the bolometer design parameters influencing the NETD is provided in [10, 11]. From this analysis it can be seen that, to achieve a low NETD (equivalent to high bolometer sensitivity), the two most important design parameters for the temperature sensitive IR thermistor material are to obtain a high TCR, and at the same time minimum LF noise from the thermistor material. The definition of TCR is given by the relative change in resistance with the temperature normalized to a resistance R_0 at e.g. room temperature. It is desirable to have a TCR of at least 0.5 %/K in most practical applications. If we consider a material with a certain activation energy E_A for the electrical conduction mechanism we get the following useful relations:

$$R(T) = R_0 e^{\frac{E_A}{kT}} \quad (1)$$

where k is Boltzmann's constant. Taking the derivative we get the TCR as a function of temperature:

$$\alpha = TCR = \frac{1}{R(T)} \frac{\partial R}{\partial T} = -\frac{E_A}{kT^2} (\%/K) \quad (2)$$

Since we are dealing with semiconductors, it can be realized that the activation energies of shallow donor and acceptor levels, typically less than 50 meV, are too small to be considered to achieve reasonable TCR at room temperature. However, it turns out that polycrystalline silicon has TCR of about 0.5 % and amorphous silicon as high as 3 %, but the conduction mechanism here is different from single crystalline materials and will not be discussed further. Somewhat surprisingly it was realized that alternating layers of Si and SiGe layers showed a large TCR of about 3% and that the TCR value in fact was exponentially related to the band gap offset in this type of heterostructure. Empirical studies over a relatively wide range of Ge content x in the $\text{Si}_{1-x}\text{Ge}_x$ alloy confirm this [24-26]. In analogy with so-called quantum-well infrared photo-detectors, employing direct conversion of photon energy into free carriers, the term quantum well thermistors was used. However it turns out that the conduction of these heterostructures can be understood in terms of the more fundamental concept built-in potential at a junction.

For the LF noise we expect the noise spectrum show little or no dependence on lattice defects or surface states. Hence, the single crystalline material will only yield so called mobility or number fluctuation noise, which is well understood [27]. In reality, the integration of these types of materials in bolometer membranes adds a few challenges to this desired situation as will be illustrated below.

DISCUSSION

Heterogeneous integration of MEMS bolometers on IC wafers

Emerging very large scale heterogeneous integration technologies enable the integration of MEMS-based IR bolometers on top of CMOS-based integrated circuit (IC) wafers. A comprehensive review of heterogeneous integration technologies is provided in [18]. Complex multi-layer bolometer structures with a pixel pitch of down to 17 μm have already been demonstrated [7]. Figure 2 depicts a schematic view of a IR bolometer design based on a SiGe thermistor material. Figure 3 depicts an example of a heterogeneous integration process suitable

for IR bolometer arrays. This process is based on joining a SOI wafer containing the high-performance SiGe bolometer thermistor material with a pre-fabricated standard CMOS wafer using adhesive wafer bonding to transfer the pre-fabricated SiGe thermistor material to the CMOS wafer. For the subsequent formation of the bolometer pixels, industry-standard stepper lithography is used that enables the small bolometer feature sizes. A cross-sectional image of the bolometer membrane with the SiGe thermistor material and the current path for the temperature measurement is illustrated in the lower part of Figure 3. In the particular bolometer design shown in Figures 2 and 3, a vertical current flow from the top contact to the bottom is needed and therefore two series connected pixel halves are realized by creating a trench in the thermistor material. The vertical current flow is illustrated along with a series connection in the highly p-type doped bottom silicon layer.

Figure 2. Schematic of a typical bolometer pixel design made of a SiGe thermistor membrane.

Heterogeneous integration techniques allow that the SiGe bolometer thermistor material can be deposited on a silicon-on-insulator (SOI) donor wafer using high-performance and high-temperature epitaxial processes to obtain crystalline SiGe materials with superior TCR and LF noise properties. In our work both 100 mm and 200 mm diameter SOI wafers with a thin top silicon layer of a few 100 nm have been used. Typically, reduced pressure chemical vapor deposition (CVD) in a temperature range of 550-650 °C was employed. Under these conditions defect-free i.e. metastable SiGe layers with thicknesses of about 10-15 nm and Ge concentrations of up to 30 % can be realized. A cross-section of a grown sample on a SOI wafer is illustrated in Figure 4. As shown, the SiGe layer is embedded in between silicon layers. The top and bottom parts of the silicon layers are p-type doped to ensure that low resistance ohmic contacts can be formed. In many cases several SiGe layers are used e.g. a stack of four SiGe layers with thin undoped silicon spacer layers. The number of SiGe layers effectively serves to tune the resistance of the final stack and has negligible influence on the TCR value, as will be discussed below.

Figure 3. Heterogeneous integration process suitable for SiGe-based IR bolometers. The bottom part of the picture shows a bolometer cross-section together with the current path for the resistance measurement.

Figure 4. High-resolution cross-sectional SEM image of a thin SiGe layer with a Si spacer and highly doped top and bottom contacts, grown on a SOI substrate.

Materials for high TCR

Many previous studies have focused on maximizing the strain levels in the SiGe layers in order to get a large valence band offset and hence large TCR values. For normal CVD growth conditions the maximum Ge concentration has been limited to about 30%, except for a few cases where carbon has been added to stabilize the lattice [24]. Nevertheless, the TCR values for all these samples show a saturating trend, where it is difficult to reach a repeatable TCR in excess of

3%/K. Recently, we designed several samples with a single SiGe layer or even a single heterojunction achieved by a one-sided trapezoidal grading to be able to model the temperature response in a predictive manner. We observe that the resistance of a total stack including highly doped contacts, Si spacers and SiGe layers is given by:

$$R_{tot} \times area = \int_0^L \rho(x) dx = \int_0^L \frac{1}{qp(x)\mu_p(x)} dx \quad (3)$$

where $p(x)$ is the carrier concentration and $\mu_p(x)$ is the temperature dependent mobility and L is the total stack thickness. Since commonly used TCAD simulators [28] for semiconductor devices have very accurate models for strained SiGe incorporated we could simulate our different structures. Note that the carrier concentration is a function of applied bias, thus, an I-V sweep was set in the simulator and the carrier profile or resistance could be extracted at each bias point. Since the SiGe layers are thin we considered the quantum mechanical corrections by comparing solutions of either the Poisson or Schrödinger equations. The input to the simulator is a SiGe composition profile vs. depth and a doping profile. The TCR is extracted from simulations at temperature of 300 and 310 K. Examples of simulated position dependent mobility and carrier profiles are given in Figure 5a and 5b below.

Figure 5. (a) Temperature dependent mobility extracted from the device simulator [28]. (b) Zoomed-in view of hole concentration in the i-Si and SiGe regions, for classical and quantum-mechanical cases.

As shown in Figure 5b the presence of the hetero-junction induces an elevated carrier concentration inside the SiGe layer. The increased concentration is needed to accommodate the potential difference, caused by the bandgap offset. At the same time, the concentration outside the SiGe layer is reduced below the background doping level of $1 \times 10^{16} \text{ cm}^{-3}$, in order to maintain the total net charge, given by the acceptor dopant profile. The resulting effect is that the low doped Si regions exhibit large resistivity, while the top and contact region and the SiGe layer itself will have little contribution to the total resistance of the structure. If one plots the resistivity at 310 K normalized to 300 K, the origin of the effective negative TCR is easily seen. To highlight the difference between a Si/SiGe heterojunction structure and a silicon layer with the same dopant profile the ‘silicon only’ case is also included in the plot, as indicated in Figure 6. The calculated TCR values are -1.53 %/K and +0.46 %/K respectively.

Using either the Schrödinger equation or the approximate density gradient (DG) formalism we obtain -1.38 %/K and -1.37 %/K for a SiGe layer, while a silicon layer is not affected by quantum-mechanical corrections.

Figure 6. Origin of negative TCR for a sample with SiGe layer, as compared to doped silicon with positive TCR.

Finally, we demonstrate the TCR vs. bias for a graded SiGe profile. From the discussion above it can be understood that the carrier concentration under forward and reverse bias in such a structure would be different. This could be translated into a strongly bias-dependent resistance and TCR. Both experimental results and simulations confirm this, as illustrated in Figure 7. The qualitative agreement between measurement and simulation is satisfactory. A SIMS profile of the graded structure was not available so the simulated and measured devices could have different grading as well as a different maximum concentration as compared to the targeted nominal values.

Figure 7. Simulated and measured TCR for a graded SiGe profile

Materials for low noise

The main motivation behind the use of a SiGe single crystalline bolometer thermistor material is its inherently low noise. Generally the LF noise is of interest since the frame rate of the readout circuit is around 30-50 Hz. The thermal noise floor depends on the pixel resistance and shot noise proportional to the current should also be considered. However, these two latter noise sources are white, i.e. not frequency dependent. There have been many attempts to reduce the noise levels in conventional bolometer thermistor materials but amorphous materials such as VO_x and $\alpha\text{-Si}$ cannot be expected to compete with single crystalline materials. In order to analyze the noise level one normally considers the power spectral density S_V of the noise for a certain applied bias voltage V :

$$S_V = \frac{K_{1/f} V^2}{f} \quad (4)$$

where $K_{1/f}$ becomes a dimensionless constant since S_V has units of $[\text{V}^2/\text{Hz}]$. We consider voltage noise since the bolometer pixel is biased to a certain voltage during the signal readout sequence. This bias voltage could be a short pulse to avoid self-heating or a constant DC bias if thermal boundary conditions allow this. The noise data presented in this section are obtained for steady state bias conditions since the acquisition time is rather long, in the order of seconds, for an averaged spectrum including frequencies below 1 Hz. In most cases $K_{1/f}$ will be inversely proportional to sample cross-sectional area, i.e. the area of current flow. Only in the case, where dominant noise sources are located at the sample periphery, a scaling with periphery length will be observed. A localized defect in the sample volume could also act as a dominant noise source. An example of this situation would be an extended lattice defect (dislocation or stacking fault) occurring due to strain relaxation or non-optimized epitaxial growth conditions.

In a microbolometer array the pixel area is on the order of $25 \mu\text{m}^2$. In our noise investigations we have considered larger areas, 70×70 , 100×100 , 140×140 and $200 \times 200 \mu\text{m}^2$ for practical reasons that are related to the probing of the test structures. The area ratio for these samples is large enough to validate an investigation of noise level (noise constant $K_{1/f}$) vs. area. We address different epitaxial growth conditions where the thickness of the alternating SiGe well and Si barrier layers are varied. The test structure for noise and initial TCR characterizations is schematically outlined in Figure 8.

Figure 8. Test structure pixel for noise and TCR evaluation on SiGe epitaxial layers [25].

Within the error limits all samples present similar TCR values of more than 2% [25]. Therefore the sample with lowest noise would present the best detectivity. Figure 9a shows the extracted noise constant as a function of area for different well layer thicknesses with a fixed nominal barrier thickness of 26 nm. The three different samples all show scaling with pixel area, somewhat surprisingly the noise constant is seen to vary more than one order of magnitude. As will be discussed below, the noise spectra typically exhibit $1/f$ dependence while in a few cases an additional generation-recombination (G-R)-type noise source can be identified. The occurrence of G-R-type noise does not in general alter the conclusion, that an actual variation in $1/f$ -type noise is observed. It can be argued that the total strain in these layers is different and that the noise level is sensitive to strain-induced defects that do not affect the TCR value significantly. The impact of varying Si barrier thickness for a nominally fixed well at around 10 nm was investigated. All thicknesses in this experiment were determined by XRD with high accuracy. The results in Figure 9b can be interpreted in a similar way and for 14 nm well layer thickness, no conclusion can be drawn since only two areas yielded reliable data. Since the bolometer is a temperature sensitive device we also considered the noise level as function of ambient temperature. Again this condition differs slightly from the actual implementation in bolometers, where the pixel membranes have a high thermal isolation towards the substrate, which is typically operated at ambient temperature. In Figure 10 we illustrate two different types of noise spectra obtained at room temperature (RT) and elevated temperatures. At RT the noise power is proportional to $1/f$ while a G-R type of behavior appears at higher temperatures. This clearly suggested that the sample is not free from extended defects.

Figure 9. (a) Extracted noise constant as a function of area for different well thicknesses showing that the noise level can vary orders of magnitude. (b) Extracted noise constant as a function of barrier thickness showing noise level variation and scaling with pixel area.

Figure 10. LF noise spectra from a $70 \times 70 \mu\text{m}^2$ pixel at three different temperatures, showing appearance of excess G-R noise.

Finally, we point out that the test structures, which are oxide passivated and treated by a forming gas anneal, are optimized to suppress noise from etched pixel sidewalls and surfaces. In the actual implementation of integrated bolometers, mostly silicon nitride passivation layers are used and anneal steps are avoided to reduce the thermal budget after the thermistor layer transfer from the SOI wafer to the CMOS wafer. It seems that LF noise levels in these bolometers are significantly higher than shown here [9].

CONCLUSIONS

The heterogeneous integration of high-TCR microbolometers, featuring single crystalline SiGe thermistor layers, has been reviewed. The design of the SiGe profile has been discussed from first principles and physically based simulations were shown to predict the TCR as a function of bias and temperature. For typical SiGe layers of about 15 nm thickness, quantum mechanical corrections are of minor importance. The LF noise properties have been discussed in terms of pixel geometry and epitaxial layer design. Noise measurements on test structures show promising results, although a variation of about one order of magnitude was observed. Further special care has to be taken to preserve the noise properties of the as-grown layer when the actual micromechanical bolometer integration is implemented.

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