Performance estimation and Variability from Random Dopant Fluctuations in Multi-Gate Field Effect Transistors: a Simulation Study

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Performance estimation and Variability from Random Dopant Fluctuations in junctionless Multi-Gate FETs: a Simulation Study

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Abstract

As the formation of nearly abrupt p-n junctions in aggressively scaled transistors has become a complex task, a novel type of device in which there are no junctions has recently been suggested (J. P. Colinge et al., Nature 2010). The device of interest is referred to as the junctionless transistor, and it has demonstrated excellent functionality, with the advantage of a simpler fabrication process than conventional FETs.

Despite the remarkable performances exhibited by the junctionless transistor, this device has to be tested against variability before it may be produced in large scale. Hence, the study of how the fluctuations in the number and in the position of the dopant atoms affects a large number of devices has been developed in this work. Such variability source is referred to as Random Dopant Fluctuations (RDF) and it is among the most critical ones for conventional MOSFETs. Our view is that RDF ought to largely affect the junctionless transistors. Hence, in this work we mainly aim at investigating the impact of RDF in these type of devices.

Firstly, we provide a detailed analysis on the performance of an ideal junctionless transistor with a uniform non-random doping concentration, by mean of simulations developed using a TCAD software. Secondly, we investigate the effects of RDF in the junctionless transistor, as the principal aim of our study. Here, we determine how the I-V characteristics are affected by the random dopants and we illustrate fundamental the causes of the variations. A first estimation of the impact of RDF is provided by the illustration of the threshold voltage and β [1] distributions, and by the computation of the fundamental statistical quantities relating to the two parameters. A further and last estimation is provided by the comparison obtained studying RDF on the inversion mode FET.

Sammanfattning

Eftersom bildandet av abrupta pn-övergångar i aggressivt skalade transistorer har blivit en komplicerad uppgift, har en ny typ av komponent, där det inte finns några övergångar nyligen föreslagits (J. P. Colinge et al., Nature 2010). Komponenten kallas "junctionless transistor", och den har visat utmärkt funktionalitet, med fördelen av en enklare tillverkningsprocess jämfört med konventionella FET.

Trots anmärkningsvärda prestanda hos en "junctionless transistor", måste variabiliteten testas innan den kan produceras i stor skala. Därför har en studie av hur variationer i antal och i position hos dopämnes atomer påverkar ett stort antal komponenter gjorts i detta arbete. Denna typ av variationer kallas Random dopämnes fluktuationer (RDF) och är bland de mest kritiska för konventionella MOSFET. Vår uppfattning är att RDF till stor del borde påverka "junctionless transistorer". Därför siktar vi i detta arbete främst till att undersöka effekterna av RDF i denna typ av komponenter.

För det första ger vi en detaljerad analys av resultatet för en ideal "junctionless transistor" med en konstant non-random dopning koncentration, genom simuleringar som utvecklats med en TCAD programvara. För det andra undersöker vi effekterna av RDF i "junctionless transistor", som det främsta syftet med vår studie. Här bestämmer vi hur IV kurvor påverkas av slumpmässiga dopämnes fluktuationer och vi illustrerar de grundläggande orsakerna till variationerna. En första uppskattning av effekterna av RDF ges av tröskelspännings och β [1] fördelningar, och genom beräkning av de grundläggande statistiska kvantiteter för de två parametrarna. En ytterligare och sista uppskattning erhålls genom att studera RDF på inversion-mode FET.

Contents

Chapter 1

Introduction

All well established transistor technology relies on the formation of nearly abrupt p-n junctions between source/drain and channel region. Nonetheless, as scaling approaches the 10-20 nm nodes the fabrication of the junctions with very high doping concentration gradients is becoming an increasingly complex task.

Therefore, a novel device has been suggested, which does not involve the formation of any junction, and whose manufacturability is thus much simpler, even at such small dimensions. This new kind of FET, referred to as the junctionless transistor [2], is made using uniformly and heavily doped Silicon nanowires, and long channel devices have demonstrated excellent functionality [2], comparable to the best conventional transistors.

Nevertheless, before these devices may be produced in large scale they have to be tested against variability, which has become a major issue in devices with low dimensions. Specifically, we aim at investigating the effects of the Random Dopant Fluctuations (RDF) which is among the most critical variability sources for conventional MOSFETs. Our view is that RDF ought to be critical for the novel type devices considered here too. This study has been carried out by mean of simulations developed using a commercial simulator.

Hence, the main achievements of this work are summarized below:

- The performance estimation of the 2D SOI junctionless transistor and of the 3D multi-gate FET, both uniformly doped;
- The determination of the effect of different uniform doping levels in the I-Vs and in the extracted parameters;
- The analysis of the difference between simulations accounting for quantum effects and classical ones shown in the 3D device;
- The determination of the RDF impact on the junctionless device and the extraction of the V_{th} and β distributions, and of their statistical quantities;
- The illustration of the impact of RDF on the inversion mode FET, as a comparison with the junctionless one.

Chapter 2

The Multi-Gate Field Effect Transistor

Increasing efforts to shrink the dimensions of MOS transistors in order to increment performance and overall yield, have led to the introduction of new configurations of devices. In this context the Silicon on Insulator technology (SOI) has already proven to be successful for the reduction of parasitic capacitances arising from the substrate Si layer and from the source and drain regions, at the price of a higher design complexity. A further improvement is provided by the introduction of Multi-Gate FETs (MuGFETs), which allow for a better control on the channel electrostatics and for a higher drive current, despite the loss of planarity, which is typical of conventional MOSFETs.

Although the SOI structure is utilized in our work, the main focus is on a novel type of Multi-gate FET (i.e. the junctionless MuGFET). Hence, our discussion will limit to the latter technology providing the reader interested also in SOI with the references [3], [4]. Therefore, in this chapter we will give an overview of conventional MuGFETs first, and then a discussion on the junctionless MugFET will follow.

2.1 Overview of conventional Multi-Gate FETs

Since scaling trends impose a reduction in the characteristic device dimensions of approximately 30% at each generation technology, and bulk or SOI planar MOSFETs may not be able to efficiently control the conduction channel, the design of new structures has been intensively studied for the past twenty years. Hence, several configurations with the gate electrode surrounding or wrapping the channel region in different ways have been explored.

The main types are represented by double-gate FET, with two gate electrodes sandwiching the channel region, tri-gate and quadruple gate FETs, with one single electrode folded on three sides of the channel, or wrapped all around the channel, respectively. Slight variations on each of these structures are most common, however they are more often dictated by design and fabrication requirements, rather than effective improvement over device performance. For instance, Fig. 2.1 a) depicts the cross sections of the principal families of Multi-Gate devices, whereas b) shows the three-dimensional structures of a planar (top) and a multi-gate (bottom) FET.

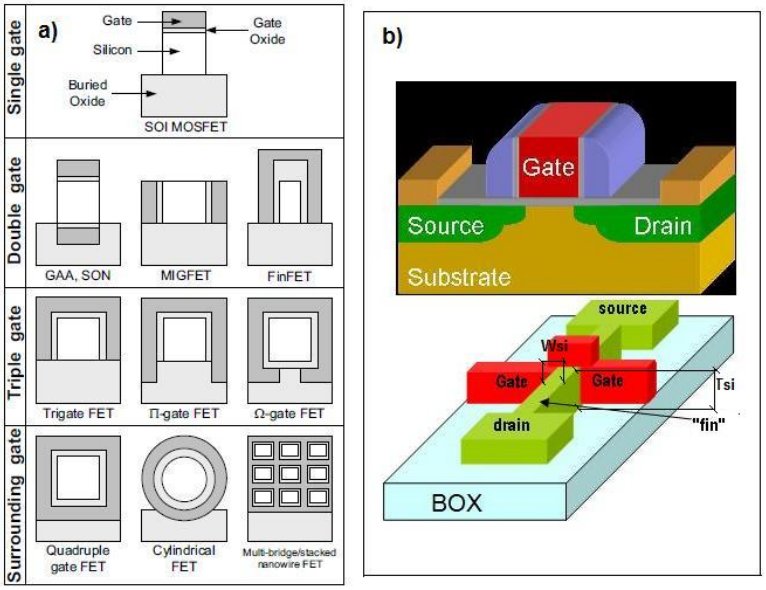


Figure 2.1: Cross sections of different gate structures (from [5])a). Scheme of a planar MOSFET (top) and a finFET (bottom) b).

2.1.1 Main advantages of Multi-Gate FETs

As mentioned before, the evolution from bulk or SOI planar MOSFETs to more complex multi-gate structures has been driven by the fact that the former technologies may not grant control over the channel electrostatics, especially in aggressively scaled devices. Issues of the kind, are commonly referred to as Short Channel Effects (SCEs), which thereby verify when the electric field from source and drain propagate through the depletion regions, hence contrasting the control acted by the gate electrode over the channel.

Although several types of SCEs can be distinguished, what we are considering in particular here is the DIBL (Drain Induced Barrier Lowering). The DIBL occurs when the height of a potential barrier – which would impede carriers' flow through the channel for a gate voltage below threshold ($V_G < V_{th}$) – is reduced by the electric field propagating from the drain through the de-

pletion region. Since higher V_{DS} will further decrease the barrier, an electron channel will form when a smaller gate voltage is applied. This will ultimately cause a reduction in the threshold voltage, and hence a direct measure of the DIBL can be given by the expression $DIBL = V_{th}(V_{DS_{small}}) - V_{th}(V_{DS_{high}})$, where $V_{DS_{small}}$ and $V_{DS_{high}}$ indicate the low and the high drain voltage values, respectively. From the description of such phenomena it stands to reason that MuGFETs in the sub-100 nm regime will be less affected by the DIBL compared to planar FETs of corresponding dimensions, owing to a better control over the field lines originating from S and D regions.

A further advantage observed in Multi-gate FETs, is the lower decrease in the threshold voltage as devices are scaled down. The reduction of V_{th} as the effective gate length L_{eff} is diminished, is referred to as threshold voltage roll-off and it represents another type of SCE, at which MuGFETs perform better than planar devices.

Moreover, Multi-gate devices, as well as Fully Depleted (FD) SOI planar FETs may reach the limit of a theoretical subthreshold slope $SS = 60$ mV dec^{-1}, which is defined according to the relation below from ref.[3]:

$$SS = \frac{kT}{q}\left(\frac{d(log_{10}I_{DS})}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right). \tag{2.1}$$

In these types of FETs the capacitance ratio $C_{dm}/C_{ox} \approx (\epsilon_{Si}t_{ox})/(\epsilon_{ox}W_{dm})$ is very small since the depletion width is extended through all the Silicon channel. Hence, they may reach such theoretical value for the subthreshold slope. Even though planar SOI FETs may reach this limit too, they do not allow for control over the gate electrostatics, which is as good as their Multi-gate counterpart.

Not only do MuGFETs exhibit a better behaviour at subthreshold and are less affected by SCEs, but also have a larger drive current. Indeed, I_{DS} increases approximately linearly with the number of gate interfaces [5] (i.e. twice for a double-gate, three times for a tri-gate etc.) and with the number of fins used in the overall device (as shown in the multiple fin structure in the bottom right figure 2.1 a)). For instance, the drain current in a tri-gate FET in the linear and saturation region is, respectively:

$$I_{DS} \approx \frac{C_{ox}}{L_G}\left(\mu_{top}W_{Si} + 2\mu_{lat}T_{Si}\right)\left(V_G - V_{th}\right)V_{DS} \tag{2.2}$$

$$I_{DS} \approx \frac{C_{ox}}{2L_G}\left(\mu_{top}W_{Si} + 2\mu_{lat}T_{Si}\right)\left(V_G - V_{th}^{'}\right)^2 \tag{2.3}$$

where W_{Si} and T_{Si} are the lateral and the vertical side of the Si fin, respectively, as indicated in fig. 2.1. Additionally, we have assumed a different mobility in the lateral and top interfaces with the gate oxide, μ_{lat} and μ_{top} , respectively. They are induced by the different scattering mechanisms given by the differently oriented Si surfaces at the interface with the oxide.

2.1.2 Drawbacks of MuGFETs and one possible solution

Despite the mentioned improvements, Multi-Gate FETs are not free of drawbacks, in particular the following detrimental effects have not improved from planar SOI MOSFETs, while they are common to both structures:

- Surface scattering is still present in low dimensional MuGFETs, since high electric fields (approximately $\epsilon_{eff} > 10^5 V/cm$) from the gate oxide may increase scattering due to surface roughness;

- Velocity saturation is detrimental for the performance of MuGFETs too, since steep potential gradients, caused by a small channel length may limit carrier mobility at the saturation region;

- Impact ionization, occurring with the formation of *e-h* pairs at high electric field regions close to the drain, may also affect MuGFETs' performance. Although it may be used in order to achieve a steeper *SS* [6], its effects may be detrimental as they may yield to breakdown [3].

Besides the phenomena described above, scattering events between different energy sub-bands – which are quantum mechanical in nature – may arise at dimensions so small that the electron channel either forms a 1 or 2 degenerate electron gas (1DEG or 2DEG) [7]. Such phenomena may obviously reduce the carrier mobility, and thus decrease the overall device performance.

Moreover, one last issue of MuGFETs compared to conventional planar MOSFETs resides in the increment of the processing complexity. Indeed, the loss of planarity is of main concern, since even aggressively scaled planar FETs would normally require increasingly smaller lithographic linewidth, the improvement in the control of etching and implantation techniques and of fast thermal annealing processes. Therefore, if this is translated into the fabrication of an more complicated structure, that is the MuGFET, such practical difficulty may even be of greater concern.

In particular, the fabrication of devices whose effective gate length will approach 10 nm in the next generation technology, requires very high doping concentration gradients in the junctions between *S/D* and channel region, for which ultra-fast thermal annealing processes are needed. The development of such advanced and costly techniques, which must also stand to the limits of a low thermal budget, presents a severe limitation on the further scalability of MuGFETs.

For this reason, recent studies ([8],[9] and [10]) have considered device structures that avoid the above-mentioned difficulty of forming junctions between *S/D* and the channel region, with so steep doping concentration gradients. Hence, the name junctionless transistor, that is the object of our study and refers to a device exhibiting a uniform doping polarity all over the channel, source and drain regions.

2.2 The junctionless Multi-Gate FET

The concept of a transistor without junctions appears appealing, since its fabrication avoids the difficulty in the formation of n-p junctions, which is especially encountered for devices below 50 nm gate length. Hence, if such type of device could show performance similar (or perhaps better) to the conventional MuGFET, it would represent a good alternative for the next generation technology.

The main advantage that the junctionless transistor presents compared with the conventional one, is that diffusion of carriers of inverse polarities does not occur in the device owing to a uniform doping concentration throughout the source, drain and channel regions. Therefore, the necessity of using millisecond annealing techniques to produce steep gradients is eliminated, and thus devices presenting a shorter channel length are easier to fabricate. The 2 fundamental requirements for producing a transistor without junctions may be outlined below [2]:

- The formation of a Si nanowire/nanoribbon, comprising the channel, source and drain regions, which has a cross section small enough so as to allow for a full depletion of carriers to switch off the device;

- A high doping concentration (i.e. n^+ or p^+) through all the nanowire in order to drive a sufficiently high current.

Accordingly, the use of high quality SOI structures and of electron beam lithography to pattern the thin nanowire are the main technological requirements for the development of a transistor without junctions. A further important step is to assure that implantation and subsequent annealing steps lead to a uniform heavy doping throughout the nanowire, typically in the range of $N_{D/A} = 10^{19} - 10^{20} cm^{-3}$. The pictures in 2.2 illustrate the scheme of a MuGFET and it highlights the different longitudinal cross-sections of a (a) junctionless and a conventional (b) transistor.

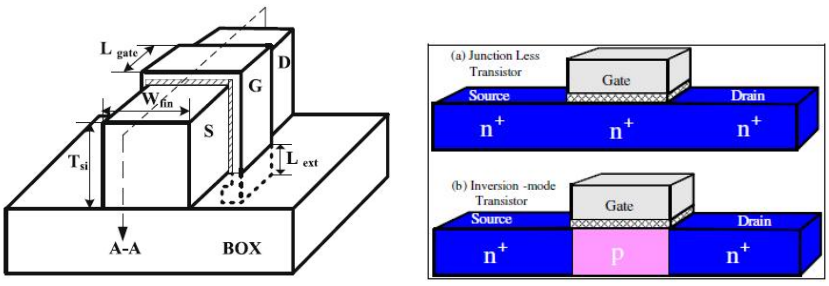


Figure 2.2: Scheme of a MuGFET (left) and longitudinal cross sections of a junctionless (a) and a conventional (b) FET, from [10].

2.2.1 Working principle of the Junctionless Transistor

Having outlined the fundamental processing techniques for the fabrication of a junctionless device, we pass now to the description of its physical properties. Indeed, whereas a typical MOSFET, as well as a conventional MuGFET works in inversion [3], accumulation is the mode of operation of a junctionless transistor.

Working in accumulation, the Junctionless transistor presents a number of different properties than conventional inversion mode FETs. First of all, whereas in inversion mode FETs a conduction channel begins to form at the interface with the gate oxide, in a nanowire junctionless transistor it forms in the middle of the nanowire at $V_G \sim V_{th}$, then it expands in the directions perpendicular to current flow as V_G is increased, until saturation is approached.

A clear illustration of such important phenomena is illustrated in fig.2.3, where a plot of the iso-surface of the electron concentration ($n \approx 10^{19}$ cm^{-3}) in the nanowire is shown at increasing values of the gate voltage. It can be clearly seen the above-mentioned formation of a conduction channel in the middle of the nanowire and its expansion in width and thickness.

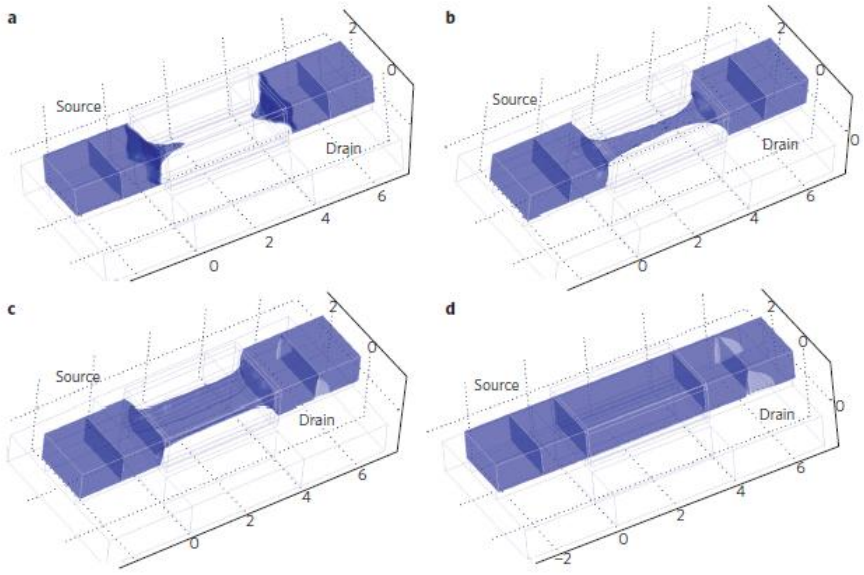


Figure 2.3: Formation of an electron channel in an n-type junctionless transistor. Iso-surface plots of the electron density resulting from a simulation $n \approx 10^{19}$ cm^{-3}. Electron density below threshold ($V_G < V_{th}$) (**a**); around threshold ($V_G \approx V_{th}$) (**b**); (**c**) above V_{th} (**c**); at saturation/flatband condition ($V_G \gg V_{th}$) (**d**), from [2].

The main reason for this phenomenon can be viewed by focusing on the energy band diagrams in a junctionless FET, and their bending at different values of gate voltage as depicted in fig.2.4, where for simplicity of the analytical model we focus on a cylindrical nanowire of radius r:

- At large negative bias below threshold (fig.2.4(a)) the conduction band bends upwards, forming a potential barrier which impedes the electron flow in the channel;
- As V_G is increased the bending diminishes, and at threshold (fig.2.4(b)) a narrow channel is formed in the middle of the NW, which is denoted by approximately flat bands at $r = 0$;
- As V_G is raised further (fig.2.4(c)), the bands will flatten out and the depletion region R_d will decrease, with the effect of an expansion of electrons in width and thickness;
- Ultimately, at $V_G = 0$ (fig.2.4(d)) full flatband condition is reached and the electrons will populate a wide region of the nanowire, experiencing a null transverse electric field.

A further characteristic of the junctionless FET is worth mentioning, that is these types of transistors are normally ON at zero gate bias [11], as it can be evinced from fig.2.4(c) and (d). Indeed, we must stress the fact that the electric field produced by reverse biasing the gate serves merely to deplete the nanowire region from electrons and thus to turn the device off. Hence, an electron channel will usually form at negative values of the gate voltage $V_T < V_G < 0$, if whatever positive drain voltage is applied, and provided that p^+-type poly-Si or a metal with a suitable work function is used as the gate electrode [10].

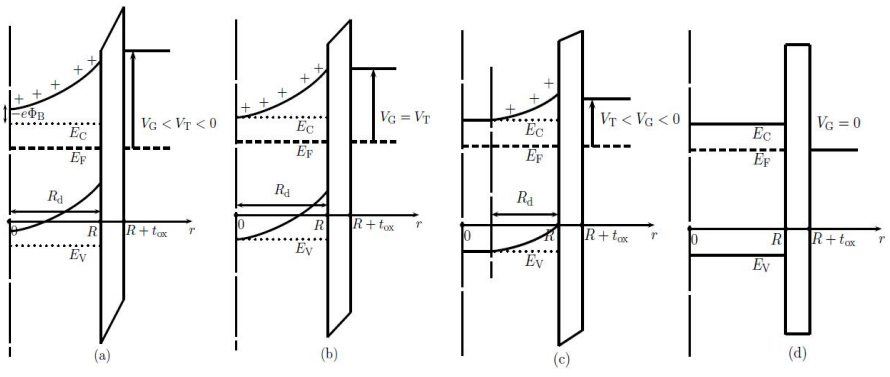


Figure 2.4: Energy bands in a junctionless nanowire FET at different applied gate voltage, provided by [9]. Band bending below V_T (a); bending at threshold $V_G = V_T$ (b); smaller bending and decrease in the depletion length R_d at $V_T < V_G < 0$ (c); flatband condition $V_G = 0$ (d).

2.3 Conventional vs Junctionless FETs

Having outlined the main differences between inversion and accumulation mode devices, we may compare their performances and transport properties in order to delineate the advantages of one with respect to the other and vice versa.

2.3.1 Performance Comparison

First of all, we may observe a comparison between the $I_D - V_G$ characteristics in fig.2.5 (**a**), derived from a simulation study performed on an inversion mode device and a junctionless one (from [10]). It may be seen that at such small dimensions (shown in the picture) the junctionless MuGFET outperforms the inversion-mode MugFET, in the fact that it has a lower subthreshold slope and DIBL (also shown in the figure).

Showing better performance at such small dimensions indicates that the junctionless transistor is less affected by SCEs with aggressive scaling. In fact, such behaviour can be evinced by looking at the plot in fig. 2.5(**b**), where the DIBL and the threshold roll-off have been computed for junctionless and inversion mode devices at different gate lengths. Both the roll-off and the DIBL increment are less pronounced in the junctionless FET compared with the inversion mode one. This makes the former type of devices more promising to meet with the scaling requirements of the next generation technologies.

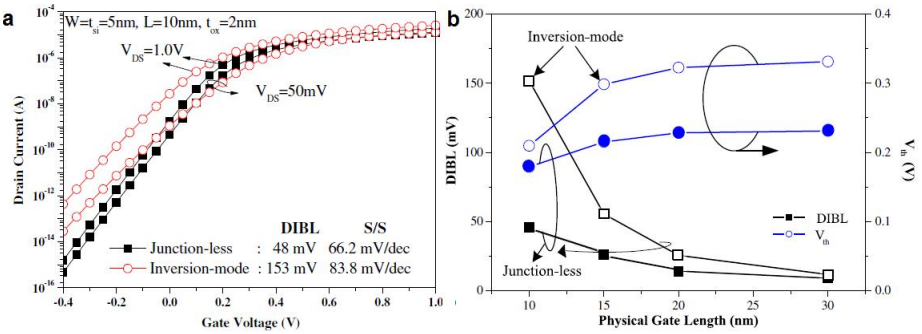


Figure 2.5: $I_D - V_G$ characteristics and extracted DIBL and SS of a junction-less and an inversion mode MuGFET with $L_G = 10$ nm (**a**); Extracted DIBL and V_{th} roll-off of junction-less and inversion mode MuGFETs with gate lengths from $L_G = 10$ nm to 30 nm, from (**b**), from [10].

2.3.2 Comparison of Transport Properties

Having a small off-current I_{OFF} is of main concern for all types of MOSFETs, and as we have seen in the picture 2.5(**a**), the junctionless device presents a smaller I_{OFF} than the inversion mode ones. As for the drive current it is obvious that it should be as large as possible. While the observed characteristics show a similar trend above threshold, the physics describing the electron flow is fundamentally different.

Indeed, whereas conventional MuGFETs present an inversion channel when fully turned on, and the drain current in the linear and saturation region obeys the laws approximately given by 2.2 and 2.3, the junctionless transistor essentially behaves like a common resistor, due to the fact that the carrier flow will experience an approximately null electric field from the gate.

Therefore, it just obeys to the simple Ohm's law which can be expressed as:

$$I \approx q\mu N_D \frac{T_{Si} W_{Si}}{L_G} V_{DS}. \tag{2.4}$$

By comparing the equation above with the form of the eqs. 2.2 and 2.3, it is obvious that the junctionless FET is apparently not affected by the oxide capacitance. Accordingly, scaling the thickness of the gate oxide t_{ox} is not a problem as crucial as it is for inversion mode devices, since one does not have to reduce t_{ox} to increase the current drive.

Furthermore, while the mobility enters the equations linearly for both type of devices, the scattering mechanisms affecting the two kind of MuGFETs are obviously different. The mobility in inversion mode FETs is mostly affected by scattering events occurring at the interface with the gate oxide and it is also limited by high gate electric fields, which peak exactly in the region of current flow [11]. On the other hand, conduction occurs in flatband conditions in junctionless FETs, in regions of low or zero field, and also in the middle of the nanowire/nanoribbon rather than at the oxide interface. Therefore, the mobility will be mostly limited by impurity scattering and by electron-phonon interactions and will be that of heavily doped bulk silicon.

Since the mobility represents one of the main issues in increasingly small devices, it is worth spending a few more words on it. In particular, a drawback of junctionless transistors with respect to inversion ones is the fact that electron mobility in the bulk heavily doped n-type (p-type) Si is around 100 (40) $\mathrm{cm^2V^{-1}s^{-1}}$, which is definitely smaller than typical values found in conventional inversion mode MuGFETs reported in the literature [2]. However, mobility in inversion mode FETs is so much affected by scaling, that if it were not for straining techniques – which are usable in junctionless devices as well – a reduction below 100 (40) $\mathrm{cm^2V^{-1}s^{-1}}$ would occur in sub-hundred nanometers devices. This is obvious if one considers that the values of the high electric field and the surface scattering induced mobilities will be progressively reduced as dimensions are shrunk. Therefore, accumulation mode FETs are supposed to show a better behaviour in aggressively scaled configurations, due to the fact that neither the electric field from the gate, nor the surface roughness play a role in the scattering phenomena.

In conclusion, we have provided the reader with an overview of the inversion and accumulation mode MuGFETs, pointing out the working principles, comparing their performances and transport properties. Hence, we may now focus on the analysis of how a variation from the design parameters in the channel doping affects the performances of a large ensemble of devices, which is referred to as a variability study on the fluctuation from random dopants.

Chapter 3

Introduction to Variability

This chapter is aimed at providing an introduction of variability in MOSFETs. Variability can be defined as the study of how the statistical variations in the design parameters, affect the performances of a large ensemble of devices.

Sources of variability can be generally distinguished into extrinsic and intrinsic ones; the former mainly consisting of deterministic type of variations shown from chip-to-chip or wafer-to-wafer, due to strain induced and layout induced changes between devices; the latter being concerned with statistical fluctuations from the design parameters induced by processing steps and/or by the nature of the particular phenomena of interest, that can be described only with statistical methods.

Our study is focused on a particular type of variability due to the fluctuations induced by the random placement of dopant atoms in the channel region. This analysis is commonly referred to as variability from Random Dopant Fluctuations (RDF) [12], [13]. A rather detailed overview of this source of intrinsic variability will be discussed in this chapter, whereas only a brief introduction to other possibly critical variation sources will be given, as they could be included in a future study on the junctionless MuGFET that we are concerned with.

A discussion of the principal variation sources such as the line edge roughness (LER) [14], oxide thickness variations (OTV) [15] and Poly-Si or Metal-Gate-Related variability ([16] and [17]) will be provided. Furthermore, we will analyse the main types of methods adopted for the investigation on Variability, usually carried out by numerical techniques.

However, for a review on variability, both intrinsic and extrinsic we refer for instance to K. Bernstein [12], whereas articles by Asenov can provide with a more detailed analysis on statistical (intrinsic) variability (e.g. references above plus [18] and [19] etc.).

3.1 Sources of Statistical Variability

Statistical Variability (SV) is of increasing concern in devices that are being scaled down to the deep sub-hundred-nanometre regime. 32 nm MOSFETs are already in production, and the manufacturability of deca-nanometre devices is predicted to be within reach in a decade, according to the ITRS 2009 [20].

At such small dimensions the control of processing steps in a large number of devices becomes so critical that bulk MOSFETs are not capable to stand a test against the variations produced by RDF, LER, OTV and Poly-Si-Gate-Related variability any more [21]. Moreover, due to the "discreteness of charge and granularity of matter (specifically of SiO_2, high-κs, Poly-Si and Metal gates)" [19], the variations in bulk MOSFETs would be too high to allow a mass production, even with a perfect processing control. The main reason for such issues is that the threshold voltage, being the principal quantity affected by SV, can suffer from variations of the order of 100 mV, which are too high for large scale fabrication.

Therefore, the study of SV in planar FD and Multi-Gate SOI FETs has recently commenced ([19], [21] and [22]), as these devices will replace bulk Si technology in the upcoming generations. Hence, we introduce to the main sources of SV and we include some of the recent studies, also to have a better outlook of what phenomena might have the greatest impact on SV in the next device generations.

3.1.1 Random Dopant Fluctuations

RDFs are produced by the placement of the dopant atoms in the channel – occurring in implantation steps – which obeys to statistical laws of nature, so that a doping profile totally corresponding to design conditions is unattainable. Moreover, the discreteness of charge does not allow for a uniform doping concentration, especially as dimensions are shrunk and such effect becomes more pronounced.

Besides the random positioning, fluctuations will occur also in the actual number of dopant atoms present in the channel region. While slight variations on this number are not crucial in sufficiently large channel volumes, they will become critical in deca-nanometre devices showing a moderate doping concentration.

For instance, MOSFETs of current technology typically have a moderately doped channel volume containing around 1000 impurity atoms, and slight variations of this number (e.g. ± 5 atoms) will not produce a significant change in the designed doping concentration (here only $\pm 0.5\%$). On the other hand, low dimensional MuGFETs having for instance a channel volume of $30 \times 10 \times 10$ nm^3 and a rather high design doping concentration of $N_D = 10^{18}$ cm^{-3} will present on average 3 atoms. Even the smallest variation on 1 single impurity will produce a change of more than 30%. If this already causes significant fluctuations over the design parameters, by taking into account also the random placement of these 3 ± 1 impurities, the impact of RDFs will be even more impressive.

Accordingly, RDFs will affect the devices' performances in the sense that they will show changes in their I-V characteristics (mostly shifts in V_{th}) owing to a different current transport occurring in each channel. It is then obvious that a particular doping profile may either favour carrier transport even at lower V_G, thus decreasing V_{th}, or contrast it, then producing an increment of V_{th}.

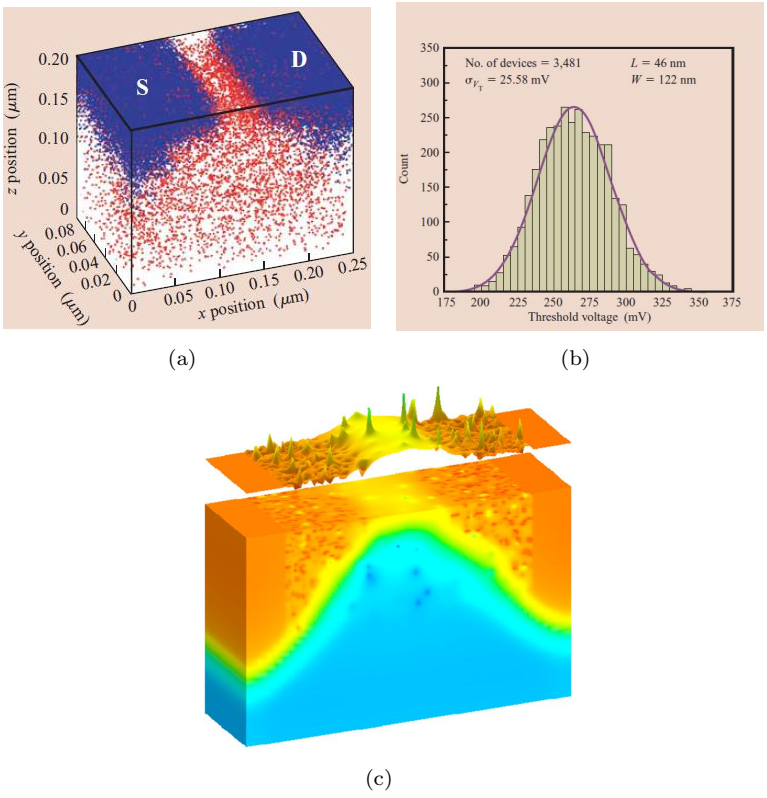


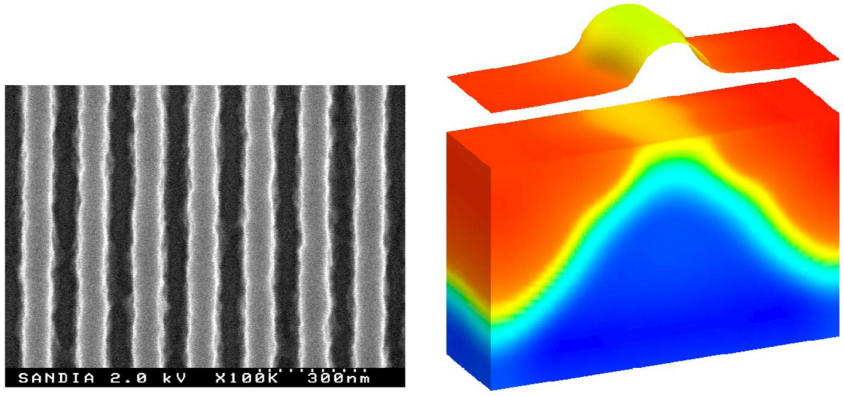
Figure 3.1: Placement of dopants 3.1(a), and Potential distribution 3.1(c), in an n-MOSFET produced by atomistic MC implantation and annealing simulations (gate not shown); frequency distribution of extracted V_{th} produced from the simulation of many devices 3.1(b), from [12] and [19].

A glance on the results from a typical analysis conducted on RDF is observed in fig. 3.1(a) and 3.1(c). Here the placement of impurities and the potential distribution derived from a Monte Carlo (MC) simulation of the implantation and annealing steps are shown, respectively. In addition, the threshold voltage distribution extracted from simulations carried out on a large number of devices is illustrated in fig. 3.1(b). The impact on the threshold voltage variations is evident from the figure and it is extremely desirable to sharpen the V_{th} distribution on the mean value, although this would hardly correspond to the value obtained as if the doping profile were chosen to be uniform throughout the channel [19]. Being RDF the focus of our work we will analyse in detail the models used to capture the physics of this phenomenon in section 3.2.

3.1.2 Line Edge Roughness

Another important source of SV is represented by Line Edge Roughness (LER), mainly produced by the variations in the number of incident photons during the lithographic exposure, and also owing to the molecular composition of the photoresist, which affects the chemical kinetics during development.

At present LER has reached the limit of approximately 5 nm [19], and it can be further scaled down only if EUV or e-beam lithography are adopted. This will cause sensible fluctuations in the devices' design and it has become one of the main limiting factors for device scaling below the 45 nm era, where a variation of 5 nm can cause significant changes in the MOSFETs' gate edges, being the most critical areas affected by LER. The consequences of LER on the photoresist edges can be seen in fig.3.2(a) and its effects on the potential distribution of a 35 nm MOSFET are depicted in fig. 3.2(b).



(a) (b)

Figure 3.2: Effects of LER in photoresist (Sandia Labs.) 3.2(a), and simulated potential distribution in a 35 nm MOSFET affected by LER 3.2(b), from [19].

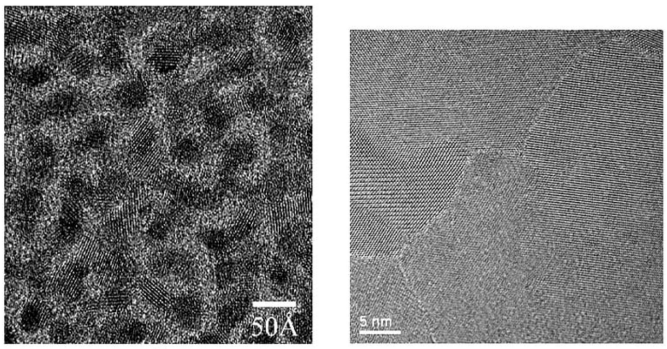
3.1.3 Other sources of Statistical Variability

While the Poly-Si granularity (PSG) of the gate and the oxide thickness variation (OTV) are problems that have already been addressed in a study of variability, some new ones are arising owing to the use of new materials in the oxide and gate stack, namely the variations in the granularity of high-κ materials and the workfunction change in metallic gates.

Oxide thickness variation (OTV) is introduced by changes in the surface roughness at the Si/SiO_2 interface. While OTV has been shown not to significantly affect variations of the threshold voltage in the technology nodes below 45 nm, its effects are supposed to increase as the dimensions are reduced, as it is obvious considering that surface effects become more pronounced at smaller L_G [15] and [18].

Poly-Si granularity (PSG) may also yield to an increase in the variability of devices. Indeed, grain size variations of the Poly-Si yield to changes in the gate workfunction and in the conductance in the Poly-Si. In addition, it may affect the potential inside the device produced by the applied gate voltage, and thus determine an uncontrolled shift in V_{th} [16].

Metal gate and high-κ materials have already been introduced in the recent technologies in order to reduce the effects of Poly-Si granularity, to increase conductance of the gate, and to redude gate leakage. Nevertheless, they may yield to further variations due to interface roughness and to the granularity of both types of materials. In particular the metal gate workfunction will be highly affected by the grain size and its variations can be critical for a good control over V_{th}. Recent variability studies have determined that the performances of novel FinFETs with a TiN metal gate are sensitive to variations of the workfunction, whose stabilization is a key factor to improve the control over V_{th} [17]. An illustration of the granularity in the HfON dielectrics and in the Metal gate producing workfunction variations is shown in fig. 3.3(a) and 3.3(b).



(a) (b)

Figure 3.3: Granularity in high-κ HfON (Sematech) 3.3(a), and in a metal gate yielding to changes in workfunction 3.3(b), from [19].

3.2 Modelling of Statistical Variability

Modelling of Semiconductor devices is a field that is well established now and the research volume in this area is constantly increasing, as Numerical Simulations allow for accurate estimation of device performance and also for the direct investigation of physics inside the device.

Moreover, variability is one of the most developed fields where Numerical Techniques are absolutely necessary in order to predict the dominating variation sources for each type of design configuration (e.g. planar FET or Multi-gate FET) and for each technological node.

In the following, we provide a background on the principal models adopted for solving the physics of MOS transistors, which are mostly used for a study on variability. Particularly, we will focus on those models aimed at giving a description of RDF.

3.2.1 Drift Diffusion Model (DD)

The drift diffusion model is the principal numerical technique used to predict the device physics under equilibrium conditions. It is based on the self-consistent solution of the Poisson equation 3.1, the drift-diffusion equations for the current density for electron and holes $\boldsymbol{J}_{n/p}$ eqs.3.2 and3.3, and the current continuity equations 3.4 and 3.5:

$$\nabla^2 V = -\frac{q}{\varepsilon}(p - n + N_D^+ - N_A^-) \tag{3.1}$$

$$\boldsymbol{J}_n = q\mu_n(-n\boldsymbol{\nabla}V + \frac{kT}{q}\boldsymbol{\nabla}n) \tag{3.2}$$

$$\boldsymbol{J}_p = q\mu_p(-p\boldsymbol{\nabla}V - \frac{kT}{q}\boldsymbol{\nabla}p) \tag{3.3}$$

$$\boldsymbol{\nabla}\cdot\boldsymbol{J}_n = qR(n,p) + q\frac{\partial n}{\partial t} \tag{3.4}$$

$$\boldsymbol{\nabla}\cdot\boldsymbol{J}_p = -qR(n,p) + q\frac{\partial p}{\partial t} \tag{3.5}$$

Where n, p, V and $R(n,p)$ indicate the electron and holes concentration, the electrostatic potential and the generation-recombination rate, respectively. The equations above form a non-linear equation system of 3 PDEs with 3 unknowns (i.e. the current density eqs. can be rewritten in terms of the continuity eqs.), which apart from simple cases, has to be solved numerically. Notice that the non-linearity is given by the mobility dependence on all the variables and by the generation-recombination term.

In the context of RDF analysis, while the drift diffusion model can predict the electrostatics inside the device, and it encompasses the behaviour at sub-threshold with the appearance of variations in the threshold voltage, it fails in capturing the fluctuations on the ON-current as well as on the maximum current. This is due to the fact that it does not take into account instantaneous scattering events and non-equilibrium carrier transport, that may be present in short channel devices [19]. In order to include such effects more complex models are to be used.

Moreover, if dopant atoms are introduced with an accurate atomistic approach (see for example fig 3.1(c)), the usage of a simple DD model may produce charge trapping in the coulomb wells formed by the discrete dopants. Such trapping is unphysical since the ground state energy is confined to a high state in the well, but this is not encompassed unless a quantum mechanical approach is used [19].

3.2.2 Density Gradient Model (DG)

In order to avoid the presence of unphysical charge trapping and also to capture the nano-scale physics typical of short channel devices, a quantum mechanical treatment must be adopted in the simulation of MuGFETs and also of the junctionless MuGFET we are concerned with. Although a rigorous quantum mechanical treatment is possible only if the Schrödinger equation is added to the eq. system 3.1-3.5, this can be replaced with an equation in terms of the electron/hole concentration, being able to predict the electron density quantization in the short channel device of interest.

Hence, the density gradient model is based on the solution of the eq. system 3.1-3.5 coupled with the equation below, assuming electrons are majority carriers[1]:

$$\frac{\hbar^2}{2rqm_{n^*_{(ij)}}}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} = \phi_n - V + \frac{k_BT}{q}\ln\frac{n}{n_i} \tag{3.6}$$

where ϕ_n is the quasi-Fermi Potential for electrons, r is a variable parameter and $m_{n^*_{(ij)}}$ is the effective mass tensor. Notice how eq. 3.6 resembles the Schrödinger equation in term of the electron density being the argument of the kinetic term in the LHS Laplacian, while the RHS contains the electrostatic and the quasi-Fermi Potential, and the thermal contribution given by the logarithmic term.

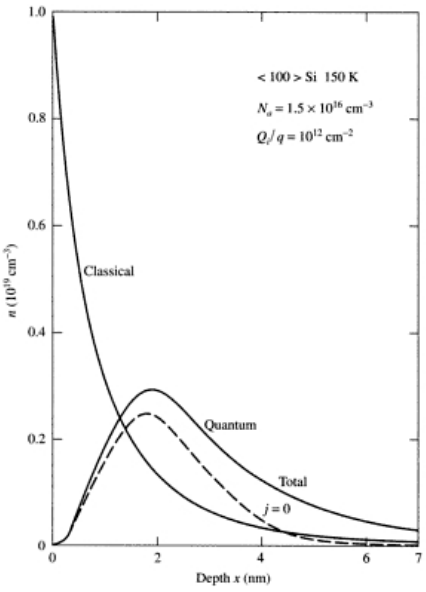


Figure 3.4: Classical and quantum mechanical electron density VS depth from the Si/SiO_2 interface, from [23].

[1]In all our study we have used only the DG equation for the majority carriers, being electrons, as the contribution from holes is negligible and taken into account already by the continuity equations.

Inclusion of eq. 3.6 in our equation system allows to correctly description of the carrier density at the Si-SiO_2 interface, which is of main importance in thin nanowire transistors, such as those to our interest. According to a quantum mechanical treatment the electron wavefunction – as well as the electron density – is null at said interface. This is required to match the boundary conditions obtained from the solution of the Schrödinger equation. On the other hand, the electron density is maximum according to a classical (DD) model. The DG model describes the electron density correctly as given by Quantum Mechanics, and it therefore gives reliable predictions of the physics of thin nanowire FETs. For this reason we choose to adopt the DG as the principal model in our calculations.

In order to visualize the difference between the erroneous classical and the quantum mechanical treatment of the interface, the illustration of the electron density in Si at distances away from the SiO_2 surface is shown in fig. 3.4.

3.2.3 More Advanced Models

With the use of the DG model coupled with the DD equations, the fundamental effects produced by RDF in the subthreshold region are captured. However, for a more rigorous treatment encompassing also the variations on the ON-current, more advanced techniques have to be used. As dimensions are shrunk these methods are more easily addressed, since the computational time though high, is quite reduced with respect to their use in bulk MOSFETs.

The Monte Carlo Method (MC) gives an accurate description of carrier transport in MOSFETs, hence it may account for the ON-current variability. Indeed, the carriers' trajectories in the channel are followed at each time instant and thus the presence of scattering events is extended over time, instead of being considered as if instantaneous [19]. Hence, quasi ballistic transport typical of short channel devices is encompassed with such methods. In addition, quantum confinement may be included in MC methods by adding a DG model. Therefore, the MC method allows for an accurate resolution of the physics of MOSFETs, for the determination of threshold voltage and ON-current variations induced by RDF.

Non-Equilibrium Green Function Techniques (NEGF) are even more complex and time consuming methods based on the Landauer formalism (see for instance [24]) to comprise quantum transport in the description of small dimension transistors. Despite its complexity, it allows for the resolution of non-equilibrium current transport given by Source to Drain tunnelling, which is no longer negligible in MOS transistors approaching the 22 and the 10 nm nodes. The NEGF technique is based on the solution of a Many-body Hamiltonian in terms of a single particle Green function, and it is a particularly fruitful method for the simulation of nanoscale devices with some sorts of "contacts" (meaning in general a non-equilibrium/irreversible process) [19] and [22].

3.2.4 Modelling of Random Dopant Fluctuations

Several models may be used to describe randomly placed dopants in the source, drain and channel region. The main ones are atomistic Monte Carlo, the Nearest-Grid-Point (NGP), Cloud-in-Cell (CIC) and Sano method [2].

Atomistic MC methods developed for the simulation of implantation and annealing steps, are widely used in TCAD simulations for the simplicity of implementation and their accuracy. However, they are not suitable for a RDF analysis where a large ensemble of devices has to be modelled, and they may yield to unphysical charge trapping in classical DD simulation, as pointed out in 3.2.1.

Models that do not require such a large CPU time and that avoid processing simulation steps, are also available in TCAD simulators that we are concerned with (e.g NGP, CIC and the Sano method). They may be used under the assumption of a uniform doping concentration. Then the doping profile is randomized according to the desired method. Although such methods may in general predict the physics of RDF, they rely on the assumptions of each type of model, and particular care has to be taken in case these methods are parameter dependent.

3.2.5 The Sano Method

The Sano method [26] and [27], the one adopted in our study (see e.g. 4.3), relies on the assumption that the dopant atoms produce long and short range Coulomb interactions which give rise to screening between each dopant. The characteristic length scale that separates the range of these interactions is given by the mean separation of dopants l_c, called screening length:

$$l_c \approx \frac{1}{2} N_{D/A}^{-1/3}. \tag{3.7}$$

The inverse of the screening length is the screening factor k_c which is a cut-off parameter, that is

$$k_c \approx 2 N_{D/A}^{1/3}. \tag{3.8}$$

It is obvious that this model strongly relies on the choice of the screening length, due to the fact that eqs. 3.7 and 3.8 represent magnitude orders estimations. The dependence on the screening length is evident from the fact that if l_c is too small compared to the average meshing step size, then screened charges are highly localized in the regions where each dopant atom resides. In this case the dominant part of the interaction is represented by the short-range screened potential. On the other hand, if l_c is too high, screening effects are averaged out and the doping profile appears smooth, and the decaying long-range potential represents the dominating part of the interaction.

In the first limit $l_c \to 0$ the dopant density resembles a δ-function, whose peaks reside in the position of each atom. In the opposite limit $l_c \to \infty$ the

[2] Our discussion focuses only on the Sano method. For a description of NGP and CIC see for instance [25]

doping profile resembles a continuous and uniform doping concentration. A more accurate discussion on the usage of the model and on the dependence of l_c will be given in 4.3, where we will adopt the Sano method in order to randomize the uniform doping profile for the simulation of RDF in junctionless MuGFETs.

Chapter 4

Simulation Analysis

This chapter aims at providing a detailed analysis of the simulation packages, developed using the TCAD software Sentaurus. Specifically, we will describe each fundamental step of the implemented packages, from the structure design to the solution of the physics in the device, and finally to the extraction of the parameters. This will provide the reader with a good understanding of the simulations it will prepare for the discussion of the results documented in Chap.5.

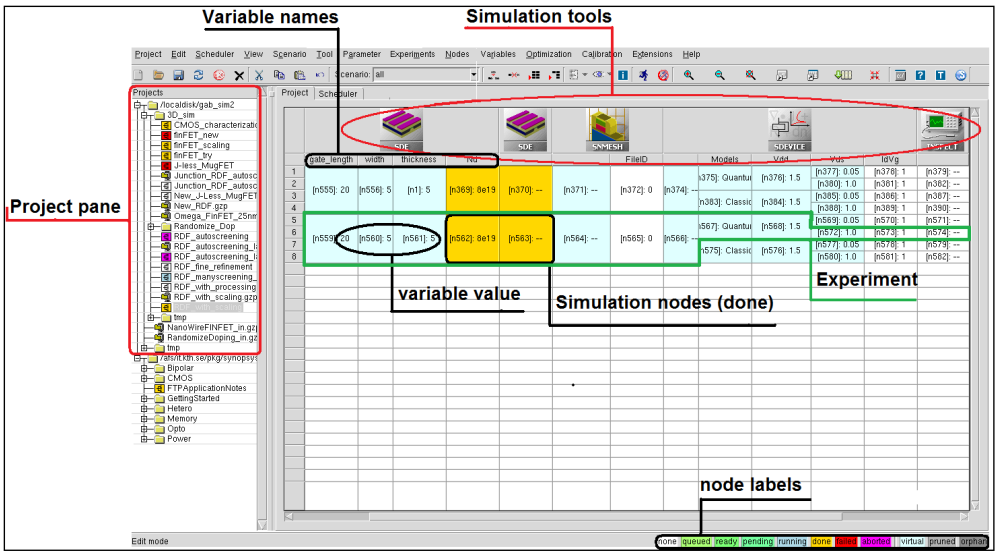


Figure 4.1: Sentaurus Workbench. Illustration of a project flow and highlights of main features.

4.1 Introduction to Sentaurus TCAD

Technology Computer-Aided Design (TCAD) simulations are widely used in the semiconductor industry, as well as in the Academia/Research Institutes, since the physics present in the devices and in the processing steps is accurately predicted by such tools. In this context, the TCAD software Sentaurus is well established for the simplicity of implementation of several packages and for its versatility, as a wide variety of devices can be studied. We have used Sentaurus in the study of the Junctionless transistor and on the impact of RDFs.

The main working environment in Sentaurus is the "Workbench", which is a graphical front integrating all the TCAD simulation tools into it. It is used to design, organize and run simulation projects. The illustration of a project flow that we have developed is shown in fig. 4.1, and the main Workbench features are summarized below [1]:

1. On the left of the figure there is the list of the developed simulation projects (project pane);

2. The environment at the right of it, comprising all the boxes (white, yellow, sky-blue etc..), represents one simulation project chosen from the list;

3. At the top of it, there are the simulation tools used in the project (encircled in red), which may be for the design of the structure, meshing, solution of device physics, etc.

4. The black rectangle below highlights the names of the variables/parameters that are defined in the Workbench environment, as well as in the input files corresponding to the related simulation tool[2];

5 Each box represents a particular node of the project. Running a node (e.g. we have run the yellow ones) will execute the input file of the related simulation tool, using the variable/parameter value of the node;

6. The green contour encircles one *experiment*, which is to be viewed from left to right. It represents the sequence of nodes, simulation tools and their input files that, when run, will give the results of the simulation according to the variables' node values;

7. Finally, the rectangle in the bottom right corner highlights the color labels used to identify the status of the node.

Having highlighted the main features and functionalities of the "Workbench" we may provide with a description of the simulation projects and to the tools utilized for their development.

[1] For a more extensive description we refer to the on-line tutorial[28] or to the manual [29]

[2] In order to parametrize a simulation project the variable names defined in the workbench must be called in the .cmd file using the syntax <@variable_name@> .

4.2 Structure and Design of junctionless FETs

The first step for the creation of a simulation project is the generation of the device structure. The tool that we have mostly used for this task is the Structure Editor, whose icon is shown in the top left corner of the fig.4.1. There are two possible alternatives for the development of a structure:

1. To draw or define each structure and material (e.g. Si channel, Poly-gate, gate oxide etc..) defined by a set of points in space forming closed contours;

2. To input a series commands for the deposition, lithography, etching etc.. that resemble the processing steps occurring used for the device fabrication.

The former approach is more suitable for a 2-D simulation, the latter is preferred in a 3-D one, as it is easier to generate complex structures with such method.

4.2.1 Structure generation of a 2-D SOI junctionless FET

In the early stages of our study we have developed a simulation of the junctionless FETs in order to explore some of the features of this device and also to become more acquainted with Sentaurus. Fig. 4.2 illustrates the structure drawn directly with the graphical interface of the "Mesh" tool, of simpler use than Structure "Editor". The top figure depicts the device structure enlightening the materials used for each layer and the source, drain and gate contacts, shown as red lines. The bottom figure depicts the mesh structure developed in the same tool to, which is needed to solve the physics in the device.

The mesh is defined by the minimum and maximum mesh step size and the region where the relating mesh step size is to be adopted. For instance, we have drawn a fine mesh in the channel region, as a great accuracy is needed to determine the electrostatics and the current transport in the channel. On the other hand, the poly-gate, BOX and *S/D* exhibit a coarser mesh as the needed resolution is not that high.

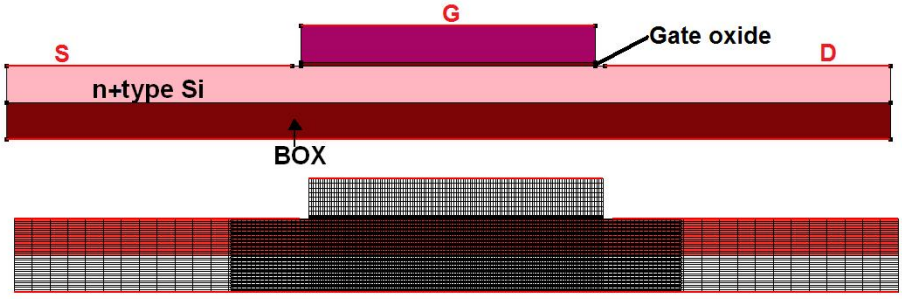


Figure 4.2: Device structure (top) and Mesh (bottom) of the 2-D SOI junctionless FET produced with "Mesh".

4.2.2 Structure generation of a 3-D junctionless MuGFET

For a more advanced study we have developed a more complex 3-D simulation, whose structure is shown in fig. 4.3. It has been generated according to the criterion **2** described above. Hence, we have given a set of commands as input in the "Structure Editor".cmd file, so that the run of a node will give as a result a device like the one shown. Notice that final structure **(a)** has been reflected from **(b)**, therefore, we only had to design half of the device and then make a call to a mirror function.

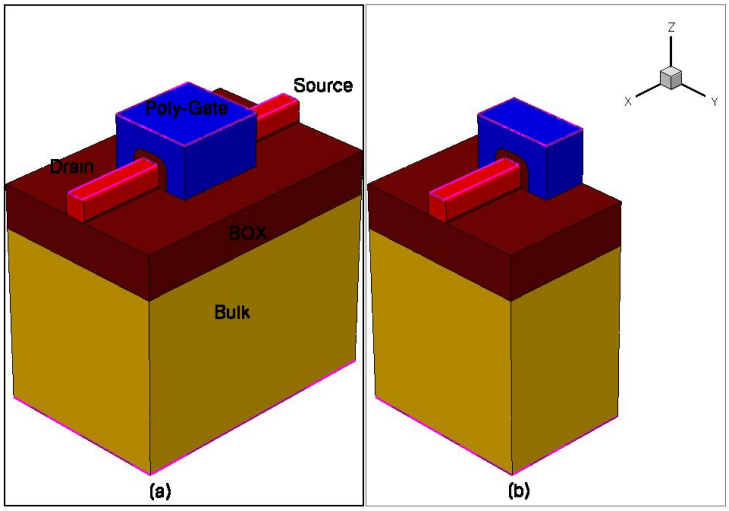


Figure 4.3: Geometrical structure of the Junctionless MuGFET generated with "Structure Editor", structure **(a)** reflected from **(b)**.

In order to give a glance on the type of commands , we insert some of the typical lines used for the structure generation, specifically for the definition of the Si nanowire on the top of the SOI layer:

```
;-0.0 SOI Wafer <-- this is a comment
(sdepe:add-substrate "material" "SiliconGermanium"    "thickness" Tsub)
(sdepe:depo          "material" "Oxide"      "thickness" Tbox)
(sdepe:depo          "material" "Silicon"    "thickness" Tsi)

;1 Define NW mask
(sdepe:generate-mask "POL" (list (list 0 Ynwmin Xmax Ynwmax)))
(sdepe:pattern "mask" "POL" "polarity" "light" "material" "Insulator1" "thickness" Thm)

;2 Etch NW layer
(sdepe:etch-material "material" "Silicon"  "depth" Tsi "type" "aniso" "algorithm" "sweep")
 ;-2.1 Remove mask
(sdepe:remove "material" "Insulator1")
```

All the commands above for the deposition, mask placement, lithography pattern, etching and mask removal are quite self-understandable. Moreover the parameters such as `Tbox`, `Tsi` etc.. have been defined in a parameter file .par which has been loaded in the .cmd file for their use.

4.2.3 Mesh of the 3D Junctionless FET

Since the design of a mesh which allows for accurate resolution of the simulated device is a complex task to achieve for a non-planar 3-D structure, we have decided to link the .cmd file for the structure generation to a further instance of the "Structure Editor" for the mesh definition.

We have used a meshing strategy based on a hierarchy of three refinement levels:

1. The definition of refinement regions with the related uniform minimum/maximum step size[3], for example:

```
; Meshing
;-- Substrate
(sdedr:define-refeval-window "SUB_RW" "Cuboid"   ; <--- placement of refinement region
  (position    0  (* -1000 Ymax ) 0)
  (position  (* 1000 Xmax) (*  1000 Ymax)  (* Zsub 1000 ) ))
(sdedr:define-refinement-size "SUB_RD"    ; <--- definition of minimum/maximum step size
  (/ Xmax 5.8) (/ Ymax 3.8) (/ Tsub 5.8)  ; <--- maximum
  (/ Xmax 6.2) (/ Ymax 4.2) (/ Tsub 6.2)) ; <--- minimum
(sdedr:define-refinement-placement "SUB_RP" "SUB_RD" "SUB_RW" )
;...After refining other regions we define the fine refinement in the channel
;-- Channel
(sdedr:define-refeval-window "Cha_RW" "Cuboid"
 (position  0   (* dYc 1000) (* 1000 Zepi1) )
 (position  (* L_spacer 1000) (* dYc_neg 1000) (* 1000 Zbox1)  ))
(sdedr:define-refinement-size "Cha_RD"
 (/  Lg 9.8) (/ WSi 9.8) (/ Tsi 9.8)
 (/  Lg 10.2) (/ WSi 10.2) (/ Tsi 10.2))
(sdedr:define-refinement-placement "Cha_RP" "Cha_RD" "Cha_RW" )
```

2. To refine those interfaces between materials needing greater resolution, with the use of the Grid Regularity function [27]. The nearer the interface the denser the mesh:

```
; Reg Grid
;-- Channel/Gate-oxide
 (sdenoffset:create-boundary "region" "R.SiEpi" "R.Oxide" ;<--names of interface regions
 "reggrid-regmode" "snap"
 "reggrid-uniform" (* (/ Lg 19.8) toum) (* (/ WSi  14.8) toum) (* (/ Tsi 14.8) toum) ; toum=1 here
 "reggrid-window"  (* Lg 1.2 toum) (* dYc toum) (* (- Zbox (/ Tsi 10.0)) toum)
                   (* Lg_refl 1.2 toum) (* dYc_neg toum) (* (+ Zepi (/ Tsi 10.0)) toum)
 "reggrid-minedgeratio" 0.2 ;<-- minimum increase of interface step size
 )
```

3. A further refinement at the interface, which is necessary for the use of the adopted mesh engine "noffset3d"[27]:

```
(sdenoffset:create-noffset-interface "region" "R.SiEpi" "R.Oxide"
 "hlocal" (* 4 A) ; minimum step size at interface in Angstrom
 "factor" 1.5     ; increase in step size from interface
 "window" (* L_spacer toum) (* dYc_neg toum) (* (- Zbox (/ Tsi 10.0)) toum)
          (* L_spacer_refl  toum) (* dYc toum) (* (+ Zepi (/ Tsi 10.0)) toum)
)
```

The structure resulting from this meshing strategy can be observed in fig.4.4, where the 3-D structure and several cross sections are shown. Fine mesh regions can be observed in the channel cross section, whereas coarser meshing is used in the bulk and in source and drain regions.

[3]Notice that there is a factor 1000 in the lines for the coordinates of the refinement regions, this is to solve a bug related to a wrong scale.

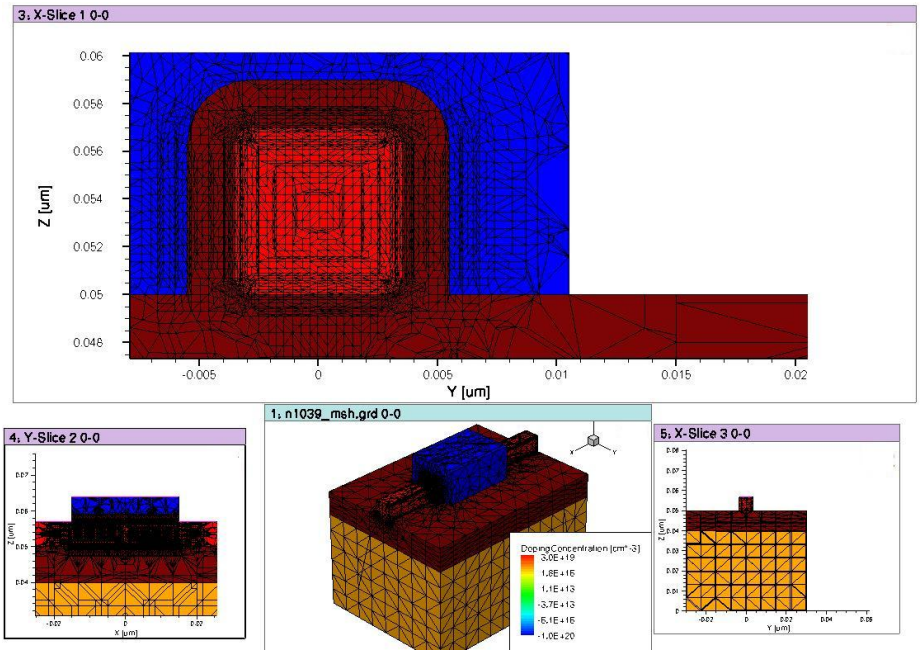


Figure 4.4: Meshing of the Junctionless MuGFET obtained according to the criteria explained in the text.

4.3 Randomization of Dopant Atoms

So far we have designed a device with a doping concentration _ chosen as a parameter/variable _ which is constant through source, drain and channel regions. Even though we also have simulated an ideal device with a uniform doping concentration in the range $N_D = 10^{19} - 10^{20}$ cm^{-3}, our principal focus is on the simulation of devices with randomly placed dopant atoms that give rise to fluctuations from the designed doping value.

A package for the randomization of the dopant atoms in the Si-nanowire has been developed for the achievement of this task. It is based on the tool named `RandomizeDoping` to be used with the "Sentaurus Mesh" tool [27], whose icon is the third one from the top-left corner in the fig.4.1.

This package loads the device and mesh structure developed in the previous steps of the project flow, and then it randomizes the doping concentration according to the chosen model. Specifically, we have adopted the Sano model [26], whose features have been described in 3.2.5. The `RandomizeDoping` tool takes the material as input and the species of impurities to be randomized. Then, an appropriate screening factor $k_c^{'}$ is chosen according to the law 3.8.

The resulting randomized profile will exhibit a non-homogeneous concentration gradient, from lower to higher concentration values, with peaks where the dopant atoms have been randomly placed. Furthermore, the number of impurity atoms inside the channel will be picked up randomly, within a certain tolerance, according to the channel volume and relating design doping concentration.

Below there is the code used in the described package for the dopant randomization, where we have parametrized the `FileID` and the `screening_factor`[4]:

```
Tools {
RandomizeDoping {
  DopingAssignment = "Sano"
  FileIndex=@FileID@ ; <-- it identifies the randomized structure
  NumberOfRandomizedProfiles = 1
    Material  "Silicon" {
         Species "ArsenicActiveConcentration" {
           ScreeningFactor = @screening_factor@
         }
      }
   }
}
```

The fig. 4.5 illustrates the results obtained by running the nodes relating to the `FileID` with different values of the screening length. It may be seen that the doping concentration in the nanowire is affected by the value chosen for the screening factor.

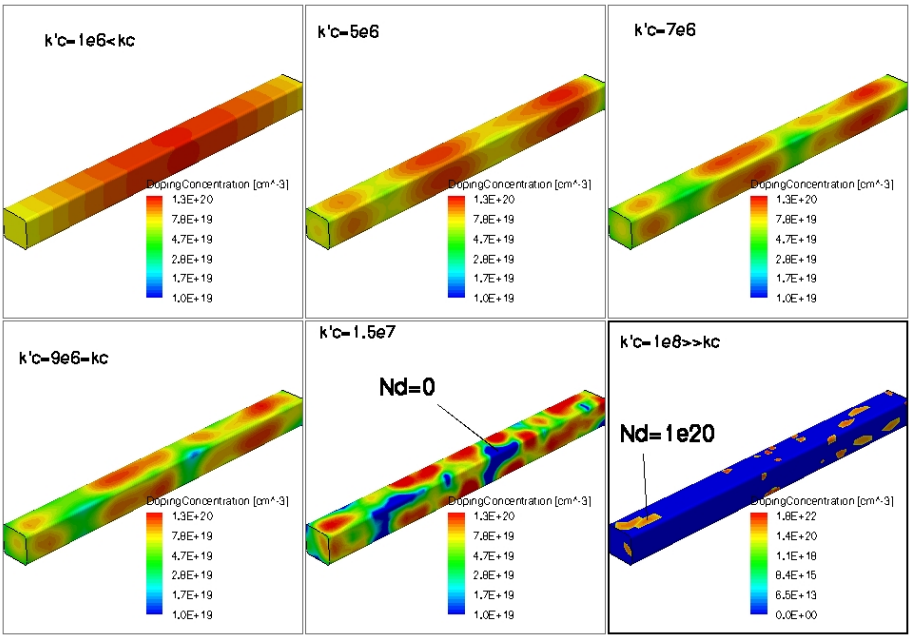


Figure 4.5: Randomized doping profile in the nanowire, obtained using different screening factors. Increasing screening factors are from the top-left to top-right corner, and then from bottom-left to bottom right.

[4]Since the function RandomizeDoping takes as input only the material and not specific regions, we had to set the bulk as SiGe and put the Ge mole fraction to zero.

According to the discussion in sect.3.2.5 the choice of a screening factor $k_c^{'} < k_c$ will spread the effects of the screening charges over a wide nanowire region, and in the limit $k_c^{'} \ll k_c$ it will give rise to a smooth and homogeneous doping profile. On the other hand, the dopants will be more affected by screening for $k_c^{'} > k_c$ and for instance, values $k_c^{'} \gg k_c$ will yield to a density of impurities resembling a δ-function. These features may be observed in the picture.

Furthermore, in fig.4.6 we may observe the different placement of the dopant atoms given by the randomization produced on several devices (with different `FileID`). Here, the nanowire is heavily n-type doped with a design concentration $N_D = 10^{20}$ cm^{-3}. The volume is $60 \times 5 \times 5$ nm^3, so that an average of 150 impurities are present in the nanowire. The screening factor used here $k_c^{'}$ is according to the law 3.8, namely $k_c^{'} \approx k_c = 8 \cdot 10^6$ cm^{-1}. However, we have explored also the effects produced also by other screening factors, in particular for values $k_c^{'} < k_c$ but within the same order of magnitude.

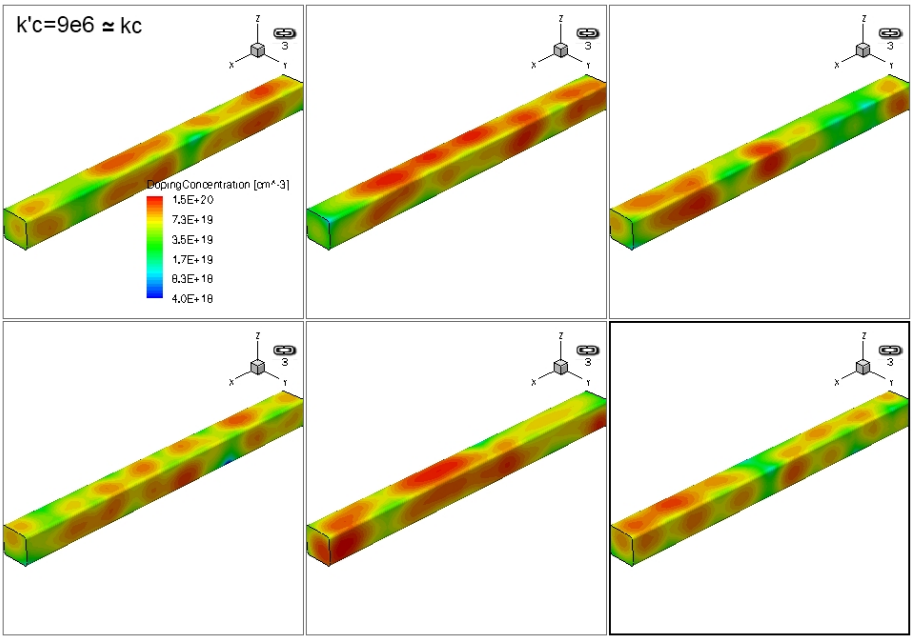


Figure 4.6: Different randomized doping profiles in the nanowires, obtained using a screening factor $k_c^{'} \approx k_c = 9 \cdot 10^6$ cm^{-1} .

4.4 Models used and Numerical Solution

After having randomized the doping profile in the Si nanowire, the device structure is loaded in the next simulation tools , that is "Sentaurus Device"[30]. The relating input file .cmd is utilized for the definition of the following settings relating to the solution of the physics in the device:

1. The physical models to be adopted in the MuGFET simulation, which are the M-B distribution of carriers (default one), band-gap narrowing model (`BGN`), the Schokley-Read-Hall model for generation and recombination (`GR`) and the Philips model (`Mob`) for the carriers' bulk mobility in Silicon[30][5] and the mobility degradation at the Si/SiO_2 interface due to transverse electric field(`Enormal`). The used models are shown in the piece of code below[6]:

```
Physics{!(puts $BGN)!}
Physics(Material="Silicon"){
 !(puts $GR)!
   Mobility(
      !(puts $Mob)!
      !(puts $HFS1)!
      !(puts $HFS2)!
      !(puts $Enormal)!
   )
}
```

2. The initial conditions at the contacts, that we have set up at zero, apart from the voltage at the gate electrode, being reverse biased, as illustrated below:

```
Electrode {
   { Name="source"    Voltage=0.0 }
   { Name="drain"     Voltage=0.0 }
   { Name="gate"      Voltage=-1.5}
   { Name="substrate" Voltage=0.0 }
```

3. The `Solve` section is used for the input of the equations to be solved numerically. An example of the code is shown below:

```
Solve {
*- Creating initial guess:
   Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts $DG)! }
   Coupled { !(puts "Poisson $DG $Major $Minor")! }
   Coupled(Method=ILS(set=2)){ !(puts "Poisson $DG $Major $Minor ")! }

*- Ramp to drain to Vd
   Quasistationary(
      InitialStep=1e-3 MaxStep=0.05 MinStep=1e-5 Increment=1.35
      Goal { Name="drain" Voltage=!(puts [expr $SIGN*@Vds@])! }
   ){ Coupled { !(puts "Poisson $DG $Major $Minor")! } }

*- Vg sweep
   NewCurrentFile="IdVg_"
   Quasistationary(
    InitialStep=1e-3 MaxStep=0.05 MinStep=1e-7 Increment=1.5
    Goal { Name="gate" Voltage=!(puts [expr SIGN*@Vdd@])! }
 ){ Coupled { !(puts "Poisson $DG $Major $Minor ")! }
     CurrentPlot( Time=(Range=(0 1) Intervals=20)  )
     Plot( FilePrefix="Snap_n@node@" NoOverWrite Time=( Range=(0 1.5) Intervals = 10 ) )  }}
```

[5] It includes the temperature dependence of the mobility, electronhole scattering, screening of ionized impurities by charge carriers and impurity scattering.

[6] All models have been renamed with simple variable names and the actual model string is called by $variable_name

A brief description of the code above is worth giving. The initial solution is obtained by coupling first the Poisson Eq. with the DG equation, and then also with the *e*-*h* continuity equations. Subsequently, the drain voltage sweep is executed and the system of the 4 coupled equations is solved until the value `Vds` is reached. Afterwards, an analogous method is used for the V_g sweep, which will terminate once the value `Vdd` is obtained. Moreover, the `CurrentPlot` statement saves the current and voltage values to obtain the I_d-V_g plots, whereas the `Plot` statement produces 10 snapshots of the device in order to visualize the physical properties inside the device.

Before concluding the chapter we wish to insert one list script taken from the output file .out of "Sentaurus Device", that has proven to be most useful in the identification of the issues relating to the crash of some simulation and also for checking the simulation runs. Moreover, the output files reports the CPU and the actual simulation time, which for a 2-D simulation is around 20 to 30 minutes, whereas for the 3-D ones is typically around 2 to 3 hours.

```
contact        voltage     electron current    hole current  conduction current
 drain        5.000E-02       4.891E-06         1.058E-23        4.891E-06
 source       0.000E+00      -4.891E-06        -1.058E-23       -4.891E-06
 gate         1.150E+00       0.000E+00         0.000E+00        0.000E+00
 substrate    0.000E+00       0.000E+00         0.000E+00        0.000E+00

Computing step from t=0.9001 to t=0.9004 (Stepsize: 3.0000e-04) :
Computing Coupled( 1 poisson-equation(s) , 1 eQuantumPotential-equation(s) ,
                   1 electron-equation(s) , 1 hole-equation(s) )
using Bank/Rose nonlinear solver.

Iteration   |Rhs|      factor     |step|     error   #inner  #iterative  time
-------------------------------------------------------------------------------
    0      6.77e+00                                                       9.71
    1      2.37e+01   1.00e+00   5.45e-04   7.16e+00    0        28     42.71
    2      7.07e+00   1.00e+00   1.54e-03   2.76e-02    0        29     72.41
Finished, because...
Error smaller than 1 ( 0.0276265 ).

Accumulated times:
Rhs time:       29.72 s
Jacobian time:   4.04 s
Solve time:     38.45 s
Total time:     72.41 s
```

The first part indicates the values of the main quantities determined in the simulation, that is the voltage and the current of majority and minority carrier at the electrodes. Then it follows the choice of the step `t` to solve the equation system at the next voltage value. Here the equations used and the numerical method used for finding the solution is written. Next, the solution of the eq. system is attempted and the corresponding table identifies iteration after which the system has converged. If the error is < 1 then the solution is found and the simulator proceeds analogously to determine the solution for the next voltage value.

Although the code above is for a simulation that has converged, we have experienced divergence problems. Specifically, non-convergence problems have occurred during the V_g sweep, that were caused by a wrong choice of the initial value for the gate voltage (e.g. see the script in the electrode section).

Indeed, the the relating current reached values below the tolerance of the simulator $\sim 10^{-19}$ A, and this caused the divergence in the solution of the equation system.

RDFs have augmented the problem as they produce a shift in the $I-V$ characteristics. Indeed, divergence has occasionally occurred even in cases where the chosen value for the initial gate voltage would not normally cause any problem, but it did in some particularly unlucky situations where the doping profile has caused a substantial change in the I-V, yielding to an initial OFF-current of $\sim 10^{-19}$ or below.

This is the main divergence issue, that can be avoided by regularly checking the output file and eventually by re-running the simulation with a different initial gate voltage value. More rare divergence issues occurred during the V_d sweep and also in the attempt to find the initial solution for the step `t=0` in the V_g sweep. Although less frequent an ultimate cause for these errors has not been determined.

Chapter 5

Simulation Results

In this chapter we present the results obtained from the simulations of the junctionless FETs. Specifically, the discussion of results will focus on the 2-D SOI FET simulation, as well as on the more elaborated 3-D one. In particular, both uniform channel doping and a randomized one have been considered in the development of the 3-D simulations.

From such study we aim at estimating the performance of the transistor without junctions, both using a 2-dimensional approximation and also a more accurate 3-D approach. Furthermore, we aim at predicting the impact of RDF in this type of devices.

5.1 Performance of 2-D junctionless FETs

Several simulations on the 2-D SOI junctionless FET, as described in in sect.4.2.1, have been run with "Sentaurus Device" for the determination of the I_D-V_G characteristics. We have considered devices n-type heavily doped, with uniform channel doping in the range $N_D = 10^{17} - 10^{20}$ cm^{-3}. As a first preliminary study we have designed a device with dimensions of gate length and Silicon thickness according to [2], that is $L_G = 1$ μm and $T_{Si} = 10$ nm. Furthermore, the oxide thickness and the buried oxide have dimensions $t_{ox} = 2$ nm and $BOX = 10$ nm, respectively.

Several I_D-V_G curves have been obtained from the solution of the Drift Diffusion model, and occasionally with the addition of Density Gradient model. However, a significant threshold voltage shift produced by QEs [23] has not been noticed in the latter case, owing to the large channel dimension. Moreover, we have observed the fundamental physical quantities, describing the electrostatics and the transport properties of the junctionless SOI transistor.

Here we report the characteristics obtained for the specified dimensions and for several values of the doping concentration. Indeed, fig. 5.1 illustrates the I_D-V_G curves obtained with several values for the doping concentration. Working devices are observed for doping concentrations in the range $N_D = 10^{17} - 5 \cdot 10^{18}$ cm^{-3}.

This is significantly less than what reported in [2], where donor impurities were implanted to yield a uniform concentration $\sim 10^{19}$ cm^{-3}. At such high doping levels (upper region of the figure 5.1) the simulated 2-D devices do not show any switching behaviour, as the current increases of less than a decade in the whole voltage range.

On the other hand, we see that the curves in the lower part of the picture show good performances:

- A large I_{ON}/I_{OFF}, reaching the maximum value of $\sim 10^{11}$, achieved for $N_D = 10^{18}$ cm^{-3});
- A subthreshold slope $SS \approx 80$ mV/dec for the device with the same N_D, which is within the tolerance of short-channel devices;
- Finally, they reach a high drive current from approximately $3 \cdot 10^{-5}$ to $2 \cdot 10^{-5}$ A. Only the device with a definitely smaller doping concentration of 10^{17} cm^{-3} has a smaller $I_{max} \approx 10^{-7}$ A.

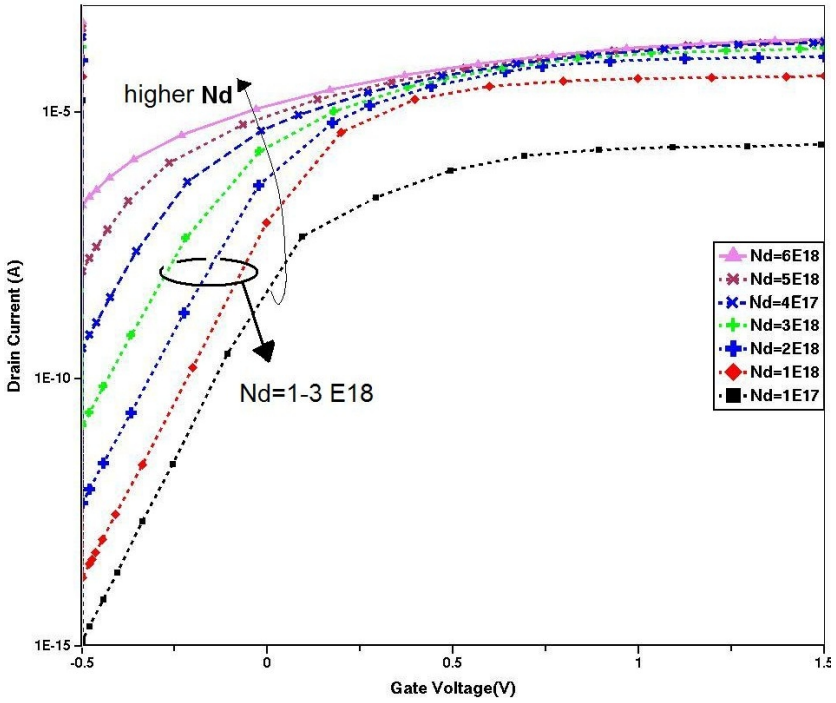
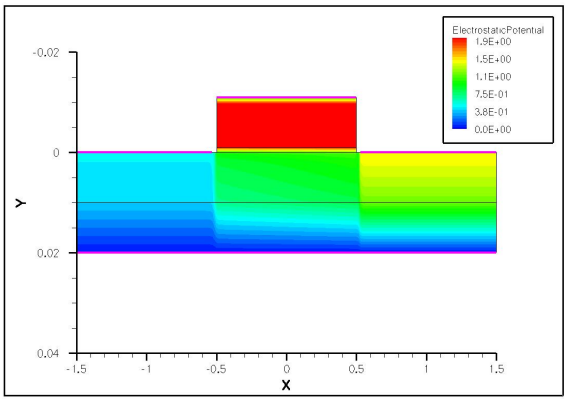
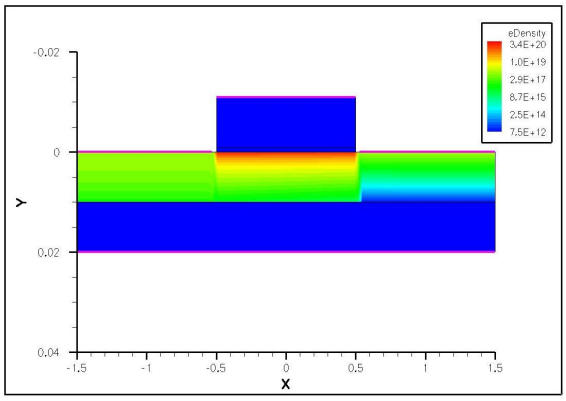


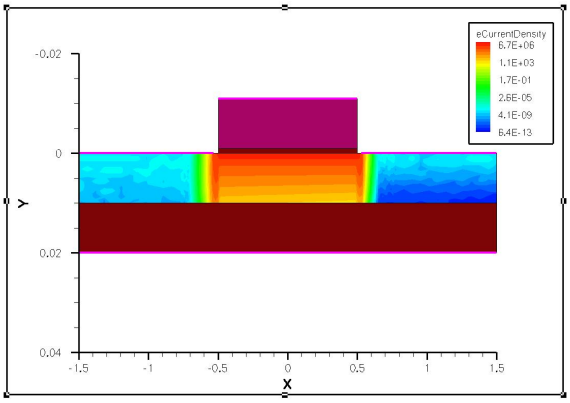
Figure 5.1: I_D-V_G characteristics obtained from the 2-D simulation of the junctionless SOI FET. Devices with $L_G = 1$ μm, $T_{Si} = 10$ nm and channel doping in the range $N_D = 10^{17} - 10^{20}$ cm^{-3} have been simulated.



(a)



(b)



(c)

Figure 5.2: Plots taken at $V_G = 1.5$ V of the electrostatic potential 5.2(a), electron carrier density 5.2(b) and current density 5.2(c), obtained from the 2-D SOI FET simulation with $N_D = 10^{18}$ cm^{-3}.

The plots 5.2(a)-5.2(c) illustrate the electrostatic potential, the electron and current density, respectively. The snapshots have been taken at the end of the voltage sweep at $V_G = 1.5$ V, with the current being at its maximum, and they refer to a device with a doping concentration $N_D = 10^{18}$ cm^{-3}.

As the electrostatic potential (fig. 5.2(a)) is small and approximately constant in the y-direction, the device is in flatband conditions with a null or very small electric field from the gate. This is in agreement with the working principle of the junctionless transistor. However, the other two figures 5.2(b) and 5.2(c) show that there is a pronounced gradient of the carrier and current density, which become larger as the interface with the gate oxide is approached.

This is a clear indication of the fact that the conduction channel starts to form in the interface with the gate oxide, rather then in the middle, as found in a juncionless MuGFET (as shown in fig.2.3). Therefore, we claim that one of the main causes for which we observed working devices with a smaller doping concentration than found in 3-D MuGFETs (i.e. $N_D \sim 10^{18}$ instead of $N_D \sim 10^{19}$ cm^{-3}), is due to the formation of the conduction channel at the gate-oxide interface rather than in the middle of the channel.

Indeed, simulated devices with a doping level $\sim 10^{19}$ cm^{-3} are normally ON even under reverse bias conditions. Here the electric field from the gate is not capable of impeding carriers' flow, which is formed in a thin region below the oxide. Besides, a further reduction of the gate voltage will not produce a significant change, as we have tried to reverse bias the devices up to -3 V and the resulting current was still too high.

Therefore, we conclude that a 3-dimensional simulation is necessary in order to accurately estimate the performance of the Junctionless MuGFET. In the following we present the results obtained from such a study.

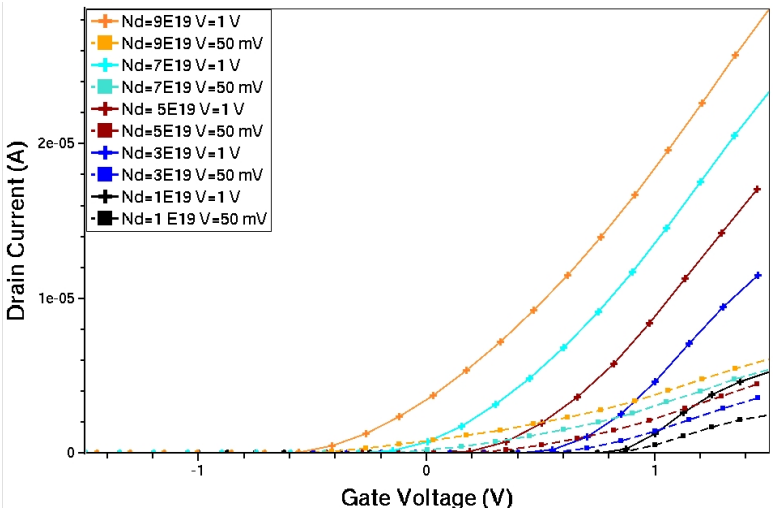
5.2 Ideal Junctionless MuGFET's performances

As the approximation of a MuGFET with its 2-dimensional cross section, taken in the direction parallel to current flow, has demonstrated not being capable of capturing some essential phenomena occurring in such device, we have decided to develop a more accurate 3-dimensional simulation. Here, we discuss the performance of an ideal device with a uniform channel doping.

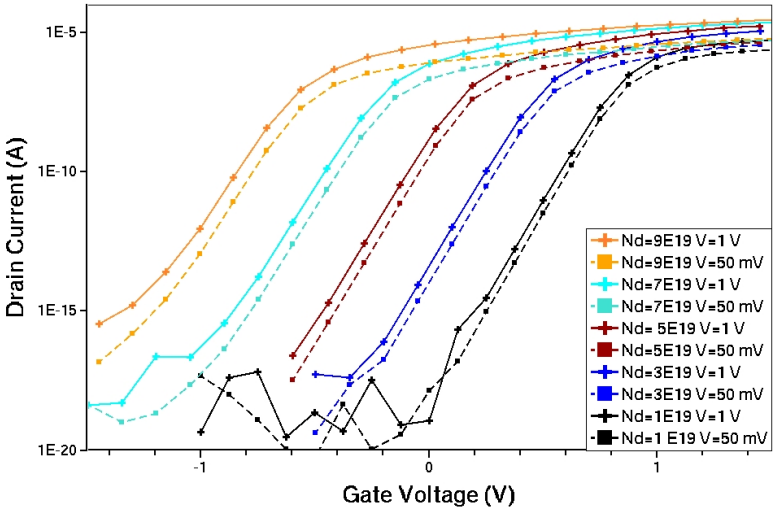
Table 5.1: Geometry and doping concentrations of the simulated junctionless MuGFETs.

	junctionless MuGFET				
4.2	N_D (cm^{-3})	$L_{G_{eff}}$ (nm)	T_{Si} (nm)	W_{Si}	t_{ox} (nm)
	$10^{19} - 10^{20}$	20	5	5	2

The devices under investigation refer to the structure and mesh shown in fig. 4.3 and 4.4. We have considered device dimensions and doping concentrations as reported in table 4.2. Besides, we have used the DD model in all simulations apart from the one with $N_D = 8 \cdot 10^{19}$ cm^{-3}, where the DG equation has been added to the eq. system, to compare the classical with the quantum mechanical model.



(a)



(b)

Figure 5.3: I_D-V_G characteristics (linear (a) and log (b)) at $V_D = 50$ mV (solid lines) and at $V_D = 1$ V (dashed), obtained from the simulations of the junctionless devices with concentrations $N_D = 10^{19} - 10^{20}$. The plots are for one every other N_Ds.

Indeed, the $I_D - V_G$ characteristics (see fig.5.3(a) and 5.3(b)) obtained at low and high drain voltage values, $V = 50$ mV and $V = 1$ V, respectively,

demonstrate the excellent functionality of such devices. Table 4.2 shows the extracted parameters to estimate device performance.

Table 5.2: Extracted parameters providing an estimation of the performances of the devices, labelled with the relating doping concentration. The threshold voltage is obtained with the maximum transconductance method at V_D = 50 mV, I_{ON}/I_{OFF} and I_{max} are for V_D=1 V.

$N_{D(10^{19}cm^{-3})}$	$I_{max(10^{-6}A)}$	$I_{ON}/I_{OFF(10^{10})}$	$SS_{(\pm 0.5\ mV/dec)}$	$V_{th(\pm 0.02\ V)}$	$DIBL_{(\pm 1\ mV)}$
1	5.3	2.4	71.3	0.85	25
2	9.4	4.0	72.3	0.77	37
3	11.8	17	72.4	0.51	23
4	15.1	8.8	73.1	0.36	46
5	18.0	24	75.2	0.20	53
6	20.9	17.4	76.1	0.06	56
7	23.4	16.7	83.2	-0.06	56
8	25	21.7	78.6	0.26	78
9	29.4	8.1	80.5	-0.58	78
10	31.4	6.6	86.9	-0.46	77

As a general trend, the higher the doping concentration the larger I_{max}, as stated by the eq. in 2.4. Furthermore, the characteristics are shifted towards smaller V_G values as the doping concentration is increased. Additionally, both the DIBL and the subthreshold slope become larger with higher N_D. The explanation for these effects is that the higher the doping, the more the mobile carriers, and thus the stronger the field needed for carrier depletion. Moreover, a larger depletion capacitance (or smaller depletion width) is the cause for a larger SS.

To further analyse the properties of the simulated MuGFETs, we present the iso-surface plots (fig. 5.4) of the electron density taken at n= 10^{20} cm^{-3}, relating to the device with $N_D = 8 \cdot 10^{19}$ cm^{-3}. The formation of the conduction channel at threshold and its extension in width and thickness as V_G is increased are evident. This is in agreement with the theory discussed in sect.2.2. This is the main feature is encompassed by our 3-dimensional simulation, not found in the 2-D one, where the channel formed at the interface with the gate-oxide and it spread towards the BOX.

Additionally, this mechanism gives us reason to believe the linear equation 2.4, valid in flatband condition is sound. As V_G is increased, the gate field will decay towards the centre of the nanowire. At threshold it will yield flat bands in the middle, with the subsequent channel formation. Then, at higher V_G there will be an extension of the channel and thus of the regions being at flatband. As in flatband conditions the transport properties are those of a simple resistor, eq.2.4 is valid in this context, and the device we are considering becomes then a "gated resistor"[2].

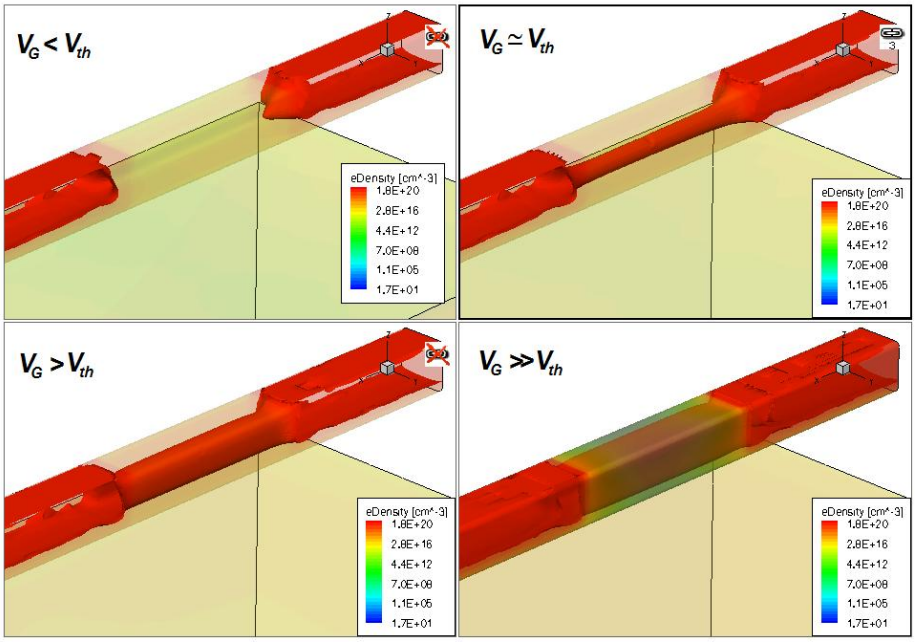


Figure 5.4: Iso-electron density plots taken at n= $8 \cdot 10^{19}$ cm^{-3} at different V_G values, relating to the device with $N_D = 8 \cdot 10^{19}$ cm^{-3}. It's apparent how the channel is formed in the middle of the NW and it's expanded in width and thickness as V_G is raised.

5.2.1 Quantum Effects in junctionless MuGFETs

Now we aim at investigating the effects of the quantum fluctuations produced by the fact that the channel region (forming a 2DEG) is so thin that Energy quantization may yield to non-negligible threshold voltage shifting [23].

Under the assumption of a free electron model, (i.e. neglecting e-e interactions and the interactions with the ions) which is valid to first approximation, we may treat the electrons as if only affected by a gate electrostatic potential that forms a potential barrier, and yields to the formation of a simple quantum well. Hence, in our discussion the quantum well resembles the region of the conduction channel formation, and it is limited by the potential barrier produced by the gate voltage.

If we further assume the potential barrier being infinite and we treat the system in 1 dimension, the particle will be confined in the region of the well of length L, and from a simple treatment of Quantum Mechanics the probability of finding it inside the well is given by:

$$|\Psi_n(x)|^2 = 2/L \sin^2(\frac{n\pi x}{L}) \tag{5.1}$$

We obtain the ground level probability for $n = 1$ and of the higher excited states for larger n.

The extension to 3 dimensions and to more complicated geometries, better resembling the potential barrier determined by the electrostatic potential, or a more accurate treatment of the potential not as infinite but decaying as $1/r$, is straightforward. However, it does not change the phenomenological picture we are trying to present here, which is represented by the sinusoidal-like behaviour of the electron probability distribution (in the range for x between 0 and L), and thus of the carrier density in the nanowire. Under these assumptions, the carriers formed in the conduction channel can be treated as if they were free particles with a probability distribution $\sim \sin^2(n\pi x/L)$, being maximum at $x = L/2$ and null at $x = L$ and $x = 0$.

If we compare the behaviour at threshold, of the carriers' probability distribution (or carriers' density) obtained from this simple quantum mechanical picture, with the classical treatment of the electron density derived from the DD model, we observe a similar trend. Indeed, at values $V_G \simeq V_{th}$ the density given according to the DD model is larger in the middle of the nanowire and it decreases at distances away from the centre, as the the potential barrier produced by the gate field is approached. This is similar to the quantum mechanical electron density $\sim \sin^2(n\pi x/L)$, and also to the density derived according to the DG model.

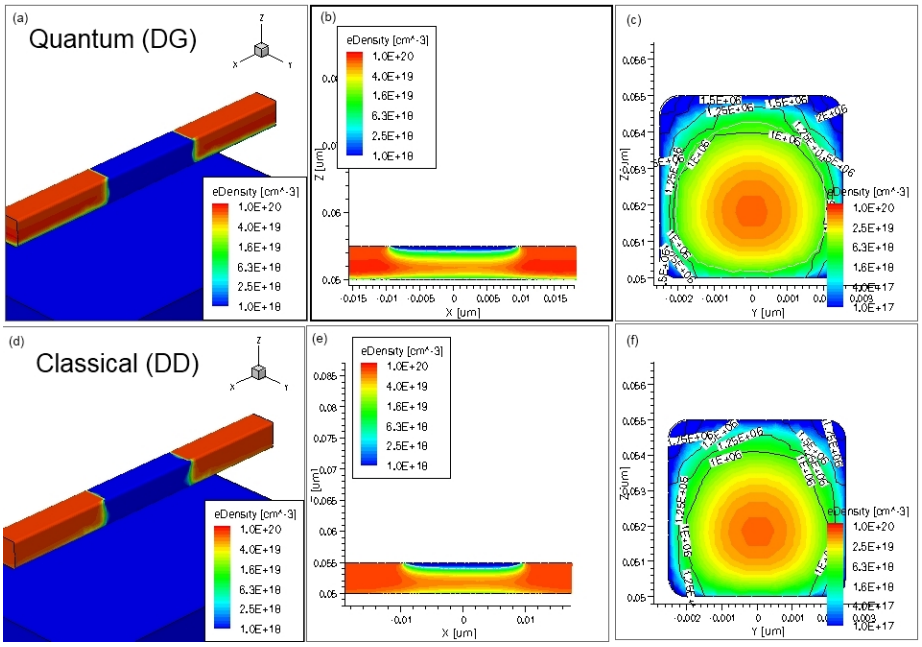


Figure 5.5: Electron density profiles, X and Y cross sections of the devices simulated according to the DG (fig. (a) to (c)) and to the DD (fig. (d) to (f)) model, obtained at $V_G \simeq V_{th}$. E-field lines are shown in (c) and (f).

In order to provide evidence of the similarity between the two effects, we present the electron density profiles and cross sections of the devices with $N_D = 8 \cdot 10^{-19}$ (fig. 5.5), obtained from a classical drift diffusion simulation and from a DG one. In the cross sections along the X-axis, we have also shown the lines of gate electric field, which impedes carriers' flow. Indeed, the carriers' density looks essentially the same in the two models, in agreement with our discussion.

If we instead compare the electron density distribution obtained at large gate voltage, as carriers have expanded throughout all the nanowire region, we observe a difference in the two models. This is the same effect as the one described in fig. 3.4. According to a classical treatment the electrons will be attracted to the gate-oxide at high positive V_G, whereas the wave function must be zero at the oxide interface in order to match the boundary conditions given by a quantum mechanical treatment. Hence, a substantial difference will be noticed in the electron density profile in the two cases. While in the DD simulation the nearer the gate-oxide the larger the electron density, in the DG simulation the electron density becomes smaller the closer it gets to the oxide. This is apparent in the fig.5.6, where the same type of plot as in fig.5.5 is shown, this time at high V_G.

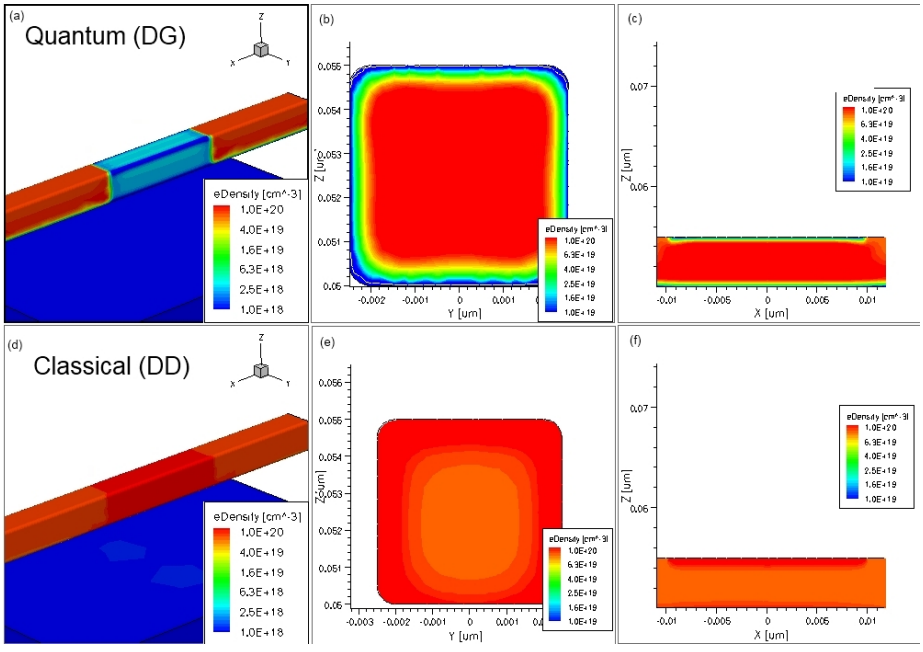
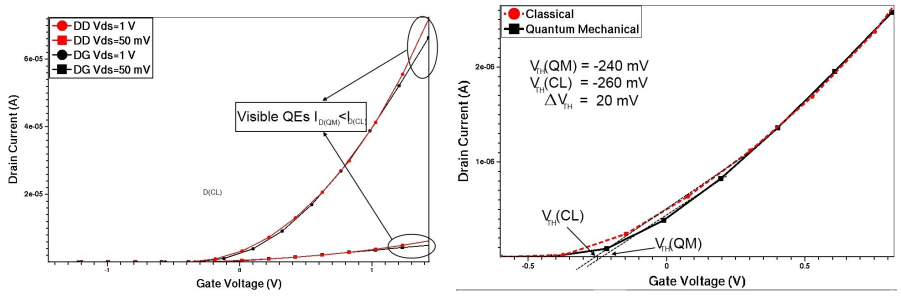


Figure 5.6: Electron density 3-D profiles, X and Y cross sections obtained at high V_G of the devices simulated according to the DG (fig. (a) to (c)) and to the DD (fig. (d) to (f)) model.

Accordingly, the classical simulation ought to present a slightly larger driving current than the DG one, due to the fact that the number of carriers in the channel volume is larger, remembering that $I_D \propto N_D$. Indeed, if we in-

tegrate the total carriers' density over the X-axis cross section, we obtain for the DD simulation $N_{DD}^{(-1)} = 2.77 \cdot 10^7$ cm^{-1}, while in the case of the DG one $N_{DG}^{(-1)} = 2.48 \cdot 10^7$ cm^{-1}. Although these two values are rather close, they have to be multiplied by the gate length $L_G = 20$ nm to have an estimation of the total number of carriers in the two cases, namely $N_{DD} \simeq 55$ and $N_{DG} \simeq 50$. In fact, the larger number of carriers present in the classical simulation will yield to a slight overestimation of the drain current, with respect to a more accurate DG one. This is what has been found when comparing the $I_D - V_G$ characteristics derived with the two models. The small reduction of the drive current when accounting for QEs can be observed in the fig. 5.7(a).

The two curves almost overlap at threshold (fig.5.7(b)), and the V_{th} increment due to quantum fluctuations is estimated to be around 30 to 40 mV, which is less than what found in inversion mode FETs [31]. The reason lies in the fact that the channel is formed in the middle of the NW, and thus the classical prediction gives results similar to the quantum mechanical one. On the other hand, in inversion mode devices the V_{th} increment due to QEs is more pronounced, since the wave function (and thus the el. density) has to to be zero at the oxide interface to match the boundary conditions. This is in contrast with a classical treatment where the electron density is maximum at such interface.



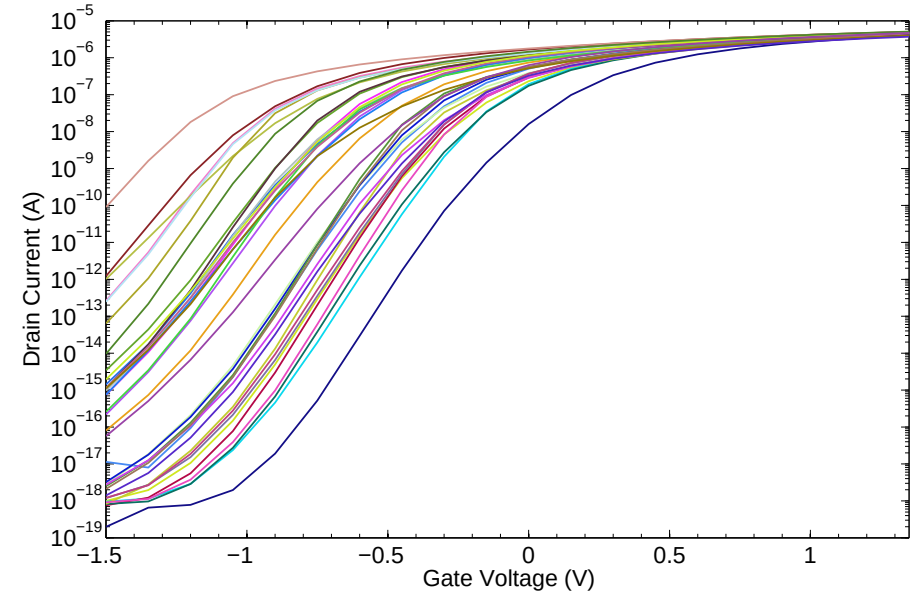
(a) (b)

Figure 5.7: Comparison between the $I_D - V_G$ characteristics obtained from a DD and a DG simulation at low and high drain bias (a) and magnification at threshold (b).

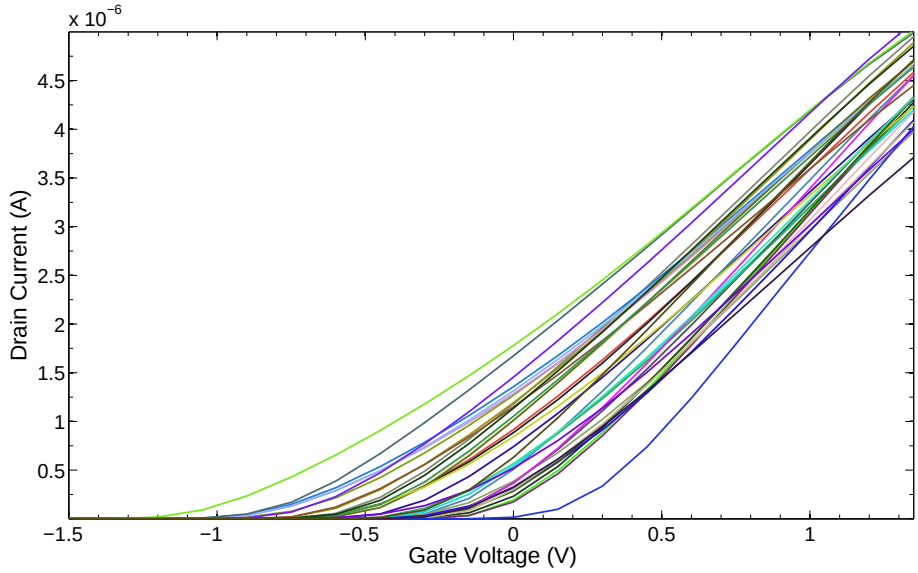
5.3 RDF in junctionless MugFETs

Having presented the junctionless transistor with ideal doping, we may discuss how the fluctuations from random dopants affect the performance of the device of interest. The Sano model [26]has been used for the dopant randomization (see sect.3.2.5 and 4.3). The simulated devices have dimensions as specified in the table 4.2, with a design doping profile $N_D = 10^{20}$ cm^{-3}. We have run 36 simulations each with a different randomized doping profile. The screening factor $k_c^{'}$ is chosen chosen according to the equation 3.8. The $I_D - V_G$ characteristics have been determined for each device by sweeping the gate voltage at low drain bias ($V_D = 50$ mV), and solving the DD coupled with the DG equations.

Figures 5.8(a) and 5.8(b) illustrate the obtained $I_D - V_G$ characteristics. The variation at threshold is evident in the curves, and it is caused by a change both in the number of dopants and in their placement in the channel region. On the whole V_{th} and SS appear much affected by RDF.



(a)



(b)

Figure 5.8: $I_D - V_G$ characteristics in log. (a) and linear scale (b) obtained from the simulation of 36 junctionless devices with a randomized doping profile ($N_D^{(des)} = 10^{20}$ cm^{-3}).

In order to have a better understanding of the nature of such pronounced variations the illustration of the channel iso-electron density surfaces, taken at increasing values of the gate voltage, is provided in fig. 5.9. The surfaces are obtained at $n = 5 \cdot 10^{19}$ cm^{-3}. Besides, we have included the Y-axis cross sections of the electron density, doping concentration and current density in the channel, obtained at $V_G \simeq V_{th}$.

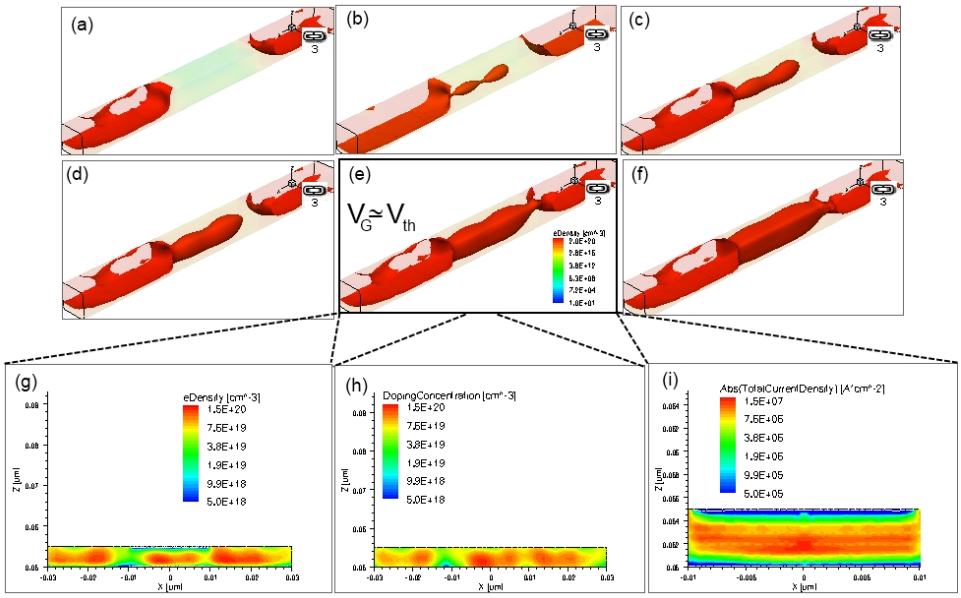


Figure 5.9: Electron density iso-surfaces taken at $n = 5 \cdot 10^{19}$ cm^{-3}, taken at increasing V_G values (fig. from (a) to (f)), and Y-axis cross sections of doping concentration, electron current densities (fig. from (g) to (i)).

While the current profile does not present visible effects of the randomized dopants, it is evident the similarity between the doping and the electron density profiles, showing that the latter is essentially given by the doping concentration in the NW. Hence, the larger the fluctuations on the doping profile, the larger the variations caused in the electron channel and thus in the overall characteristics.

Furthermore, observing the iso-surface plots, it may be noticed that the conduction channel formation appears much affected by the randomly placed dopants. From a comparison with fig. 5.4 we may conclude that the randomized impurities have caused quite clear inhomogeneity and pronounced asymmetry in the formation of the electron channel. This feature was not observed in the ideally uniform transistor. Hence, we may conclude that one of the main causes yielding important variations at threshold produced by RDF is the varying inhomogeneous and asymmetric channel formation caused by the doping profile.

A further important cause of statistical variations is represented by the change in the number of dopants. Indeed, the expected number of impurities in the overall nanowire volume V= $60 \times 5 \times 5$ nm^3 is $N_{tot} = 150$, for the specified doping concentration. This is different from the mean value extracted for the 36 devices with randomized doping, which is $\langle N_{tot} \rangle \simeq 147$ and the relating standard deviation is found to be $\sigma_{N_{tot}} \simeq 13$.

A different trend is observed in the small variation of the maximum drain current ranging from approximately $3.5 \cdot 10^{-6}$ to $5 \cdot 10^{-6}$ A. There may be more than one reason for this. Firstly, non-equilibrium carrier transport effects and the accurate description of scattering events extended over time, which may both cause variations in the maximum current, are not included in our treatment [19]. Secondly, the relatively large mean value of the number of dopant atoms in the channel yields to a reduction of the impact the dopant fluctuations have with respect to the maximum current drive.

In order to provide a deeper analysis of the impact of RDF we have extracted the distribution of the threshold voltage and of the parameter β, which is the multiplier of the gate-threshold voltage difference in the linear region equation 2.2, which is assumed to be the same of inversion mode devices, and where the mobility is also assumed the same in the three sides of the the nanowire:

$$\beta = \frac{C_{ox}\mu 3 W_{Si}}{L_G} \tag{5.2}$$

Hence, the threshold voltage has been extracted as the intersect in the voltage-axis of the line interpolating the characteristics. Subsequently, β has been determined using the following relation according to [1]:

$$\beta = \frac{I_D}{(V_G - V_{th})V_D - 1/2(1 + F_B)V_D^2} \tag{5.3}$$

where for small drain bias $(1 + F_B) \approx 1$, and we have taken the average of the points (I_D, V_G) used for the linear interpolation. Moreover, in order to obtain the frequency distribution in fig. 5.10 we have adopted the following criterion.

Firstly, we have sorted in increasing order the values p_i of the extracted parameters (i.e. V_{th} or β). Secondly, if the difference between the parameters' values p_i and p_j (with $i < j$ and $j = i + 1, i + 2, \ldots$) is less than a chosen tolerance $tol(p)$, namely

$$p_i - p_j < tol(p) \tag{5.4}$$

then, we determine the extracted parameter value p_k by taking the following average:

$$p_k = \frac{\sum_{i=k}^{i=j} p_i}{(j - k)}$$

and thus the frequency of each p_k is simply $f_k = j - k$. Obviously, if $p_i - p_{i+1} < tol(p)$ then $p_k = p_i$ and $f_k = 1$. Furthermore, we have chosen the tolerance to be below the relating standard deviation for each parameter.

The obtained frequency distributions for β and V_{th} are shown in fig. 5.10, where we have also included the first and second order statistical moments in the plots. The threshold voltage distribution exhibits a pronounced variation, with a definitely high relative error $\sigma_{V_{th}}/\langle V_{th}\rangle \approx 100\%$.

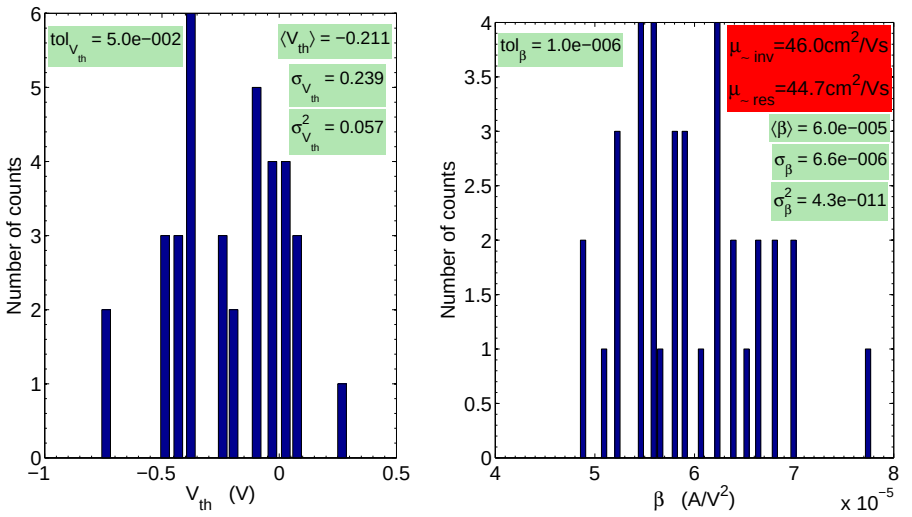


Figure 5.10: V_{th} and β frequency distribution extracted for the 36 junctionless devices. The mean value, the standard deviation, the variance and the chosen tolerance are shown in the plots, together with the mobility, extracted as described in the text.

Moreover, a large number of devices is observed to fall in two main ranges of V_{th}, namely $-0.5 \leq V_{th} \leq -0.4$ V $-0.1 \leq V_{th} \leq 0.1$ V. Indeed, there is a relatively extended region ($-0.5 \leq V_{th} \leq -0.1$ V) with a low number of counts. As such region is where the mean value $\langle V_{th}\rangle$ resides, such quantity is not a good indicator of the average threshold voltage. One possible reason for the presence of such a "void" could be that we have not gathered enough statistics.

The distribution of β appears slightly more uniformly distributed, however it can be noticed a low frequency area between two more dense regions. Nevertheless, there is a smaller relative error of $\sim 10\%$, meaning that the largest impact of RDF is on the threshold voltage shift.

Furthermore, the average mobility $\mu_{\sim inv}$ has been extracted from $\langle\beta\rangle$ according to the equation 5.2, where the subscript signifies that the model for β is derived according to the inversion mode device equation. In addition, we have extracted the mobility $\mu_{\sim res}$ inverting the gated resistor's equation 2.4.
The vicinity of the two numbers lets us suppose that a small error is committed if the model for inversion mode devices is applied to the the junctionless ones, although the physical phenomena describing the two types of devices is different. Even though the mobility is rather small in the junctionless transistor, it has a reasonable value, especially considering how much it is affected by ionized impurity scattering caused by the high doping level.

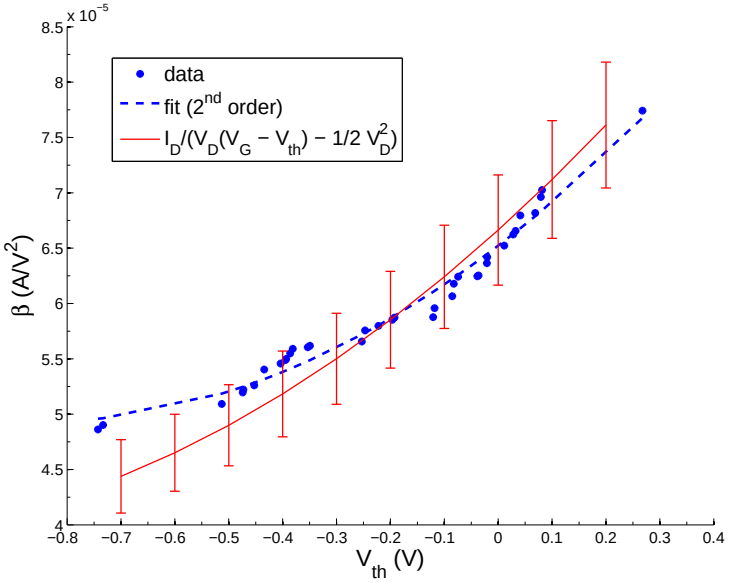


Figure 5.11: β VS V_{th} plot relating to the simulations of the 36 junctionless transistors. The points and the solid line represent the extracted data and the quadratic fit, respectively. The dashed line shows the 2^{nd} order Taylor expansion of eq. 5.3 which is superimposed to the data in the region far from the limits.

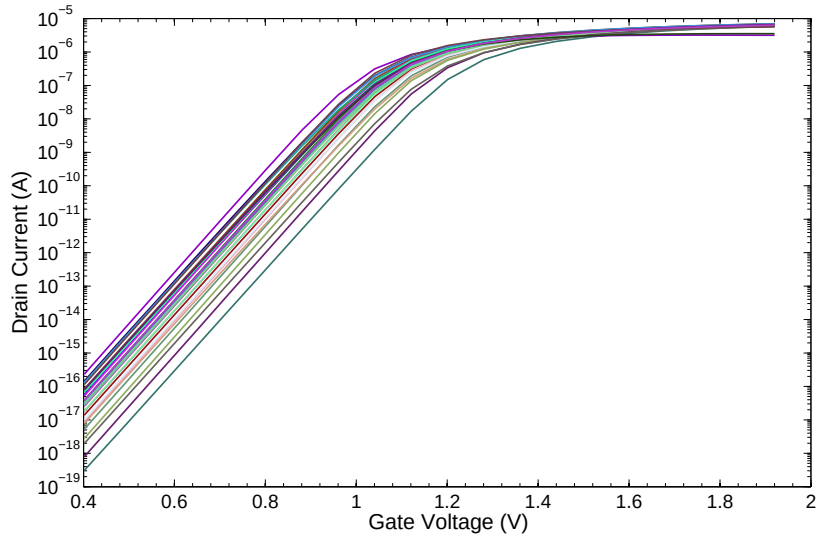
We finally illustrate the plot of β vs V_{th} in fig.5.11, in order to investigate the relation between the 2 quantities. The dots represent the extracted values, and the dashed line is a quadratic fit. The fitted data well resemble a parabola, showing that $\beta \sim V_{th}^2$, up to second order. Indeed, we also have plotted the second order expansion of eq. 5.3, as a comparison and it is quite superimposed to the fit, demonstrating that the parameter extraction is consistent with the analytical model used.

Such expansion is obtained at $V_{th} = -0.4V$ and at fixed V_G and I_D. We have taken $V_G = V_{G_{max}} = 1.35$ V and the mean maximum current I_D, which is averaged over the whole 36 devices[1]. Moreover, the error bars are obtained from the same Taylor expansion but this time using $\sigma_{I_{max}}$, instead of $\langle I_{max} \rangle$. Although the analytic curve almost superimposes with the fitted data, a divergence is observed at the points corresponding to two opposite V_{th} limits, which are also representing the tails of the distributions. At those limits our argument may not be valid any more.

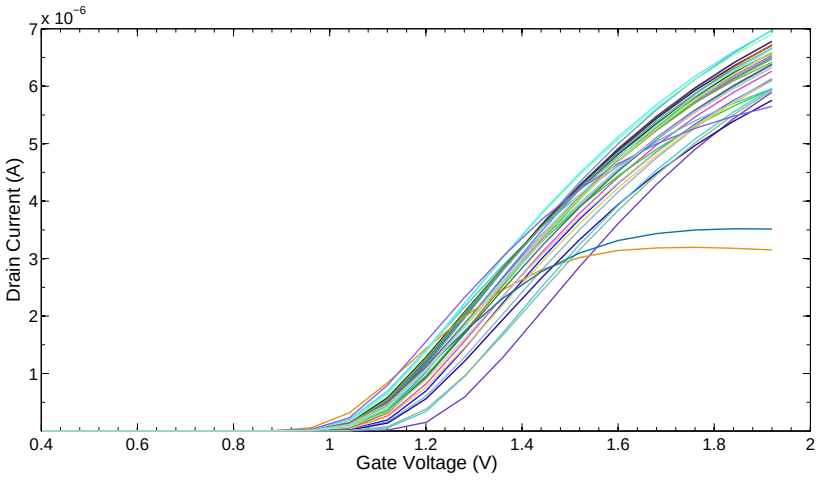
[1]The values have been chosen since the β extraction has been carried out in the last part of the characteristics.

5.3.1 RDF in inversion mode MuGFETs

For a deeper investigation of the impact of RDF we compare the study performed on the junctionless transistor with the one made on the inversion mode MuGFET. Table 5.3 illustrates the geometry and design doping levels for the inversion mode devices and the characteristics resulting from the simulations are shown in the figures 5.12(a) and 5.12(b).



(a)



(b)

Figure 5.12: $I_D - V_G$ characteristics in log. (a) and linear scale (b) obtained from the simulation of 36 inversion mode FETs with random doping profile.

Table 5.3: Geometry and design doping concentration of the simulated inversion mode MuGFETs.

Inversion mode MuGFET					
$N_{A_{(Ch.)}}$ (cm^{-3})	$N_{D_{(S/D)}}$ (cm^{-3})	$L_{G_{eff}}$ (nm)	T_{Si} (nm)	W_{Si}	t_{ox} (nm)
10^{18}	10^{20}	48	7	7	2

In order to include a significant number of dopants in the channel region of the inversion mode FET, we had to use a moderately high p-type doping, and we also chose to increase the overall dimensions with respect to the junctionless device for the same reason. Again, we run 36 simulations with a randomized doping profile obtained using two different screening factors $k_c^{'}$, for the channel and for the S/D regions, respectively. We had to increase the value of $k_c^{'}$ in the channel to twice the value predicted by the equation 3.8, owing to the small number of impurities, so that we could visualize a non uniform doping profile.

At first glance the impact of RDF appears smaller than what observed in the junctionless FETs. Especially at subthreshold the I-Vs are more uniformly distributed and they fall in a smaller voltage range, which lets suppose that the threshold voltage variations are less pronounced than in junctionless devices. On the other hand, variations on the maximum current drive are quite evident, as for instance 2 devices exhibit a significant drop in I_{max}, from $\sim 6 \cdot 10^{-6}$ A to $\sim 3 \cdot 10^{-6}$ A.

The accurate estimation of the impact of RDF on the threshold voltage and on β is provided by the frequency distributions of the two quantities, as shown in fig.5.13.

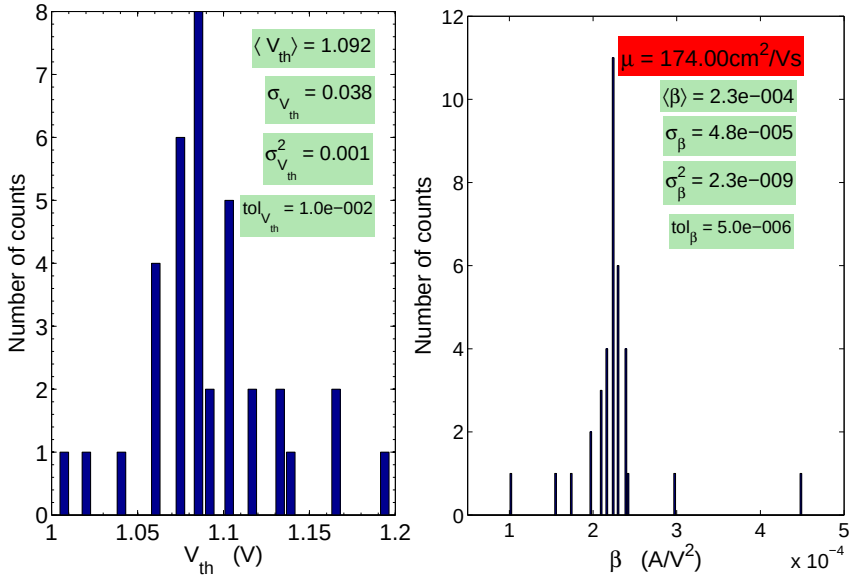


Figure 5.13: V_{th} and β frequency distribution extracted for the 36 inversion mode devices. The relevant quantiles and the chosen tolerance are shown in the plots.

The graphs confirm our first observation. Indeed, the values for V_{th} are more densely distributed around $\langle V_{th} \rangle$ Moreover, the relative standard deviation is only $\sigma_{V_{th}}/\langle V_{th} \rangle = 3.5\%$, much smaller than what we found for the junctionless FET.

However, the effects of RDFs are more evident in the β distribution. Although it resembles a normal distribution with a large peak in the mean value around 2.3 mA/V^2, it is evident the presence of the tails at the limits of the distribution. Moreover, the relative standard error in this case is larger than what observed in the study of the threshold voltage, namely $\sigma_\beta/\langle \beta \rangle = 20.8\%$. Finally, we have extracted the mobility from β according to eq.5.2, whose value is around 174 cm^2/Vs, approximately 4 times larger than the one of the junctionless device. Here the mobility is mostly affected by the electric field perpendicular to the gate oxide, but also by the impurities and also by high field saturation.

Again we present the plot of β VS V_{th} (fig. 5.14) to capture the relation between the parameters. In this case there is a less clear trend, and the parabolic trend we observed in fig. 5.11 is not apparent. Instead, we notice a large region of V_{th} at which β appears nearly constant. Then an opposite divergence towards large or small β values is observed at the limits of V_{th}. Again such limits represent the tails of the distribution, which were quite pronounced in β in this case.

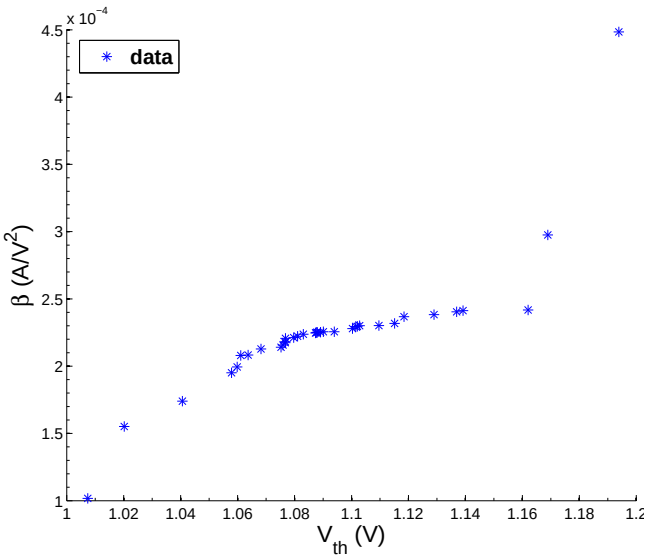


Figure 5.14: β VS V_{th} plot relating to the simulations of the 36 inversion mode FETs. β is approximately constant in the range $V_{th} = 1.06 - 1.16$ V, whereas it diverges to small (large) values at small (large) V_{th}.

5.3.2 Random Dopant Fluctuations Results Comparison

From our compared study of RDF we can conclude that the threshold voltage variation induced by the dopant fluctuations is larger in the junctionless transistor, whereas it is limited and probably within the fabrication's tolerance in the inversion mode MuGFET. However, the statistical variations of β, accounting here for the change in the mobility, can be considered within the tolerance limits in both types of devices.

Although the junctionless MuGFET exhibits remarkable performances, as highlighted in section 5.2, these are quite deteriorated by the presence of dopant fluctuations, and a comparison with the conventional MuGFET illustrates the superiority of the latter device with respect to RDF. If we had simulated the junctionless devices with larger dimensions, the overall results would have probably been better. Also, running simulations with design doping concentration in the whole range $N_D = 10^{19} - 10^{20}$ cm^{-3} would allow to find the optimum doping level for the specified dimension to limit RDF.

Nevertheless, we have to carefully understand how accurately our simulations may predict the two types of devices. Indeed, we have not developed any processing simulation including ion implantation and annealing steps. While neglecting processing simulation is not critical for the junctionless device, it may be for the inversion mode FET. The former device can be treated as being made of a uniformly doped nanowire, whose statistical variations in the doping profile are well accounted for by the Sano model. On the other hand, applying the same criterion to the inversion mode FET may yield to significant underestimations of the impact of RDF. Indeed, by carrying out simulations without processing steps in the inversion mode MuGFETs, we are implicitly assuming abrupt junctions, which is not the case. Hence, such simulations ought to be considered as accounting for RDF in the ideal inversion mode MuGFET.

Accordingly, more realistic results might be given by implementing processing and annealing steps to the inversion mode FETs' simulations. However, for a more rigorous testing they ought to be implemented in both types of devices.

Moreover, take into account LER has become of main importance in the study of the variability in inversion mode FETs, since the impact of LER is comparable to that of RDF at the dimensions we are concerned with [18]. On the other hand, neglecting it ought not to induce an error so large in the junctionless FETs, especially at threshold, since the oxide interface does not play a critical role in these devices.

This said, as our aim is the study of RDF on the junctionless transistor, we wish to provide a guideline to limit as much as possible the impact of the dopant fluctuations. Although RDF cannot be eliminated since ion implantation and thermal diffusion are techniques based on the random motion of the atoms and cannot get rid of the fluctuations over the number and positions of the atoms, some ways to limit their impact are possible. Besides fast annealing steps, which serve to reduce the thermal diffusion of the dopants, while still making them electrically active, advanced ion implantation techniques have been developed.

For instance, by using Single Ion Implantation [32] it may be possible to implant one atom at the time until the desired number is reached. Such technique is based on focusing an ion beam using a small aperture. Then, the number of implanted atoms is controlled by the detection of secondary electrons, emitted from the target. Although a very controlled and uniform doping profile may be produced with such technique, how it could be implemented in mass production is an unsolved issue.

In conclusion, the impact of RDF on the junctionless MuGFET has been tackled in this last section. Even though it has been shown that there are significant variations in the threshold voltage, more simulations with a different geometry and doping level might provide with better results for $\sigma_{V_{th}}$, which might be within the fabrication tolerance. Moreover, although the comparison with the inversion mode FET has demonstrated the superiority of such device with respect to RDF, the abrupt junctions assumption must have underestimated the impact of the dopant fluctuation in the devices.

Chapter 6

Conclusion

The performances of the Junctionless MuGFET have been deeply investigated in this work, by mean of different types of simulations implemented with the TCAD Sentaurus. Several packages have been developed in our study, starting from the one for the fabrication and meshing of the device structure, passing then to that used to randomize the doping profile for the investigation of RDF, and finally to the simulation of the device characteristics and transport properties.

Hence, a first 2-dimensional study has proven that the junctionless transistor may be a good alternative to conventional MOSFETs, for the shown remarkable characteristics and for its simpler fabrication. However, the development of a more accurate 3-D simulation has been necessary in order to include important physical properties such as the formation of the conduction channel in the middle of the nanowire. In the study of the uniformly doped 3-D MuGFET we have also tackled the impact of QEs in such device, and we have provided evidence of the fact that QEs ought to be less pronounced in the junctionless FETs than in the inversion mode ones.

Finally, we have focused on the impact that RDF may have on this type of devices. Many simulations with randomized doping profiles have been developed and the shown characteristics have proven that RDF may yield to significant threshold voltage variations, whereas the change over β is somewhat limited. A final comparison with the inversion mode FETs with larger dimensions has shown that the performances of this type of FETs are less deteriorated by the presence of RDF. However, such comparison ought to be placed in the context of larger dimensions and of ideally abrupt n-p junctions. Before claiming that the inversion mode MuGFETs outperform the junctionless transistor with respect to RDF, a more advanced study with different dimensions and doping concentration ought to be developed. Furthermore, for a more accurate simulation of the impact of RDF process simulations should be included both in the junctionless and in the inversion mode MuGFETs.

On the whole, the junctionless transistor has shown to be a promising alternative to the conventional MuGFETs, and our belief is that RDF ought to be limited, and comparable to inversion mode FETs with an optimized design and doping level. However, it stands to reason that as dimensions continue to shrink the impact of RDFs is supposed to increase, and the development of advanced ion implantation and annealing techniques is necessary to limit its effects. Hence, ultra-fast annealing and the future development of large-scale Single Ion Implantation may be considered in order to meet future scaling requirements.

Acknowledgements

The following thesis, while an individual work, benefited from the insights and support of many. First of all, I would like to thank my supervisor Dr. Gunnar Malm for providing me constant feedback, for his expert guidance and attention towards the development of the project. I am also most grateful to prof. Carl-Mikael Zetterling, who has given me the thrilling opportunity to work in the Device & Technology group at KTH, and from whose expertise and accurate observations I have benefited several times during some meetings. Moreover, during some discussions on my possible future employment he has encouraged me to apply for a PhD (not another master), and this has proven to be most successful. I am thankful for that too. Special thanks go also to the other professors and PhD students in the group with whom I have had a great time, and who have helped me for the development of the project.

Finally, I wish to thank my parents and my friends from Italy who have come all the way to Sweden for me, and who have given me all the support and affection I might have desired. Even though my experience in KTH has for the moment come to an end, I deeply wish that some collaboration might arise in the future, as I will always leave a part of me in Stockholm and in Electrum, here at KTH.

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