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Wafer-level integration of NiTi shape memory alloy on silicon using Au–Si eutectic bonding

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Abstract

This paper reports on the wafer level integration of NiTi shape memory alloy (SMA) sheets with silicon substrates through Au–Si eutectic bonding. Different bond parameters, such as Au layer thicknesses and substrate surface treatments were evaluated. The amount of gold in the bond interface is the most important parameter to achieve a high bond yield; the amount can be determined by the barrier layers between the Au and Si or by the amount of Au deposition. Deposition of a gold layer of more than 1 μm thickness before bonding gives the most promising results. Through patterning of the SMA sheet and by limiting bonding to small areas, stresses created by the thermal mismatch between Si and NiTi are reduced. With a gold layer of 1 μm thickness and bond areas between 200×200 and $800 \times 800 \mu\text{m}^2$ a high bond strength and a yield above 90% is demonstrated.

(Some figures may appear in colour only in the online journal)

1. Introduction

The work output per volume of shape memory alloy (SMA) microactuators exceeds that of other actuation principles such as electrostatic, piezoelectric and magnetic actuation [1]. SMAs are therefore very interesting to use in microelectromechanical systems (MEMS). The high work density is well suited for the creation of large deflection actuators that can exert high forces. SMAs exhibit the shape memory effect (SME), which is the ability of a material to remember its initial shape when deformed. At low temperatures, the SMA material is in the cold martensitic phase, where the SMA is easily deformable and stays deformed also after the deforming stress has been removed. Upon heating the material transforms to the hot austenitic phase and the initial shape is recovered.

There are several materials demonstrating the shape memory effect but the most relevant material to use commercially is an equiatomic composition of Nickel and Titanium (NiTi) [2, 3]. Compared to other SMAs, NiTi alloys exhibit better mechanical properties, higher shape

memory strains, higher resistivity for electrical actuation and superior corrosion resistance. In addition, the transformation temperature of the NiTi alloy can be selected over a wide temperature range, typically -100 to 100°C , only by changing the Ni over Ti ratio of the alloy [4].

Despite its material advantages, the successful use of NiTi in MEMS applications is limited mainly since proper methods for the wafer-scale and batch compatible manufacturing and integration are lacking. Traditionally there are two main approaches for the integration of SMA materials with MEMS devices.

The first approach is to fabricate the SMA element and the MEMS components separately, and then assemble them by a pick and place approach on a per device level [5]. The main advantage for this approach is the use of bulk SMA, which is commercially available in a wide thickness range and therefore allows for adjustable mechanical robustness and reduced material cost. However the required per device assembly is not batch compatible and results in high manufacturing costs.

The second integration approach is based on sputter deposition or evaporation of thin SMA films directly onto

the MEMS structure [1]. This allows for batch compatible processing. High annealing temperatures are however needed after deposition and the achievable layer thickness is limited. A recent report has demonstrated SMA film deposition up to 30 μm [6]. However, reliable fabrication of thick NiTi thin films with reproducible transformation temperatures and strains is still difficult to achieve with these methods since precise compositional control is needed.

Methods for wafer-scale and cost-efficient batch compatible processing with the use of robust bulk SMA material, and the ability to avoid the complicated SMA deposition processes are therefore sought. Wafer-scale integration of bulk SMA also allows the separation of the SMA machining and the silicon machining, thus avoiding the risk of damaging the silicon structures with the harsh techniques needed for the machining of SMA, e.g. HF:HNO₃ etching. In addition, with the use of bulk SMA material there is also no need for high temperature annealing of the SMA.

Recently, methods for the wafer-level integration of bulk NiTi wires and sheets with silicon substrates have been reported. Wire integration approaches have been demonstrated using adhesive bonding [7], electroplating [8] and wire bonding [9]. There are only a few reports on bulk SMA sheet integration. One approach is the wafer-scale patterning of an SMA sheet and its selective transfer by laser ablation onto polymer microvalves [10]. However, the cold state SMA reset was provided by a spacer, which still requires pick and place assembly. Another study integrates SMA sheets onto plastic substrates using microriveting by electroplating [11]. However the riveting occupies a large area and has not been demonstrated in full wafer scale yet.

A full wafer-level integrating process of NiTi sheets onto silicon microstructures has been presented recently [12]. In that work, a wafer-sized SMA sheet was first patterned and subsequently bonded onto a microstructured silicon wafer using BCB (benzocyclobutene). The adhesive was stamped onto the silicon structure before bonding. The stamping process is complicated and the resulting bonding layer thickness is difficult to control. During the bonding, large reflow of the adhesive occurs, which also potentially results in unwanted bonding of moving parts in the MEMS structure. In addition, the long-term stability of the polymer bond is potentially limited during high strain cycling actuation and has so far not been investigated.

To overcome the limitations of the previous methods, this paper presents an investigation of wafer level integration of bulk NiTi sheets with silicon wafers using Au–Si eutectic bonding. Gold and silicon (18.6 at% silicon) form a liquid above the eutectic point of 363 °C. The Au–Si eutectic can thus be used as an intermediate bonding layer between two substrates [13]. However, large thermal stresses occur when bonding materials with different thermal expansions. Therefore, previous eutectic bonding has been limited to Si–Si and Si–glass bonding. Gold–silicon eutectic bonding of SMA sheets to silicon has previously been used for the creation of high performance microvalves [14]. However, the Au–Si eutectic bonding process used had low yield.

This paper investigates how to achieve high yield Au–Si eutectic bonding of SMA sheets and which parameters

Figure 1. Schematic of the bonding stack used before bonding (left) and the silicon/gold diffusion process forming the eutectic during bonding (right). An optional barrier/adhesion layer is here shown that will be investigated in this paper.

influence the bonding quality. To the author’s knowledge, this paper presents the first wafer-level eutectic bonding scheme overcoming problems related to large thermal stress and allowing for the wafer-level bonding of thermally mismatched metal sheets and silicon substrates.

As the starting point for this research, Au–Si eutectic bonding parameters typically used for silicon-to-silicon wafer bonding are used. Simulations were performed to investigate the effect of thermal stress in the material after eutectic SMA-to-silicon bonding, to study crack formation in bonded structures and to derive design parameters for increased bond reliability. An extensive experimental investigation by bonding test samples is also presented. The combined results of the simulation and experimental work are used to outline which parameters affect the bond quality.

2. Design and process parameters

Because the Au–Si eutectic formation in SMA-to-silicon bonding is similar to that in silicon-to-silicon bonding, typical parameter values used for eutectic bonding for silicon-silicon bonding are used as the starting point in this study.

When performing gold–silicon eutectic bonding, the bonding temperature, gold thickness and the silicon surface are key parameters influencing the reliability of the bond. Eutectic bonding is based on the diffusion of silicon and gold as illustrated in figure 1.

A high bonding temperature promotes the diffusion process and thus increases the thickness of the resulting eutectic bonding layer. However, a too high bonding temperature can lead to significant diffusion of gold into the silicon, which can result in a less reliable bond and also potentially degrade the function of the silicon device. A previous report on Si–Si eutectic bonding indicates that the maximum bond strength is achieved at 400 °C and that at higher temperatures the bond strength decreases [15]. The same report found that the gold thickness of 1 μm resulted in the highest bond strength and maximum bond yield.

To achieve a successful eutectic bond the surface preparation before bonding is very important. The presence of oxide on the silicon substrate can both affect the bond yield and the bond strength of a eutectic bond due to poor adhesion or a limited eutectic reaction. The purpose of the surface preparation is to increase the adhesion of gold on the silicon substrate either by the removal of the native silicon

Table 1. Numerical values of the coefficient of thermal expansion, Young's Modulus and yield strength for Si and SMA [18–20].

Material	Coefficient of thermal expansion (α) ($^{\circ}\text{C}^{-1}$)	Young's modulus (Y) (GPa)	Yield strength
Si	2.3×10^{-6}	190	7 GPa
SMA (Austenite)	11×10^{-6}	75	560 MPa
SMA (Martensite)	6.6×10^{-6}	28	100 MPa

oxide or by an adhesion layer deposition [16]. HF treatment is most frequently used for the removal of the native oxide layer on the silicon. For adhesion, materials that adhere well to both an oxidized silicon wafer and gold can be used, such as Ti and Cr [16].

The diffusion of Au and Si can be controlled by different barrier layers. To limit Au diffusion into the silicon it has been demonstrated that a silicon dioxide layer serves the purpose best, whereas Ni and Pt barriers have limited barrier capability [17].

A large difference in the coefficient of thermal expansion of NiTi and silicon exists, which is displayed in table 1. This results in large stress build up during cooling after bonding, with a high risk of destruction of the bond. Bonding of full wafer sized sheets is therefore not feasible. To reduce the stress, the NiTi sheet must first be patterned and the different shapes to be bonded are connected with stress releasing flexures as illustrated in figure 8 [12]. In addition, by patterning the SMA sheet prior to bonding the risk of damaging the target substrate by aggressive SMA etchants is eliminated.

3. Simulations

The main difference between SMA-silicon bonding, as compared to silicon-silicon bonding, is the large difference in thermal expansion between the two materials. To achieve a good and reliable bond, it is therefore important to understand the stress profile after bonding and how cracks can form. To investigate this, 2D simulations were performed in Comsol Multiphysics 3.4. The largest stress in the bond interface is expected to occur during the cooling of the bond sequence and just before the SMA transforms from the austenitic to martensitic phase. The simulation therefore studied the cooling of a wafer stack from 370°C , just above the Au-Si eutectic temperature, to 50°C , the assumed temperature for the SMA transformation to martensite where the stresses decrease. A $30\text{ }\mu\text{m}$ thick SMA piece fixed on top of a $300\text{ }\mu\text{m}$ thick silicon wafer at 370°C was used as a starting condition. Both materials were modeled as isotropic with the parameters from table 1. The simulated length of the SMA piece was varied from 50 to $2000\text{ }\mu\text{m}$ to study the importance of the bond area size for the stress level. The point of maximum stress occurs in the silicon just at the edge of the SMA. Figure 2 plots the von Mises stress in the silicon at $1\text{ }\mu\text{m}$ underneath the bond surface as a function of the SMA length as an indication for the stress in the bond interface.

The maximum stress as a function of SMA length is plotted in figure 3, clearly demonstrating that for SMA lengths

Figure 2. Simulated von Mises stress at the bond interface after cooling from 370 to 50°C . The position 0 (x -axis) indicates the point where the SMA starts to be in contact with the silicon. At the bottom the 2D cross sectional stress levels are illustrated schematically. The curves display the magnitude of the stress at a position $1\text{ }\mu\text{m}$ down in the silicon (represented by the red line in the schematic) for different total lengths of the bonded SMA (50 – $2000\text{ }\mu\text{m}$ long). The maximum stress, $1\text{ }\mu\text{m}$ down from the bond interface, increases with increasing length of the SMA piece.

Figure 3. The maximum stress as a function of the length of the bonded SMA piece.

below $200\text{ }\mu\text{m}$, a decrease in bond area decreases the maximum stress levels. However, above $200\text{ }\mu\text{m}$ the maximum stress is almost constant.

The stress distribution and possible crack formations were further analyzed by first removing a part of the silicon at the point of maximum stress (figure 4). The removal of material simulates a void or a start of a crack at a point in the bond interface. In this void, two regions of high stress can thereafter be observed; one directly inside the bond interface, i.e. in the silicon just below the SMA, and one downward into the silicon at an angle of around 40° . It can also be observed that the stresses into the silicon are lower at larger void diameters. If the stresses are too high it is likely that a crack will start propagating in one of these directions, either

Figure 4. Simulation of a void at the SMA edge and the von Mises stresses for void size diameter of (a) 1 μm , (b) 2 μm , (c) 4 μm . The highest stresses are not only precisely at the bond interface but also into the silicon at an angle of around 40°C. The stresses in the silicon decrease with increasing void diameter.

Figure 5. Simulation of crack propagation into the silicon substrate. If a crack would start forming downward into the bulk at a void (as in the direction of maximum stress in figure 4(a)), the crack would continue propagating downward (b) but after a while starts changing direction (c). Finally the crack will propagate parallel to the SMA at a depth of more than 30 μm .

inside the bond interface or into the silicon bulk. The point of maximum stress was used to determine the most likely point of failure and the propagation direction of a potential crack. The crack propagation into the silicon was therefore simulated by removing material at the point of maximum stress as illustrated in figure 5. First a 1 μm wide and 3 μm long bar is removed in the direction of maximum stress (figure 5(a)) thereafter a new stress simulation is performed. The maximum stress from this simulation is still in the same direction and first, by removing an additional 20 μm of material the direction of maximum

stress changes (figure 5(b)). By continuing to remove material in this new direction (figure 5(c)) the highest stress further changes direction to being parallel to the SMA (figure 5(d)). The crack continues to propagate underneath the SMA at a depth of more than 30 μm into the silicon (figure 6(a)). The crack can continue to propagate in this way until it starts reaching the other end of the SMA, where the crack starts moving upward (figure 6(b)).

This indicates that if a void exists at the point of maximum stress and a crack starts to form, there is a high likelihood the crack will continue to propagate deep into the silicon bulk with the result of transferring silicon onto the SMA.

4. Fabrication

To study the effect of bond parameters on the bond yield, an extensive parameter study was performed by fabricating a multitude of test samples.

Two different process runs (A and B) were performed to characterize the Au–Si eutectic bonding of SMA sheets to silicon.

In the first process run, A, aiming to investigate the influence of the silicon surface preparation and the gold layer thickness on the bonding yield, NiTi cantilevers were bonded to silicon wafers. The fabrication starts with the separate preparation of the NiTi sheets and the silicon wafer substrates as shown in figure 7. Since harsh machining techniques are needed for patterning NiTi sheets, all SMA structuring is preferably performed prior to the bonding of the SMA to the silicon.

Figure 6. Von Mises stresses in the silicon and SMA after a simulation of crack propagation (a) when the crack has propagated halfway underneath the SMA and (b) when the crack almost has reached the other side of the SMA. (Note: In (a) the maximum stress is still around 3 GPa, at the end of the crack, but is not illustrated in the color range of the image.)

Figure 7. Process flow for the test structures in process run A. In process run B the patterning (steps (b–e)) was replaced by dicing the SMA into different sizes.

Each SMA machining starts with a square $10 \times 10 \text{ cm}^2$ cold rolled NiTi sheet (Ti 44.62/Ni 55.37 wt.%, $A_f \approx 46^\circ\text{C}$), commercially available from Johnson Matthey. To remove contaminations, the sheet is first cleaned in acetone, isopropanol and water. After cleaning and drying, any deformations of the sheet are straightened by briefly heating the sheet above the transformation temperature on a hotplate.

The sheet is thereafter placed in a sputter machine and a TiW adhesion layer and an Au layer are deposited onto the sheet (figure 7(a)).

For easier handling during the subsequent fabrication steps, the SMA sheet is thereafter attached to a carrier wafer (not illustrated in the process flow). Due to the aggressive nature of the SMA etchant, an oxidized silicon or glass wafer are suitable sheet carrier wafers. The carrier attachment is performed by gently attaching the sticky side of a blue wafer dicing tape (Nito Denko) onto the backside of the SMA, i.e. the side without Au on. It is important to avoid bending and stretching of the SMA during the attachment, to achieve good lithography on the sheet afterward. It is also important to remove all air bubbles between the blue tape and the SMA since the bubbles can cause SMA features to be destroyed during etching. The SMA with blue tape is thereafter placed

Figure 8. Schematic of a group of SMA cantilevers used in the process run A. To reduce the thermal stress during bonding the SMA is patterned and all structures are connected via stress releasing flexures. Four different bond area geometries ($a = 0.64 \text{ mm}^2$, $b = 0.16 \text{ mm}^2$, $c = 0.04 \text{ mm}^2$, and $d = 0.0144 \text{ mm}^2$) were tested.

on the carrier wafer with the blue tape side toward the carrier. The stack is heated to 90°C on a hotplate and gently pressed together to make the blue tape backside stick to the carrier wafer, as described in previous work [12]. Excess blue tape and SMA sheet material are subsequently cut away with a scissor to match the shape of the carrier wafer.

A resist layer ($1.5 \mu\text{m}$ SPR 700-1.2) is spun onto the Au side of the stack. Lithography is performed to define 2.5 mm long and 1 mm wide SMA cantilever structures that are interconnected with $200 \mu\text{m}$ wide flexures as illustrated in figure 8.

The gold layer is patterned using an iodine based wet etchant (KI and I₂) to define a hardmask for the SMA etching (figure 7(b)). To avoid the SMA delaminating from its carrier, the resist is stripped by spraying acetone and isopropanol toward the exposed SMA side only, followed by rinsing the stack in water.

The SMA with the Au hardmask is again spin coated with the same positive photoresist ($1.5 \mu\text{m}$ SPR 700-1.2) to define the bond pad area on each cantilever (figure 7(c)). Since the SMA sheet is quite rough, (more than $1 \mu\text{m}$ from the highest to lowest point), the contrast of the pattern is quite low, making alignment challenging. Four different bond area geometries were tested as illustrated in figure 8. One large bond area with size $800 \times 800 \mu\text{m}^2$ (a), one large bond area divided into 10×10 small areas each of size $40 \times 40 \mu\text{m}^2$ (b), one small bond area of size $200 \times 200 \mu\text{m}^2$ (c) and one small bond area divided into 3×3 small areas each of size $40 \times 40 \mu\text{m}^2$ (d).

Thereafter, the SMA sheet is etched in a mixture of HNO₃ and HF (30% and 5%) using the Au hardmask [12]. Achieving a uniform etch is difficult. Therefore it is important to stir the solution slightly during etching. Small etch features have a risk of not being completely etched through and therefore some overetching is needed to define these. An undercut: etch depth ratio of approximately 1:1 is achieved. The etching is fast, around $10 \mu\text{m min}^{-1}$. The wafer is removed from the etchant when the blue tape is visible underneath the SMA. It is also important to perform the etching in good ventilation,

Table 2. Bond yield after dicing and releasing the cantilevers for every bond area type (a, b, c, d) together with the average yield for the four bond areas and also the shear strength data for the samples. (For the nondestructive shear tests, the highest value recorded is instead reported in *italic*.)

Sample			Si-1		Si-2		Si-3		Si-4		Si-5		Si-6		Si-7	
Oxide removal			Sputter etch		Sputter etch		HF dip		HF dip		None		None		HF dip	
Re-oxidation time			0 ^a		0 ^a		10 min ^b		3 h ^b		Native oxide		Native oxide		10 min ^b	
Adhesive layer/thickness (nm)			0		0		0		0		0		TiW/20		0	
Gold thickness (nm)			1000		350		350		350		350		350		0	
Bond yield %	SMA-1 (30 μm thick with 350 nm Au)	a	100	100	100	50	100	69	100	75	100	56	100	81	75	38
		b	100		50		75		100		75		75		25	
		c	100		25		100		75		50		100		25	
		d	100		25		0		25		0		50		25	
	SMA-2 (50 μm thick with 1000 nm Au)	a	100	95	100	90	100	100	100	90	100	95	100	95	80	35
		b	100		80		100		100		100		80		20	
		c	100		100		100		80		100		100		40	
		d	80		80		100		80		80		100		0	
Bond strength(MPa)	SMA-1 (30 μm thick with 350 nm Au)	a	>7.7		>6.6		>6.4		>7.7		>5.9		>7.7		>5.4	
		b	>21		9.3		22		14		16		>31		>9.0	
		c	120		43		33		14		0		>53		10	
		d	100		64		0		1.0		0					
	SMA-2 (50 μm thick with 1000 nm Au)	a	>7.7		1.2		>7.7				6.1		>5.4		>4.0	
		b	30		10		>17		17		>31		>22			
		c			0		110		53		74		22		18	
		d	140		30		27						>90		0	

^a *In situ* sputter deposition.

^b In ambient air.

Figure 9. Silicon surfaces after the eutectic bonding process for non SMA regions. The calculated Au content is displayed for every surface. (a) Si-1, 90% Au. (b) Si-2, 77% Au. (c) Si-3, 97% Au. (d) Si-4, 94% Au. (e) Si-5, 67% Au. (f) Si-6, 97% Au.

since toxic fumes are formed. More details on the effect of different etch recipes can be found in [12]. In contrast to previous work, where resist directly on the SMA delaminated during etching [12], the resist (1.5 μm SPR 700-1.2) on the Au is not perceptibly affected by the etch mixture. The resist mask is then used to pattern the Au layer/hardmask in iodine Au etchant to form the bond pad areas (figure 7(e)). Finally, the stack is put in acetone to strip the photoresist and to release the SMA sheet from the carrier substrate. Two SMA sheets were prepared in this way, one 30 μm thick sheet with a 350 nm thick Au layer and one 50 μm thick SMA with 1000 nm Au, as listed in table 2.

In parallel, seven different silicon substrates were prepared, hereafter referred to as Si-1 to Si-7. The substrates consisted of 550 μm thick (100) 4 inch silicon wafers. Each silicon wafer was processed differently to investigate the effect of the gold thickness, oxide removal and adhesion layer. The seven different substrates are listed in table 2. Before processing, the Si wafers were cleaned in Piranha ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$, 3:1) to remove the organic and metallic contaminations from the surface of the wafers. Two of the silicon wafers were sputter etched to remove the surface oxide followed by *in situ* sputter deposition of a gold layer at different thicknesses (Si-1, Si-2 table 2). The *in situ* sputter deposition of gold on sputter etched Si-surfaces prevents the re-growth of a native oxide layer on the silicon surface. Two silicon wafers were HF treated for the removal of the oxide layer and thereafter left for 10 min and 3 h respectively in ambient air for the re-oxidation before the sputter deposition of gold (Si-3 and Si-4). For one wafer, a TiW adhesion layer was sputter deposited directly onto the native oxide of a silicon wafer and before Au deposition (Si-6). For comparison a silicon wafer was processed where the gold layer was sputter deposited directly on the silicon wafer with native oxide and with no

adhesion layer (Si-5). One silicon wafer was dipped in HF to remove the native oxide just before the bonding without any deposition of gold on the silicon wafer (Si-7).

The two patterned SMA sheets were cut into groups, with each group consisting of four SMA cantilevers, each with one of the four bond area sizes as illustrated in figure 8. Four groups of cantilevers from SMA-1 and five groups of cantilevers from SMA-2 were placed on each silicon wafer and heated to 100 $^\circ\text{C}$, to flatten the SMA cantilevers through shape recovery. A glass wafer was placed on top of the cantilevers for protection against the bond chuck. Then the wafers were bonded in vacuum with an input tool force of 1 kN (the average bond pressure on a bond area is estimated to be 10 bar) and at 400 $^\circ\text{C}$ over a period of 10 min. The experiments were performed in a commercially available bonder (SUSS MicroTec CB8 Chamber bonder).

After bonding, the glass cover was removed and a resist layer was spun onto the wafer to stabilize the cantilevers during dicing and to protect them from saw dust. The wafer was then diced, cutting the SMA flexures and hence separating the individual cantilevers. Finally the protective resist layer was removed in acetone.

The second fabrication run, B, was performed to investigate the relation between bond area size and yield. The same NiTi sheets as in process run A were used, but instead of patterning them as in figure 7(b-e), the SMA sheets with gold were diced into squares with side lengths of 1, 2, 4 and 8 mm respectively. For easier handling and to protect against saw dust, the NiTi sheets were placed in between two layers of blue tape during dicing. All diced NiTi squares were thereafter bonded to a silicon wafer with the same parameters as in Si-1 in table 2 and with an input tool force of 1 kN and at 400 $^\circ\text{C}$ over a period of 10 min.

Figure 10. Average bond yield as a function of total gold thickness for all process run A samples.

Figure 11. Bond yield of SMA-1 for the four different oxidation times of Si-2, Si-3, Si-4 and Si-5.

5. Evaluation

The bonded cantilevers were characterized by measuring the bond yield after dicing and the bond strength by shear testing. The bond interface was further studied in an SEM (Scanning Electron Microscope).

Integrated SMA cantilevers have been used successfully as actuators in gas valves, demonstrating that the shape memory effect still exists in the cantilevers after the Au–Si eutectic bonding procedure [14]. Small changes of the transformation temperatures occur after heat treatment of NiTi at 400 °C, as has been studied previously by differential scanning calorimetry measurements [21]. However, the changes in the thermal properties are highly dependent on the material's previous history and the applied stresses during the thermal cycling after the integration [21]. For designing an integrated device, the lifetime of the material in its specific application needs to be taken into account for reliable data. Therefore, only the heterogeneous integration process and bonding yield were studied in detail in this paper, and not the actuation cycling.

5.1. Bond yield

Firstly, the influence of the surface treatment and the gold layer thickness on the yield was evaluated. After the wafer had been diced, the number of SMA cantilevers still bonded

Figure 12. Bond yield of SMA-1 as a function of the gold content at the surface from the SEM pictures in figure 9.

Figure 13. Average bond yield and the data points (table 2) for the four different bond areas (a, b, c, d) for SMA-1 and SMA-2 respectively.

Figure 14. Schematic of the shear testing setup from the side and the top.

to the silicon wafer was counted. The result is presented in table 2 as the bond yield, i.e. the number of cantilevers still bonded relative to the total number of cantilevers for each bond parameter.

A first observation is that a thicker gold layer results in a higher yield. The average bond yield for the samples as a function of the total gold layer thickness, i.e. the sum of the gold thickness on the SMA and the silicon before bonding, is

Figure 15. Average shear strength (not including the samples with the largest bond area). The nominal bond area, i.e. the designed bond area, has been used in the calculations.

Figure 16. Relation between the yield (table 2) and the shear strength (figure 15).

plotted in figure 10. The SMA with a 1000 nm thick gold layer (SMA-2) had excellent yield percentage for all different types of bonded substrates except for the one without gold on the silicon (Si-7). The combination of an SMA sheet with only 350 nm Au but bonded to a thick gold layer on the substrate, also resulted in a high yield.

The yield for the rest of the samples of the SMA with a 350 nm thick gold layer (SMA-1) is dependent on the surface treatment of the substrate. As the gold layer is thinner as compared to SMA-2, other factors have influenced the yield. For a 350 nm thin layer of gold on both the silicon and the SMA (SMA-1 with Si-2, Si-3, Si-4, Si-5), the yield is related to the oxide thickness as displayed in figure 11. With an increased oxide thickness the yield increases and with a maximum of 75% at 3 h reoxidation time in atmospheric conditions. However, for the wafer with a fully developed native oxide, which should correspond to the thickest oxide layer, the yield is lower.

On sample Si-6 a significant increase in bond yield can be observed as compared to sample Si-5. By having a TiW layer

between the oxide and the gold, the yield increases to 81% whereas without TiW, the yield is 56%.

The relation of the gold content at the wafer surface to the bond yield was then studied. SEM pictures of the silicon surface for every wafer after the eutectic reaction are displayed in figure 9. Variations of the eutectic pattern over the wafers exist. Especially for the wafer with native oxide (Si-5), both regions with eutectic reaction and without eutectic reaction exist. Figure 9(e) displays a reacted region. From these SEM pictures, the relative Au content at the surface has been evaluated by pixel counting of gold (bright pixels) relative to the total number of pixels. The relation between the Au content at the surface after the eutectic reaction is plotted versus the yield of SMA-1 in figure 12.

The size of the bond area also affects the yield as plotted in figure 13. A larger bond area results in a higher yield. For SMA-1, the size of the bond area has a larger influence on the yield than for SMA-2.

5.2. Bond strength

The bond strength of the samples was then investigated through shear testing. The test was performed using a standard commercially available Dage PC 2004 shear stress tester, commonly used for wire bonding testing. This is a contact tool, with a needle applying a force at the edge of a bonded cantilever at an angle of 90° as illustrated in figure 14. The force is ramped from zero while the needle is at the edge of the cantilever. The bond strength is expressed as the force needed to shear the bonded surfaces apart divided by the bonded area. In order to avoid displacement during the test, all the diced chips were glued on a plane Si wafer and the handle wafer was then mounted on the sample holder. The resulting bond strength (destructive shear force/bond area) is listed in table 2 for the measured samples. For seven samples, measurements were not conducted, since no sample was left to shear test, due

Figure 17. SEM images of destructed bond interfaces after shear tests with (a) only Au on Si and (b) native oxide and TiW layer before Au. The SMA cantilever is displayed on the left side and the corresponding silicon substrate on the right side. (a) Si-1 (sputter etch and 1 μm Au). (b) Si-6 (native oxide and TiW layer before Au)

Figure 18. EDX mapping of the Si and Au in the bond interface and indication of the average Au diffusion depth and diffusion profile in (a) Si-1 with no diffusion barrier. (b) Si-6 with a native oxide layer and a TiW layer.

to low yield or other investigations that had been conducted on them.

For the samples with the largest bond area (a, 0.64 mm²), the tool limit of 5000 mN was reached for 11 out of 13 samples tested. For these samples the highest recorded nondestructive bond strength is instead shown as a lower limit. Most of the samples with smaller bond areas were possible to shear off, but for eight samples the temporary adhesive to fix the sample

was instead the point of failure and the highest value recorded is listed in the table. The average shear strength is plotted in figure 15 (not including bond area a samples where the tool limit was reached). Si-1 displays the highest bond strength and Si-7, with no Au on the surface, displays the lowest. The large variation between the measured values can be related to the shear tool probe not being precisely aligned toward the bond area, movement of the sample on the tester stage during

testing, stiction between the SMA and the silicon and also the real bonded area not being the same as the patterned gold bond area. The uncertainty in total bonded area is largest on the samples with small and divided bond areas, where it is possible not all of the fabricated bond areas are bonded or/and stiction between the SMA and wafer exists between and around the real bond areas. The relation between the bond yield and the average bond strength for all samples is plotted in figure 16, demonstrating a correlation between an increased yield and an increased bond strength.

The shear testing experiments showed that the point of bond breakage is most of the time inside the silicon bulk. Typically, a large piece of silicon, roughly 100 μm thick is removed and transferred to the SMA. The crack is defined around the bond area. Figure 17(a) shows a bond area after the SMA cantilever has been sheared off. For the samples with the TiW adhesion layer (Si-6), the point of failure is, however, not inside the silicon but in the bond interface as shown in figure 17(b).

5.3. Cross sectional analysis

The bond was further studied by dicing the silicon close to the SMA cantilever, embedding the sample in polymer and polishing it until a cross sectional view of the bond interface can be seen. The bond was analyzed by SEM (Scanning Electron Microscope) and EDX (Energy-dispersive x-ray spectroscopy). The difference between samples with a TiW adhesion layer on an oxide layer (Si-6) relative to nonoxide samples (Si-1) were studied and are shown in figure 18. For the sample where there is no oxide on the silicon (Si-1), the silicon surface has been dissolved and a resulting wavy eutectic surface can be seen. In the case of the sample with silicon dioxide and a TiW layer, the silicon surface remains planar. The diffusion depth of the Au into the silicon was further measured by EDX analysis. For Si-1 the depth is on average 1 μm from the Au rich interface and for Si-6 the depth is 0.2 μm . It can also be noted that for the sample with a TiW layer, there exists small gold pits where the TiW and oxide layer has been broken on the surface and gold has diffused down into the silicon [22]. A good illustration of a hole in the diffusion barrier can be seen in figure 19. Here the surface barrier has been broken and all gold at the surface has diffused down into the silicon and at the same time silicon has diffused upward.

Even though the native oxide layer and TiW layer decreased the Au diffusion into the silicon, a eutectic is still formed. The eutectic formation can be explained by silicon diffusing through the barrier, or that holes in the diffusion barrier exist. Holes in the diffusion barrier can be caused by high bond forces or by Ti dissolving part of the native oxide [23].

The bond interface for seven samples was investigated for Si-1, Si-4 and Si-6 listed in table 3. In some of the samples a crack was observed either at the bond interface or in the silicon, as shown in figure 20. No correlation was seen between the existence of a crack and the bond area size or the silicon wafer type.

(a)

(b)

Figure 19. Schematic (a) and SEM picture (b) of a hole in the diffusion barrier with the result of Au flowing down into the pit and Si flowing upward, similar to a sink for the gold on the surface.

Figure 20. Cross sectional SEM picture of a crack in the silicon underneath the SMA.

Table 3. Detected cracks at the bond interface from the cross sectional analysis

Sample	Si-1	Si-4	Si-6
Number of samples with cracks	2	1	1
Number of investigated samples	3	2	2

5.4. Investigation of the influence bond area size

Process run B, with different sizes of bonded SMA pieces, was first investigated by visual inspection. More than 90% of the samples were bonded to the substrate. However all samples demonstrated large bowing effects and cracks in the silicon. Examples of a bonded 8 × 8 mm sample and a 2 × 2 mm sample can be seen in figure 21. Some samples

Figure 21. (a) Picture of bowing and delamination of a bonded SMA piece of 8×8 mm. (b) Optical profilometer measurements of the bowing of a 2×2 mm SMA sample.

had also been completely removed from the wafer and with a complete transfer of silicon onto the SMA, similar to figure 17(a). Since the failure rate was so high for all process run B samples, no more investigations were performed in detail on these samples.

6. Discussion

From the simulations and the many fabricated test samples conclusions can be drawn about which parameters are important to achieve a good SMA integration.

To achieve a high yield when performing Au–Si eutectic bonding of NiTi sheets onto silicon, the gold layer thickness is critical. A gold layer of 700 nm in total was too thin but by using a thickness of 1350 nm a yield $>90\%$ was achieved. This yield is relatively independent of the underlying substrate treatments as seen in table 2. The observed increase in bond yield related to an increase in gold thickness (figure 10) corresponds well to previous reports on Au–Si eutectic bonding of silicon wafers [15]. Unlike [15], a decrease in bond yield at thicknesses above $1 \mu\text{m}$ was not observed in our tests.

When thin gold layers are used (700 nm, SMA-1) the surface treatment influences the bond yield. The yield for these samples can be seen to be related to the ratio of gold/silicon in the bond interface, as plotted in figure 12. Since oxide is a good Au diffusion barrier, longer reoxidation times will result in less gold diffusing into the silicon [17] and will result in a higher gold concentration in the bond as shown in figure 11. However, Si-5 with native oxide and therefore a very long oxidation time in ambient air, demonstrates a lot of silicon on the surface (figure 9(e)). This lower gold content on the surface can be the effect of not modifying the surface by HF treatment and the decreased wetting of the Au–Si eutectic on an oxide layer [24]. By applying a TiW adhesion layer on a native oxide layer (Si-6) also increases the yield significantly (table 2). Both a decrease of Au diffusion into the bulk silicon and an increased adhesion to native oxide for the Au can contribute to this improved yield. As a conclusion, the amount of gold in relation to the amount of silicon in the bond interfaces is very important and is easy to control by deposition of a thick gold layer. Also creation of barrier layers like an oxide layer and TiW layer on the surface can increase the gold concentration and are interesting alternatives since the processing can be less expensive compared to thick Au layer depositions.

The bond strength of the Au–Si eutectic bond is very high as indicated by the shear tests (figure 15). The bulk silicon is the weakest point during shear testing (figure 17(a)). However

stress at the bond interface caused by the difference in thermal expansion of the two materials is a major concern. Bonding of samples of size $1 \times 1 \text{ mm}^2$ and larger was not feasible since there was a very high likelihood of crack formation in the bulk silicon as demonstrated in process run B. The large bowing observed on the samples (figure 21) also indicates that large stresses exist after the bonding. This indicates that patterning of the bond area to smaller than $1 \times 1 \text{ mm}^2$ is needed. The bond quality in process run B can also have been influenced by the edges of the SMA being slightly deformed or that some contamination was present from the dicing step before bonding but was most likely caused by the large thermal expansion mismatch. The increase in stress for larger bond areas is also validated by the simulations (figure 3). Even for bond areas smaller than $1 \times 1 \text{ mm}^2$, as for the bonded cantilevers in process run A, some cracks were detected during the cross section analysis (table 3). However, no correlation was seen between the existence of a crack and the bond area size or the silicon wafer type. It was not possible using our methods of analysis to determine whether these cracks were caused by the thermal mismatch of the materials or induced by the dicing, polymer embedding and polishing for the cross sectional analysis. Ideally the bond size should be as small as possible to reduce the risk of crack formation. On the other hand table 2 and figure 13 indicates that a larger bond area results in a higher yield, especially for samples with process parameters generating a low process yield, such as the SMA-1 samples (not including Si-1). However, for samples with process parameters generating a high yield, such as the SMA-2 samples (not including Si-7), the bond area influence is much lower. The high forces during dicing and handling and the risk of a small areas not being in contact with the target substrate during bonding can be the reasons for this decrease in yield for the smallest bond areas. A trade-off is therefore needed between the risk of crack formation for larger bond areas and the decrease in bond strength and yield for small areas. The bond area chosen should therefore be determined by the forces induced on the sample during fabrication and device cycling to achieve high bond strength with low risk of crack formation. Figure 13 also shows that a divided bond area, as in the case of bond area b, does not increase the yield for SMA-2 even though the total bond area is larger compared to bond area c.

If a crack would start to form it is likely to propagate into the bulk silicon. This is both demonstrated by the simulations (figure 6) and the destructed samples after shear testing (figure 17(a)). However, for the samples with a TiW adhesion

layer on a native oxide layer (Si-6) the destruction of the bulk silicon was not observed. This can be explained by the silicon surface not being consumed in this case and possible voids in the bond interface, which can act as crack initiating points, will be above the bulk silicon, not in it. A bond interface with voids or other non adhering regions has also been reported in literature to increase the stresses at the bond interface and to be responsible for crack formation [25]. Another important factor that can contribute to crack formation is that an increased gold diffusion, as is the case for Si-1 relative to Si-6 (figure 18), weakens the silicon lattice and can also increase the risk of crack formations [26].

An optional way to reduce the risk of crack formation in the bulk silicon can be to deposit amorphous silicon on an oxidized wafer since amorphous Au–Si eutectic is considered to have a more uniform bond interface and with lower chance of void formations [27]. An alternative method is to deposit a Ti layer, which dissolves any native oxide layer and increases the bond strength as demonstrated in a recent report [23]. These methods were not tested in this work.

Future research should investigate the bond area size influence for dimensions smaller than $800 \times 800 \mu\text{m}^2$. The risk of crack formation should be evaluated on free standing silicon structures to avoid the harsh dicing and polishing processing for cross sectional analysis of the bond interface. Also deposition of an additional layer of amorphous silicon or Ti is interesting to investigate for Au–Si eutectic bonding.

7. Conclusion

A wafer scale method for the integration of NiTi SMA cantilevers to silicon has been studied in detail. The SMA was Au–Si eutectically bonded to seven silicon substrates which had been prepared using different surface treatments, interface layers and Au layer thicknesses. The evaluation of the samples showed that the amount of gold in the bond interface is critical to achieve a high bond yield. The gold amount can be tuned by creation of barrier layers between the Au and Si or by the amount of Au deposition. A bond yield of more than 90% can be achieved with a deposition of an Au layer thickness of more than $1 \mu\text{m}$ thickness before bonding. To reduce the risk of crack formation caused by the thermal mismatch between the silicon and NiTi it is important to have a small bond area. A bond area between 200×200 and $800 \times 800 \mu\text{m}^2$ gave the highest yield in the test and lower risk of crack formation than bond areas larger than $1 \times 1 \text{ mm}^2$.

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