Digitally Enhanced Continuous-Time Sigma-Delta Analogue-to-Digital Converters

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Abstract

The continuous downscaling of CMOS technology presents advantages and difficulties for IC design. While it allows faster, denser and more energy efficient digital circuits, it also imposes several challenges which limit the performance of analogue circuits. Concurrently, applications are continuously pushing the boundaries of power efficiency and throughput of electronic systems. Accordingly, IC design is increasingly shifting into highly digital systems with few necessary analogue components. Particularly, continuous-time (CT) sigma-delta (ΣΔ) analogue-to-digital converters (ADCs) have recently received a growing interest, covering high-resolution medium-speed requirements or offering low power alternatives to low speed applications. However, there are still several aspects that deserve further investigation so as to enhance the ADC’s performance and functionality. The objective of the research performed in this thesis is the investigation of digital enhancement solutions for CT ΣΔ ADCs. In particular, two aspects are considered in this work.

First, highly digital techniques are investigated to minimize circuit impairments, with the objective of providing solutions with reduced analogue content. In this regard, a multi-bit CT ΣΔ modulator with reduced number of feedback levels is explored to minimize the use of linearisation techniques in the DAC. The proposed architecture is designed and validated through behavioural simulations targeting a mobile application. Additionally, a novel self-calibration technique, using test-signal injection and digital cancellation, is proposed to counteract process variations affecting single loop CT implementations. The effectiveness of the calibration technique is confirmed through corner simulations using behavioural models and shows that stability issues are minimized and that a 7 dB SNDR degradation can be avoided.

The second aspect of this thesis investigates the use of high order CT modulators in incremental ΣΔ (IΣΔ) and extended-range IΣΔ ADCs, with the objective of offering low-power alternatives for low-speed high-resolution multi-channel applications. First, a 3rd order single loop CT IΣΔ ADC, targeting an 8-channel 500 Ksamples/sec rate per channel recording system for neuropotential sensors, is proposed, fabricated and tested. The proposed architecture lays the theoretical groundwork and demonstrates a competitive performance of high-order CT IΣΔ ADCs for low-power multi-channel applications. The ADC achieves 65.3 dB/64 dB SNR/SNDR and 68.2 dB dynamic range. The modulator consumes 96 μW from a 1.6 V power supply. Additionally, the use of extended range approach in CT IΣΔ ADCs is investigated so as to reduce the required number of cycles per conversion while benefiting from the advantages of a CT implementation. The operation, influence of filter topology and impact of circuit non-idealities are first
analysed using a general approach and later validated through a test-case. It was found that, by applying analogue-digital compensation in the digital domain, it is possible to minimize the noise leakage due to analogue-digital transfer function mismatches and benefit from relaxed amplifiers’ finite gain-bandwidth product and finite DC gain, allowing, as a consequence, a power conscious alternative.

**Key Words**

analogue-to-digital conversion, sigma-delta modulation, digital enhancement, continuous-time, multi-channel applications