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Very high aspect ratio through-silicon vias (TSVs) fabricated using automated magnetic assembly of nickel wires

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Abstract
Through-silicon via (TSV) technology enables 3D-integrated devices with higher performance and lower cost as compared to 2D-integrated systems. This is mainly due to smaller dimensions of the package and shorter internal signal lengths with lower capacitive, resistive and inductive parasitics. This paper presents a novel low-cost fabrication technique for metal-filled TSVs with very high aspect ratios (>20). Nickel wires are placed in via holes of a silicon wafer by an automated magnetic assembly process and are used as a conductive path of the TSV. This metal filling technique enables the reliable fabrication of through-wafer vias with very high aspect ratios and potentially eliminates characteristic cost drivers in the TSV production such as advanced metallization processes, wafer thinning and general issues associated with thin-wafer handling.

Some figures may appear in colour only in the online journal

1. Introduction

3D-integrated system in package (3D-SiP) solutions, which are based on vertical chip stacking, are a general trend in electronics and MEMS packaging. Not only do 3D-SiPs decrease device cost by reducing the volume and weight of the package, but they also improve the system performance through enhanced signal transmission speed and lower power consumption, which is important for various demanding applications [1, 2]. Different technologies for the electrical interconnection of stacked dies exist, such as wire bonding, flip-chip bonding and through-silicon vias (TSVs). In particular, TSVs enable shorter signal path lengths with superior electrical characteristics in terms of lower capacitive, resistive and inductive parasitic components [3]. Therefore, large development efforts for the realization of reliable and cost-efficient TSVs are currently ongoing and first commercially available devices such as MEMS inertial sensors and microphones, CMOS imagers and power LEDs successfully incorporate TSV technology [4–6].

The structure and hence the fabrication of TSVs can be roughly divided into three major elements: a vertical hole through the substrate, a conductive core and a dielectric layer acting as an insulator between the conductor and the substrate. The most common fabrication techniques of these elements are briefly discussed in the following subsections.

Via holes. Various methods for the formation of via holes exist and can be categorized into dry etching [1, 7–13], wet etching [8] and drilling processes [4, 14]. Via holes can have either straight [9, 10, 12, 13, 15] or tapered sidewall profiles [7, 11] as well as combinations of both [8, 1]. Typical diameters of via holes vary between a few microns [2, 9] and several hundreds of microns [12, 15]. The majority of TSVs have an aspect ratio between 1 and 10. Deep reactive ion etching (DRIE) is by far the most commonly used technology to form TSV holes. DRIE offers an excellent process controllability and is capable of creating high aspect ratio vias with specific sidewall profiles and topographies. The etch rate of DRIE is aspect ratio dependent and may cause several topographic imperfections on the sidewalls of the via holes such as scalloping, caused by alternating etch and passivation steps,
which results in corrugated sidewalls. By using state-of-the-art DRIE equipment, these effects can be minimized [7] and adopted to the demands of subsequent insulation, barrier and seed-layer deposition steps.

Via insulator. Chemical vapor deposition (CVD) is a well-established CMOS-compatible process with moderate temperature requirements [1, 2, 11, 9] and is therefore the most commonly used method for a direct deposition of silicon dioxide or silicon nitride on via sidewalls. Organic dielectrics [16, 17] including benzocyclobutene (BCB) [13, 15, 18, 19], epoxy-based polymers [13, 12], silicone [13] or Parylene [11] are used as well. Polymers, especially low-k types with a lower relative permittivity compared to silicon dioxide, are very attractive for the realization of TSVs with improved electrical characteristics in terms of lower capacitive parasitics [20, 12, 15]. The relative permittivity of selected via insulation materials, including silicon nitride and silicon oxide as well as emerging low-k insulators. Silicon serves as reference in the first row.

Table 1. Relative permittivity $\epsilon_r$, Young’s modulus $E$, and coefficient of thermal expansion (CTE) of commonly used TSV insulation materials, including silicon nitride and silicon oxide as well as emerging low-k insulators. Silicon serves as reference in the first row.

<table>
<thead>
<tr>
<th>Material</th>
<th>$\epsilon_r$</th>
<th>$E$ (GPa)</th>
<th>CTE (ppm/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si [23]</td>
<td>$-$</td>
<td>190</td>
<td>2.33</td>
</tr>
<tr>
<td>SiO$_2$ (PECVD TEOS) [24]</td>
<td>3.9</td>
<td>64</td>
<td>2.61</td>
</tr>
<tr>
<td>Si$_3$N$_4$ (LPCVD) [25]</td>
<td>7</td>
<td>261</td>
<td>1.7–2.3</td>
</tr>
<tr>
<td>BCB 3000 Series (Dow) [26]</td>
<td>2.65$^a$</td>
<td>2.7–3</td>
<td>42.3</td>
</tr>
<tr>
<td>Parylene N [27]</td>
<td>2.65$^b$</td>
<td>2.4</td>
<td>69</td>
</tr>
<tr>
<td>SU-8 2000 (MicroChem) [28]</td>
<td>3.2$^c$</td>
<td>2</td>
<td>52</td>
</tr>
<tr>
<td>InterVia 8023 (Dow) [29]</td>
<td>3.2$^d$</td>
<td>4</td>
<td>62</td>
</tr>
</tbody>
</table>

$^a$ 1–20 GHz.
$^b$ 60 Hz–1 MHz.
$^c$ At 10 MHz.
$^d$ At 1 GHz.

Via conductor. The formation of a low-resistivity via conductor is the most critical and often most costly part of the via fabrication. The two basic via designs are either based on solid or lined metallizations for the vertical conductor. Established processes are electrodeposition of copper [8, 9, 11–13, 22], CVD of tungsten [2, 30], CVD of polysilicon [2, 31] and the use of low-resistivity bulk silicon [10]. In particular, electrodeposition of copper, being a very well established semiconductor process, is used by many research groups and implemented in most commercialized devices containing TSVs. Electrodeposition of copper benefits from widely available tool vendor support and process maturity as well as being amenable to deposition at near to room temperature, but suffers due to its complexity in terms of process controllability, reliability and throughput [4]. In particular, it is challenging to implement high aspect ratio TSVs with void-free conductive metal cores [4, 9, 32]. Alternative approaches to plating processes have therefore been investigated, such as the via filling with conductive metal pastes [1, 33, 34], solder [35, 36] as well as the use of wire-bonded metal cores [37, 38, 15].

As shown in Table 2, the electrical resistivity of ferromagnetic nickel is similar to tungsten, but approximately three to four times higher as compared to gold and copper. Volume-manufactured nickel wires with diameters down to 10 $\mu$m are commercially available and are typically used for chemically resistant woven filter cloth, screen printing masks and recently also for wire bonded interconnections in high-temperature packaging of SiC electronics [40].

In this work, we present the automated magnetic assembly of solid conductive via cores into TSV holes with very high aspect ratios. Magnetism as a non-contact force enables a controlled manipulation of ferromagnetic features over long distances and is insensitive to the surrounding medium and independent of details of the surface chemistry. Magnetic fields can have high-energy densities and can influence feature sizes from macro- to nano-scale. These advantageous characteristics are very attractive and have been reported in various assembly approaches [41]. The presented concept for the TSV metallization and insulation process enables high aspect ratio vias with an inherently void-free metal core.

As depicted in figure 1, the filling of the via with a conductive material is not realized by a deposition of a
metal but by an instant filling technique that magnetically assembles pre-formed conductive via cores into the via holes. The via insulator is a polymer that acts both as low-k electrical insulator and buffer against thermo-mechanically induced stresses. As shown in figures 1(b) and (c), the order of the metallization and insulation process step is reversed as compared to most conventional TSV fabrication scenarios where the metallization is gradually grown on barrier, insulation and seed layers. The proposed approach therefore does not require any additional high aspect ratio lithography and patterning of the insulation polymer. More importantly, this insulation technique is insensitive to the topography of the via sidewall (i.e. scallops). The proposed fabrication method enables a cost-effective fabrication of high aspect ratio TSVs especially for low- to medium-D0 density applications such as interposers and MEMS. A proof of concept of the fabrication of TSVs with an aspect ratio of 8 by manual magnetic assembly has been shown by the authors earlier [18, 19]. This method has also been adopted for the assembly of SMD capacitors into through-silicon holes [42].

2. TSV fabrication by automated magnetic assembly

2.1. Robotic assembly setup

An automated assembly process that utilizes the ferromagnetic properties of nickel has been developed for the placement of nickel cores into via holes. In this process, an excess amount of nickel wires are randomly placed on the frontside of a wafer and assembled into etched via holes. By applying a magnetic field, induced by a permanent magnet from the backside of the wafer, the nickel wires align themselves along the field lines and erect themselves perpendicular to the wafer surface, as shown in figure 2. Because of the magnetic force the wires always will remain above the magnet. This effect allows the nickel wires to be steered around on the wafer surface by simply moving the permanent magnet laterally underneath the wafer. The assembly of the nickel cores is achieved by magnetically moving the wires over the via holes. The upright position of the wires allows them to be pulled into the holes by the magnet.

For this magnetic assembly process a robotic setup has been devised. It is based on a handler robot (IWH-series) for 200 mm wafers from Isel Germany AG. Figure 3 shows a schematic depiction of the robot arm that has been modified in order to mount a cubic permanent magnet with an edge length of 5 mm. This tool enables a programmable movement of the magnet with three degrees of freedom at a precision of 30 μm. That way different movement patterns were implemented and adopted to varying layouts of via holes. Also depicted in figure 3 is a camera that is mounted directly above the magnet and faces the frontside of the substrate. It is used to optically inspect the substrate surface before and after the assembly and to monitor the assembly process. Furthermore, the tool still retains its capability to handle wafers with the wafer gripper that is a part of the robot arm. This robot arm has a movement range of ±240° around its axis, ±366 mm in the radial direction and 323 mm in the vertical direction. The maximum speeds are 360° s⁻¹, 1000 mm s⁻¹ radial and 450 mm s⁻¹ vertical. By using a wafer handler robot for the magnetic assembly, an automated cassette-to-cassette process can be implemented, i.e. picking a wafer from a input/output cassette, placing it on a dedicated assembly stage, performing the magnetic assembly and placing the wafer back into the cassette.

Figure 2. Behaviour of nickel wires in a magnetic field. (a) About 300 straight nickel wires (35 μm diameter, 350 μm length) without an applied field. (b) A magnetic field of 1.1 T is generated by a cylindrical permanent magnet. It aligns the nickel wires along the field lines perpendicular to the ground plane.

Figure 3. (a) Assembly setup with the wafer gripper and assembly part on the robot arm in the centre of the table, the wafer cassette station and the assembly stage to its right. The assembly process consists of four steps: (1) scanning the cassette for wafers, (2) picking the chosen wafer and placing it on the assembly stage, (3) positioning the assembly arm, placing the magnetic via cores manually on the substrate and carrying out the automated magnetic assembly, (4) putting the wafer back into the cassette. (b) Schematic drawing showing the custom-built assembly arm that consists of a permanent magnet mounted on an aluminium sheet and a camera above the magnet.
2.2. Nickel wire preparation

In order to cut a nickel wire into rods of a defined length, a cutting process was developed. For the experiments, Ni-270 wire with a purity of 99.97% with two different diameters was used, 15 and 35 μm. As depicted in figure 4(a), several wires are placed in parallel on a silicon carrier wafer and subsequently embedded in a polymer matrix (figure 4(b)) in order to safely fixate the wires on the carrier wafer and to minimize the deformation and burr creation during the cutting process. The wires are then cut with the help of a wafer dicing tool (figure 4(c)) and finally released by dissolving the polymer in a solvent.

A good adhesion of the photoresist to the silicon substrate is essential in order to ensure a proper fixation of the wire rods during the dicing process. Figure 4(d) depicts that the photoresist tends to peel off with decreasing dicing pitch (i.e. nickel rod length) on substrates that are treated with standard hexamethyldisilazane (HMDS) as an adhesion promoter. In order to increase the yield of the wire cutting process, the bond strength between the carrier substrate and the novolac-based photoresist was increased by a custom-made adhesion promoter. The silicon carrier substrate was immersed in a solution of 5% 3-(triethoxysilyl)propylsuccinimide and 95% Toluene for 10 min. The wafer was then rinsed with Toluene, blow-dried and finally baked in a oven at a temperature of 105 °C for 10 min. The applied silane reacts with the wafer surface via a silanization reaction, forming a very thin, covalently bonded organic layer. Upon completion of the silanization step, a very dense concentration of anhydride groups is exposed on the surface. Anhydride groups readily react with the hydroxyl groups present in the uncured novolac photoresist, that is applied later on. After the aforementioned treatment, the wires were manually placed on a dummy wafer and fixated with blue tape at the outer perimeter of a carrier, as shown in figure 4(a). A layer of AZ® 4562 photoresist was then spin-coated on the carrier wafer at 1000 rpm for 30 s. The photoresist was soft baked on a hotplate at a temperature of 50 °C for 3 min. A low soft-baking temperature was chosen in order to retain sufficient elastic properties of the polymer. As depicted in figure 4(c), the nickel wires were fully embedded in the photoresist matrix. A DAD 320 (DISCO Corporation, Japan) wafer dicing tool that was equipped with a 38 μm wide dicing blade was used to cut the wires. The dicing feed speed was 10 mm s⁻¹. The accurate alignment of the dicing tool allowed for perfectly perpendicular cuts and the length of the rods could be precisely controlled by the dicing tool. Figure 4(e) shows that the resist fully adheres to the silicon surface and does not peel off for dicing pitches of 150 μm. That way a yield of 100% for the cutting process could be achieved. Subsequently, the nickel rods could easily be released by dissolving the resist layer with acetone. This process allows a very precise cutting of many wires in parallel and can produce several thousands of nickel rods per run.

Laser cutting or automated wire cutting tools may serve as an alternative method especially for a high-volume production of nickel rods.

2.3. TSV fabrication

The fabrication process for the TSVs is illustrated in figure 5 and is based on double-side polished 100 mm Si wafers with a 2 μm thick silicon dioxide layer on both sides, which was created by thermal wet oxidation at 1100 °C. The oxide acts
Figure 5. The TSV fabrication scheme can be divided into three main steps. First is the formation of the via hole by DRIE etching, second is the magnetic assembly of the conductive TSV core and third is the filling with the dielectric.

both as a hard mask for the DRIE step and as an electrical insulator for the metal lines, which will finally connect the via on the frontside and backside of the substrate. A standard lithography on the frontside of the substrate defines the circular openings for the vias. The silicon dioxide is dry-etched by RIE, as illustrated in figure 5(b). As depicted in figure 5(c), a Bosch DRIE process creates via holes with straight side walls. The DRIE stops at the silicon dioxide on the bottom of the cavity. A subsequent high temperature treatment at 1100 °C in a furnace is used to remove polymer residuals from the DRIE passivation cycles by pyrolization. In the same furnace, a thermal oxidation at 1100 °C creates a 0.5 μm thick silicon dioxide layer, as shown in figure 5(d). The silicon dioxide layer ensures an electrical insulation of the via sidewalls and creates a hydrophilic surface on the via sidewall, which is of importance for the insulation step that is carried out later on.

The pre-fabricated nickel cores are then distributed on the frontside of the target wafer. By utilizing the robotic assembly tool, the permanent magnet on the assembly arm can be moved into close proximity of the backside of the wafer, as indicated in figure 5(f). The nickel wires that are manually placed on the wafer surface are drawn to the location of the magnet and erect themselves perpendicular to the substrate surface. With programmed patterns for the magnet movement, all via holes can be filled in an automated process. The results of the performed assembly experiments, including the movement patterns and the yield of the filling process, are presented in section 4.

The via cavities are subsequently filled with the thermosetting polymer BCB CYCLOTENE® 3022-46 (figure 5(g)), which is known to be suited for a void-free filling of high aspect ratio features [43]. In order to reduce the viscosity of the polymer, the substrate is placed on a hotplate with a temperature of 60 °C before the polymer is manually applied to the wafer surface using a syringe. As the polymer is not spin-coated, the resulting polymer layer has a non-uniform thickness on the order of 100−150 μm. The subsequent hard-curing of the BCB is performed on a hotplate in a vacuum chamber using the temperature profile according to the manufacturer’s standard process procedures [26]. The entire curing procedure was performed in a vacuum environment at 0.02 mbar in order to prevent any void formation in the polymer. A subsequent grinding and polishing step removes excess nickel and BCB from the surface of the substrate, as shown in figure 5(i). A lithography and RIE of the silicon dioxide and BCB residues opens the contact area of the via on the backside of the wafer, as illustrated in
Two consecutive TiW/Au depositions (50/1000 nm) on both sides of the wafer interconnects the nickel cores of the vias. A lithography, wet Au etch and dry TiW etch (figure 5(k)) are made to define the Kelvin test structures.

3. Experimental results

The performance of the robotic assembly setup in terms of assembly speed was evaluated and an optical inspection and an electrical characterization of the fabricated TSVs were performed.

3.1. Automated magnetic assembly

A series of assembly experiments with different movement parameters was conducted. As shown in figure 6, the magnetic assembly process was performed on array structures of via holes with an excessive amount of nickel wires of approximately 2500–3000. The wires in these experiments had a diameter of 35 μm and a length of 360 μm. The via holes had a diameter of 42 μm and were fabricated in arrays of 10 × 10 vias with a pitch of 350 μm on a substrate with a thickness of 350 μm. With respect to the array size of 3.5 mm and the size of the cubic permanent magnet with an edge length of 5 mm, two different movement patterns were programmed, as schematically illustrated in figure 6. The pattern in figure 6(a) has a very short sweep length \( d \) of 0.76 mm, whereas the pattern in figure 6(b) sweeps over the array with a sweep length \( d \) of 1.5 cm. Furthermore, the experiments have been conducted at two assembly motion speeds, a fast motion at 120 °s⁻¹ and a slow motion at 4 °s⁻¹. The vertical distance of the magnet to the backside of the wafer was approximately 125 μm in all experiments.

As figure 7 shows, the filling rate, i.e. the number of filled via holes per second, is dependent on the speed and the sweep length \( d \) of the assembly motion. Larger sweep lengths result in a faster filling process. The lateral force on the wires only occurs due to a gradient in the magnetic field, which is more prominent near the edge of the cubic magnet. For small sweep lengths, this implies that the wires located above the centre of the magnet move very little or not at all, which explains the poor filling rate from the movement pattern shown in figure 6(a). Also shown in figure 7, the assembly process improves with decreasing speed of the assembly motion. A fast assembly motion causes the wires to tilt from their perpendicular position while being dragged along the substrate surface which makes it more difficult to pull them into the via holes. Slower motion speeds reduce the wire tilt and therefore increase the filling rate. As shown in figure 7, a filling yield of 100% within 66 to 81 s could be demonstrated by using the movement pattern indicated in figure 6(b) and a slow motion speed of 4 °s⁻¹.

As shown in figure 8, assembled wires that are protruding the substrate surface act both as a mechanical and magnetic obstruction for the excess wires during the assembly process.

**Figure 7.** Filling rates for the assembly of via arrays (10 × 10 holes). Two different movement patterns and two different speeds were tested. The slow patterns exhibited a yield of 100% and the highest filling rate.

**Figure 8.** SEM image of a 30 × 30 array with a pitch of 120 μm of nickel wires placed in the via hole prior to the filling of BCB. The minimum via hole diameter for a 35 μm wire was determined to be 40 μm.
These two effects have a negative impact on the filling rate. In order to overcome the mechanical obstruction, the wires can be cut to a length that is the same or shorter as the depth of the via holes. Due to the magnetization of the nickel during the assembly process, the excess wires can stick to the ends of assembled wires and cluster even if the assembly-magnet moves on. It is possible to demagnetize and thereby eliminate the clustering of the ferromagnetic nickel rods by reversing the magnetic field by either flipping the permanent magnet or using an alternating magnetic field that is induced by a electromagnet. By flipping the permanent magnet it was even possible to fill a via array with a very dense pitch of 120 μm with wires that were considerably protruding the surface by approximately 150 μm, as shown in figure 8.

Potentially, the assembly process can be improved and further accelerated by the implementation of a direct optical inspection feedback. The camera, depicted in figure 3, that is mounted on the assembly robot has only been used for monitoring the assembly process in our experiments. By using an automated pattern recognition, the software can be extended to be able to identify filled and empty holes. This information can then be used to implement a feedback loop for the assembly movement. Thus, an adaptive optimization of the assembly movement during operation can be obtained. Moreover, this addition would provide the assembly process with an inherent quality control functionality that detects unfilled via holes.

3.2. Cross-section inspection of filled TSVs

In order to evaluate the filling with dielectric and nickel, several polished cuts through magnetically assembled TSVs have been prepared and inspected by optical microscopy and scanning electron microscopy (SEM). As shown in figures 9(a) and (b), the filling with BCB was successfully conducted without any visible air-voids or defects after the complete hard curing procedure. Also, due to the use of wire as a base material, the nickel core is inherently void-free. There are no indications for delamination of the BCB at the via side walls or the via core, which might cause mechanical or electrical failures of the vias. Figure 9(a) shows the cross-section of a magnetically assembled TSV with an aspect ratio of 8 that consists of a nickel core with diameter of 35 μm, a length of 325 μm and a via hole diameter of 40 μm.

As depicted in figure 9(b), a similar inspection was performed with a magnetically assembled TSV with an aspect ratio of approximately 24. This TSV consists of a nickel core with diameter of 15 μm and a length of 470 μm that was assembled in a via hole with a diameter of 20 μm.

3.3. Electrical characterization

The electrical resistance of magnetically assembled nickel TSVs with a diameter of 35 μm and a length of 250 μm has been evaluated. A chip with a 10 × 10 array of TSVs with a pitch of 350 μm was mounted in a ceramic dual in-line package with an open cavity (figure 10(a)). As illustrated in figure 10(b), each via was contacted on the frontside with two wire bonds that have been placed with an automatic wire bonder model ESEC 3100+. On the backside, the vias are
electrically connected by a blank metallization. A four-wire measurement was performed on 25 pairs of TSVs (i.e. 50 TSVs) using a HP 34401A digital multimeter. The measured total resistance is in average 83 mΩ for two TSVs, including their contact metallization on the frontside and backside of the chip. This is in good agreement with the theoretical resistance of one pair of Ni TSVs of the given dimensions, which is approximately 40 mΩ, excluding any contact metallization.

4. Conclusions

The fabrication of TSVs with aspect ratios of up to 24 based on an automated magnetic assembly process has been demonstrated. Smaller TSV diameters and higher aspect ratios are feasible but limited by the smallest commercially available diameter of ferromagnetic wires, which is to our knowledge currently 10 μm for nickel. The novel automated magnetic assembly process enables a high-speed filling of TSV holes with high aspect ratio via cores for low- to medium-I/O density applications such as interposers and MEMS. The presented concept addresses main fabrication objectives relevant for state-of-the-art, low-resistance metal TSVs such as reliable fabrication of high aspect ratio vias, void-free solid metallizations, sufficient thermo-mechanical stability and reduction of fabrication costs.

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