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Experimental Comparison of Different Gate-Driver Configurations for Parallel-Connection of Normally-on SiC JFETs

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Abstract— Due to the low current ratings of the currently available silicon carbide (SiC) switches they cannot be employed in high-power converters. Thus, it is necessary to parallel-connect several switches in order to reach higher current ratings. This paper presents an investigation of parallel-connected normally-on SiC junction field effect transistors. There are four crucial parameters affecting the effectiveness of the parallel-connected switches. However, the pinch-off voltage and the reverse breakdown voltage of the gates seem to be the most important parameters which affect the switching performance of the devices. In particular, the spread in these two parameters might affect the stable off-state operation of the switches. The switching performance and the switching losses of a pair of parallel-connected devices having different reverse breakdown voltages of the gates is investigated by employing three different gate-driver configurations. It is experimentally shown that using a single gate-driver circuit the switching performance of the parallel-connected devices is almost identical, while the total switching losses are lower compared to the other two configurations.

Keywords– Junction Field Effect Transistor; parallel-connected switches; gate drivers; Silicon Carbide;

I. INTRODUCTION

A variety of advantageous characteristics of silicon carbide (SiC) switches contributes to the establishment of such devices as a serious competitor to state-of-the-art silicon counterparts. One of the most promising SiC switches is the junction field effect transistor (JFET) due to the very simple structure [1]-[2], and the very low specific on-state resistance [3]. Two additional benefits of the SiC JFET are that there is no need for a base current as in the SiC bipolar junction transistor [4], neither a gate oxide layer is necessary as in the metal-oxide-semiconductor field-effect transistor.

Switch-mode power supplies, power electronics converters for photovoltaic power generation [5], hybrid electric cars [6]-[7], power factor correction circuits [8], and high-power applications such as Static Synchronous Compensators (STATCOMs) and high-voltage direct current transmission

(HVDC) [9] can be considered as possible future applications of SiC JFETs.

Although there is an excellent potential for employing SiC JFETs in medium and high-power future applications, the present development status of the SiC JFET from the voltage and current ratings point-of-view decelerates this possibility. The main reason for this is probably the very low fabrication yields obtained if large chips are fabricated. It is, therefore, obvious that the only way to reach higher current ratings is either to build multi-chip modules [10] or to parallel-connect several single-chip discrete components [11]-[12]. Even though these seem to be the ideal solutions to the problem, they might suffer from mismatches both in transient and steady-state currents.

There are, basically, four crucial parameters affecting the feasibility of parallel-connected normally-on SiC JFETs. The first parameter is the on-state resistance of the devices which must have a low spread and a positive temperature coefficient. Having a low spread means that the steady-state current sharing will be even and thus the conduction losses will also be evenly distributed among the discrete devices. The second parameter is the pinch-off voltage that is the gate-source voltage of the device at which the JFET starts to conduct current. From experience it is known [11] that a spread in the pinch-off voltages of the parallel-connected JFETs will affect the transient current and, therefore, the distribution of the switching losses among the parallel-connected chips. The reverse breakdown voltage of the gates, $V_{br,g}$, counts as the third important parameter affecting the performance of the parallel-connected SiC JFETs. This parameter determines at which voltage the gate-source junction is driven into either punch-through (PT) or avalanche, based on the JFET design, and it must not be exceeded. If the spread between the pinch-off voltage and the reverse breakdown voltage of the gate is too large, there might be no possibility for a stable off-state operation. In particular, in such an extreme case one of the chips might still conduct, while the gate-source junction of the other one would already have been driven into PT or

avalanche. A solution to this problem could be sorting of the parallel-connected devices with respect either to their pinch-off or reverse breakdown voltages of the gates. However, the sorting criteria might be affected by the temperature dependence of the reverse breakdown voltage of the gate [10]. Last, but not least the variations in the static transfer characteristics among the devices can also be considered as a crucial parameter affecting the performance of the parallel-connection.

An investigation regarding parallel-connection of normally-off SiC JFETs and SiC Bipolar Junction Transistors (SiC BJT) has been done in [12]. This study basically focuses on the dependence of various static and dynamic characteristics of the devices on the temperature. Moreover, a first attempt to show the problems of parallel-connected normally-on SiC JFETs is shown in [11], where the devices are sorted with respect to their pinch-off voltages. It is not only the current mismatches that are shown in this study, but also the uneven distribution of the switching losses among the JFETs. The application of a module with four parallel-connected single SiC JFET chips is presented in [10].

The goal of the present paper is to investigate the effect of the gate-driver configuration on the performance of parallel-connected SiC JFETs. Various gate-driver designs are studied both from the switching performance and the switching losses point-of-views. Section II shows the structure of the SiC JFET which has been considered in the present study. The basic characteristics of the gate drivers that have been employed are analyzed in Section III, while in Section IV the experimental setup is described and various experimental results are presented. Finally, a discussion regarding the results is given in Section V.

II. VERTICAL-TRENCH SiC JFET

The JFET design which has been taken into account in this study is the so-called “Vertical-Trench SiC JFET” (VTJFET). The cross-section of this JFET design is shown in Fig. 1. This device can be either normally-on or normally-off depending on the thickness and the doping levels of the vertical channel. In the present study the normally-on version of this specific JFET design, which is also called Depletion-Mode Vertical-Trench SiC JFET, was employed.

Fig. 1. Graphical illustration of the cross-section of the Depletion-Mode Vertical Trench JFET.

The typical gate-source pinch-off voltage of this device is approximately -6 V, while the range of $V_{br,g}$ is -19 to -28 V. It must be noted that this JFET design has no anti-parallel body-diode like in the case of Lateral- Channel SiC JFET [1]. However, the reverse current can flow through the channel in the SiC VTJFET. An additional advantageous characteristic of the VTJFET is the almost temperature independent $V_{br,g}$, as can be seen in Fig. 2. It is clear from this figure that $V_{br,g}$ is slightly increasing when the temperature is also increasing. However, as it has been already shown in [11] $V_{br,g}$ of the Lateral-Channel SiC JFET is a strongly temperature-dependent device parameter. It must also be noted that in both JFET designs the pinch-off voltages are temperature independent. Thus, the margin between $V_{br,g}$ and the pinch-off voltage of the VTJFET is almost constant from room temperature up to elevated temperatures.

Fig. 2. Measurements of the temperature dependence of the reverse breakdown voltage of the gate of a vertical trench SiC JFET.

Taking into account the analysis shown above, the VTJFET design has been considered in the present investigation. In particular, two discrete SiC VTJFET devices were chosen with respect to their values of $V_{br,g}$. Table I shows $V_{br,g}$ of the two devices under test (DUT), while the voltage and current ratings and the on-state resistance at room temperature are also summarized in the same table, where a difference in $V_{br,g}$ of approximately 7 V is observed.

Device No.	Voltage and Current ratings	On-state resistance at room-temperature	$V_{br,g}$
45	1200 V, 27 A	85 mΩ	-21.1 V
50	1200 V, 27 A	85 mΩ	-28.0 V

Fig. 3 illustrates experimental results of the static transfer characteristics of these devices, indicating that the difference of approximately 7 V in $V_{br,g}$ is correlated to a difference of approximately 0.5 V in the pinch-off voltages of the devices. The device with the less negative $V_{br,g}$ also has the less negative pinch-off voltage. Even if this is not a solid statistical proof of the correlation between the $V_{br,g}$ and the pinch-off voltage, it is a strong indication that the $V_{br,g}$ can be used as a sorting criterion.

Fig. 3. Measured static transfer characteristics showing the relevance between the reverse breakdown voltage of the gate and the pinch-off voltage.

III. GATE DRIVERS FOR PARALLEL-CONNECTED SiC JFETs

The gate or base-drive unit counts as one of the most vital parts of a power electronics converter. By properly adjusting the parameters of the driver, the power semiconductor devices are able to switch as fast as possible and produce the minimum amount of switching losses. On the other hand, the power consumption of a drive unit also contributes to the total losses of the converter and it might be quite significant if high switching speeds are required.

In the case of parallel-connected SiC JFETs, a special design effort for the gate driver must be made in order to overcome any possible mismatches in the transient currents of the devices. In this paper three different gate-driver configurations are considered. They are all based on a gate-drive unit which has been previously proposed [13] and it is depicted in Fig. 4. It consists of a parallel network of a diode D , a resistor R_p and a speed-up capacitor C , while a gate resistor, R_g , is connected in series with this network.

In order to overcome any variations in the reverse breakdown voltages of the gates, the gate driver is supplied by a voltage which is more negative than the most negative reverse breakdown voltage of the gate of all parallel-connected devices. Additionally, the leakage current of the gate is limited by means of resistor R_p and it is therefore impossible to drive the gate-source junction into avalanche if R_p is chosen adequately.

During the on-state of the device, the buffer output voltage, V_{gs} , equals zero and the JFET is conducting. When the turn-off process starts, the buffer output voltage, V_{gs} , equals the supply voltage, V_s , and a high negative current peak is supplied to the gate-source junction of the device through C and R_g (shown with the dashed line in Fig. 4). Thus, the gate-source parasitic capacitance, C_{gs} , is charged to a voltage that equals the reverse breakdown voltage of the gate. Simultaneously, the gate capacitor C is also charged and the voltage drop across it equals the difference between the supply voltage V_s and the reverse breakdown voltage of the gate. A low gate current is required during the steady-state operation in the off-state and it is supplied through the high-value resistor R_p , as shown with the red solid line in Fig. 4.

Fig. 4 Gate driver of the normally-on SiC JFET.

Based on the fundamental design of this gate driver, which has been already described above, three different configurations were designed and experimentally verified for parallel-connected normally-on SiC JFETs. According to the first design, a separated diode-resistor-capacitor network (DR_pC network) and a series-connected gate resistor are employed for each of the parallel-connected devices, as shown in Fig. 5. The second driver design is based on the separated DR_pC networks and gate resistors, but a small ferrite core is connected on the signal outputs in order to eliminate any possible unbalances in the gate currents (Fig. 6). It might, therefore, be possible to obtain an almost identical behavior of the transient currents of the devices. Finally, the third gate-driver design employs a common DR_pC network and gate resistor for all parallel-connected SiC JFETs as depicted in Fig. 7. Thus, there is only one common path for the gate current.

In order to perform a fair comparison between the three different gate-driver configurations, the switching speed of these should be identical. This practically means that the parameters of the DR_pC networks and the value of the gate resistors should be properly adjusted, so that the switching speed of the drivers themselves will be approximately equal. From the DR_pC network point-of-view, there are basically two driver configurations: with separated DR_pC networks and with a single DR_pC network. In the case of n parallel-connected SiC JFETs which use a single DR_pC network, the value of the speed-up capacitor should be equal to n times the corresponding value of the capacitor in the separated DR_pC networks. On the other hand, the gate resistor should be reduced such that the total resistance, considering the internal resistance in the Integrated Circuit driver (IC-driver), will be the same for both driver configurations.

Fig. 5 Parallel-connected SiC JFETs fed by separated DR_pC networks.

Fig. 6 Parallel-connected SiC JFETs fed by separated DR_pC networks with a small ferrite core.

Fig. 7 Parallel-connected SiC JFETs fed by a single DR_pC network.

TABLE II. PARAMETERS OF THE GATE-DRIVER CIRCUITS

Gate-driver configuration	Double DR_pC network	Single DR_pC network
Gate-driver supply, V_s	-30 V	-30 V
Gate resistor, $R_{g1,2}/R_g$	5 Ω	1.7 Ω
R_{p1}, R_{p2}, R_p	12 k Ω	12 k Ω
C_1, C_2, C	22 nF	44 nF
D_1, D_2, D	Schottky diode SMA 40 V, 1 A, SK 14	Schottky diode SMA 40 V, 1 A, SK 14

In this paper, the switching performance of two parallel-connected normally-on SiC JFETs is investigated by employing the three different gate driver configurations. The parameters of the separated and single DR_pC networks were properly adjusted for each case such that the driver switching speeds were approximately equal. Table II summarizes the parameters of the two different gate driver configurations.

IV. EXPERIMENTAL RESULTS

The feasibility of the parallel connection of normally-on SiC JFETs can be studied both from the static parameters point-of-view, but also by investigating the switching performance of these devices. Both static and dynamic parameters of the devices are important and they might affect the effectiveness of the parallel-connected JFETs. However, this paper only presents the possible problems caused during the switching transients of SiC JFETs having different $V_{br,g}$. As shown below, the current mismatches during the switching transients are strongly related to $V_{br,g}$ and they might be significantly reduced or even eliminated by employing an appropriate gate-driver design. This is basically the reason why the focus of the present study is limited to the impact of $V_{br,g}$ on the performance of the parallel-connected devices.

The experimental evaluation of the three different driver configurations has been performed by using a standard double-pulse test circuit. The circuit layout, which is believed to affect the effectiveness of the parallel-connected devices, was designed to be as symmetrical as possible (Fig. 8). Furthermore, in order to reach a higher degree of symmetry, two parallel-connected SiC Schottky diodes were employed and placed in such a way that the inductive paths from the anodes pins to the drain pins of the JFETs are approximately the same.

Fig. 8 Schematic of the circuit layout.

A. Gate driver with double DR_pC

The first set of measurements was performed using a gate driver with a double DR_pC network. The turn-on transients for the currents of the two parallel-connected devices are depicted in Fig. 9. Despite the approximately equal current speeds, a significant difference in the currents after the turn-on process is obtained. The reason for this seems to be the different voltage drops across the parasitic capacitances of the gate-source junctions of devices No. 50 and No. 45 when both JFETs are in the off-state. This difference in the gate-source voltages equals the difference in $V_{br,g}$ of these two devices. When the devices are turned on, the parasitic gate-source junction of JFET No. 45 is discharged faster than for JFET No. 50. Thus, JFET No. 45, having less negative reverse breakdown voltage of the gate, carries a higher transient current during the turn-on process. As a consequence, the turn-on losses for JFET No. 45 will be higher than for No. 50.

Fig. 10 shows the turn-off process when a gate-driver with a double DR_pC network is employed. A mismatch in the transient currents is also observed in this case.

Fig. 9 Currents during the turn-on process when a double DR_pC network is employed.

Fig. 10 Currents during the turn-off process when a double DR_pC network is employed.

B. Gate driver with double DR_pC and ferrite core

In order to balance the gate currents supplied to the two parallel-connected JFETs, a small ferrite core was connected on the outputs of the double DR_pC gate driver as shown in Fig. 6. Figs. 11 and 12 show the turn-on and turn-off processes respectively. A faster balancing for the steady-state currents is observed due to the balancing ferrite core, but on the contrary there are still mismatches in the transient currents. Even though the gate currents are approximately identical, it is the hypothesis of the authors that the transient differences in the drain current are due to a combination of differences in the static transfer characteristics and a small parasitic inductance in the main circuit. It is clear that these mismatches have an impact on the switching losses as it is shown below.

Fig. 11 Currents during the turn-on process when a double DR_pC network with a ferrite core is employed.

Fig. 12 Currents during the turn-off process when a double DR_pC network with a ferrite core is employed.

C. Gate driver with single DR_pC

The final set of measurements has been done by employing a gate driver with single DR_pC network. The turn-on process is depicted in Fig. 13, where it can be seen that the current mismatches have been significantly reduced but they are not totally eliminated. The device with the more negative $V_{br,g}$ conducts a slightly higher current than the other one. The steady-state current seems to be well-balanced, while the transient currents during the turn-off process are approximately identical (Fig. 14). This is caused due to the fact that the parasitic capacitances of the gate-source junctions are charged at the same voltage level, which in this certain case equals the less negative $V_{br,g}$ of JFET No. 45.

Fig. 13 Currents during the turn-on process when a single DR_pC network is employed.

Fig. 14 Currents during the turn-off process when a single DR_pC network is employed.

D. Switching losses

The switching losses for both parallel-connected SiC JFETs have been estimated by using recorded data from measurements and they are shown in Table IV. The total losses per device seem to be a good indication on how different the temperature distribution on the devices will be when they are employed in a converter. From Table IV it is observed that the difference in the total losses per device for the single DR_pC driver configuration is the lowest one among all the drivers. Similarly, by investigating the total losses for both devices it can be concluded that the lowest amount of switching losses are caused by using a single DR_pC network, even though the losses per device are not evenly distributed between the JFETs. Finally, by employing a double DR_pC network the total amount of the switching losses are the highest of all driver configurations.

It must also be noted that a correct estimation of the switching losses of the DUTs can only be done if the sum of the switching losses at turn-on and turn-off is studied, and not on the turn-on and turn-off contributions separately. The reason for this is that the energy which is stored and released from the stray capacitances of the DUTs is also included in the corresponding values of turn-on and turn-off losses in Table IV. This phenomenon is only observed when sufficiently high switching speeds are used. If the switching speed of the DUTs is significantly reduced, the values for turn-on and turn-off losses will be the actual ones.

CONCLUSIONS

In this paper three different gate-driver configurations for parallel-connection of normally-on SiC JFETs have been presented.

As it has been already presented [11], there are basically four crucial device parameters affecting the feasibility of the parallel-connected SiC JFETs. In the present study the parallel-connected JFETs were chosen with respect to their $V_{br,g}$. In particular two devices having a difference of approximately 7 V in $V_{br,g}$ were chosen for the experiments. The sorting criterion is based on the correlation between the pinch-off voltages and $V_{br,g}$ of the DUTs. In particular, it was experimentally shown that any relevance difference between $V_{br,g}$ of the DUTs is anticipated into a relevant difference in the pinch-off voltages (Fig. 3). Even though this assumption is based on measured data and it is valid for the present case, it requires a further investigation. Both the switching performance and the switching losses of the DUTs have been studied for all three gate-driver cases.

It is experimentally shown that by employing a gate driver with a single DR_pC network the currents of the JFETs during the switching transients are improved. In particular, during the turn-on process the current sharing among the two JFETs is much better (Fig. 13) than for the other two gate-driver configurations. Similarly, an even greater improvement is obtained during the turn-off transient with a single DR_pC network (Fig. 14). In this case the currents through the two parallel-connected SiC JFETs are almost identical. The main reason for this seems to be that the parasitic capacitances of

the gate-source junction are charged to the same voltage. On the contrary, in the two other gate-driver configurations these parasitic capacitances were charged to different voltages equal to their $V_{br,g}$. Thus, assuming that the DR_pC networks in the double-DR_pC driver are identical (equal gate resistors and speed-up capacitors), the device with the more negative $V_{br,g}$ is reaching the value of the steady-state current slower than the other one (Figs. 9 and 11).

The switching losses for the parallel-connected devices have also been estimated using experimental data. It is shown in Table IV that the most even distribution of the switching losses among the parallel-connected devices is obtained when a single DR_pC network is utilized. Furthermore, the total switching losses in the JFETs are the lowest in the case with a gate driver with a single DR_pC network. This can be verified by studying the current overshoots during the switching transients. In the case with a single-DR_pC driver the high current overshoots were significantly reduced compared to the gate-driver configuration with a double DR_pC network.

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TABLE IV
SWITCHING LOSSES

<i>Driver configuration</i>	<i>Device No 50</i>		<i>Device No 45</i>		<i>Total losses per device (μJ)</i>		<i>Total losses for both devices (μJ)</i>
	<i>Turn-on losses (μJ)</i>	<i>Turn-off losses (μJ)</i>	<i>Turn-on losses (μJ)</i>	<i>Turn-off losses (μJ)</i>	<i>Device No 50</i>	<i>Device No 45</i>	
Double DR _p C	130	90	170	100	220	270	490
Double DR _p C /core	130	85	145	110	215	255	470
Single DR _p C	115	100	100	80	215	180	395