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Layer-by-Layer 3D Printing of Si Micro- and Nanostructures by Si Deposition, Ion Implantation and Selective Si Etching

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Abstract—In this paper we report a method for layer-by-layer printing of three-dimensional (3D) silicon (Si) micro- and nanostructures. This fabrication method is based on a sequence of alternating steps of chemical vapor deposition of Si and local implantation of gallium (Ga⁺) ions by focused ion beam (FIB) writing. The defined 3D structures are formed in a final step by selectively wet etching the non-implanted Si in potassium hydroxide (KOH). We demonstrate the viability of the method by fabricating 2 and 3-layer 3D Si structures, including suspended beams and patterned lines with dimensions on the nm-scale.

Index Terms—3D silicon patterning, 3D Si printing, focused ion beam (FIB) writing, ion implantation, microstructures, nanostructures, MEMS, NEMS

I. INTRODUCTION

Silicon (Si) is a very attractive material for micro- and nanoscale devices due to its excellent mechanical, optical and electrical properties [1]. Conventional Si machining techniques, including lithography and Si etching, allow cost-efficient implementation of simple suspended three dimensional (3D) Si structures. To implement more complex 3D Si structures, elaborate process schemes involving a multitude of different processes are required. Additive layer-by-layer manufacturing techniques have been developed in which 3D structures are formed by adding several patterned layers on top of each other, using iterative processes to implement 3D structures in polymers or metals [2–10]. The possibility for additive layer-by-layer fabrication of arbitrarily shaped 3D Si structures could provide a wealth of opportunities for new types of nanophotonics, nanoelectromechanical systems (NEMS) and microelectromechanical systems (MEMS).

Examples of additive layer-by-layer manufacturing include stereolithography [2, 3], solid ground curing [2], selective laser sintering [2, 8], 3D inkjet printing [2], fused deposition modeling [2, 8–17] and laminated object modeling [2, 18, 19]. In direct laser writing, solid ground curing and stereolithography 3D, polymer structures are fabricated by a local exposure of a photosensitive polymer with light and subsequent selective dissolution of the

polymer [2–6]. In 3D inkjet printing and similar techniques, 3D structures are formed by printing functional inks, often in combination with supporting sacrificial inks that are subsequently selectively dissolved [2, 8]. Typical materials used in 3D inkjet printing include polymers, waxes and inks filled with e.g. metal, carbon or ceramics. Laser-beam [11–13], focused ion-beam (FIB) [14–16] electron-beam [14] and proton-beam [17] assisted deposition are other techniques for additive fabrication of 3D structures. Focused ion-beam, electron-beam and proton-beam assisted deposition methods can achieve structural dimensions as small as a couple of tens of nm. However, the fabrication of suspended Si structures has not been shown with these techniques. In [18, 20] methods for the layer-by-layer fabrication of 3D polycrystalline Si structures with dimensions below 1 μm using conventional semiconductor manufacturing processes have been demonstrated. The applied processes are combinations of poly-crystalline Si deposition, SiO₂ deposition, photolithography, reactive ion etching, chemical-mechanical polishing (CMP) and selective etching of the sacrificial layer. These approaches require a large number of different processing and photolithography steps that cannot be easily automated. Transfer printing of pre-patterned Si membranes (laminated object modeling) is another approach to realize 3D Si structures with dimensions in the micrometer-range [19, 21]. It is however difficult to efficiently automate these processes for devices with dimensions in the nm-scale.

In this paper, we report a method for additive layer-by-layer fabrication of arbitrarily shaped 3D Si micro- and nanostructures [22]. This method is schematically illustrated in Figure 1, and involves an iterative process of defining a pattern with implanted Ga⁺ ions in Si layers using FIB writing (Figure 1, steps 1 and 3), followed by chemical vapor deposition of 40–70 nm thick Si layers (Figure 1, step 2). The local implantation of Ga⁺ ions into Si causes an etch selectivity towards various wet and dry etching techniques [23–25]. By repeating steps 2 and 3, 3D structures are defined within the deposited Si layers. The defined 3D Si structures are then formed by selective free-etching (Figure 1,

step 4) in a final patterning step. To demonstrate the method, both 2- and 3-layer Si structures were fabricated. These structures comprise suspended beams and narrow patterned line structures with dimensions in the nm-scale.

II. FABRICATION

The test structures, shown in Figure 2 - 4, were fabricated on a 100 mm diameter p-type, $0.005 - 0.020 \Omega\text{cm}$ Si (100) wafer. An iterative process of defining a pattern with implanted gallium ions (Ga^+) in a Si layer using FIB writing (Figure 1, steps 1 and 3) was used. This was followed by chemical vapor deposition of a Si layer (Figure 1, step 2) and pattern definition in the deposited Si layer using FIB writing. This process is repeated for as many layers as desired to define the Si structures. A final wet etch releases the structures. Based on that approach, Si structures consisting of 2-layers (Figure 2) and 3-layers (Figure 3), as well as Si structures that determine the maximal resolution of the ion implantation (Figure 4), were fabricated.

In the ion implantation, an area dose of $10 \text{ pC}/\mu\text{m}^2$ of Ga^+ ions was used, at an acceleration voltage of 30 kV, using a Nova 600 NanoLab from FEI (the Netherlands). Before each Si layer deposition, the Si wafer was cleaned by the following steps: 10 s dip in 5% hydrofluoric acid (HF), 5 min wash in deionized (DI) water, 5 min etch in hot $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ 3:1, 5 min DI wash, 10 s dip in 5% HF, and 5 min DI wash. The Si layers were grown from a disilane (Si_2H_6) precursor, at a pressure of 2600 Pa and a temperature of 635°C , using an Epsilon 2000 single wafer epitaxy tool from ASM International N.V. (the Netherlands). During the wafer loading procedure, the wafers were exposed to temperature steps of 850°C for 13 s, followed by 725°C for 120 s. After the final implantation, the wafers were treated with a rapid thermal anneal in an argon atmosphere at 650°C for 30 s. The structures were formed by a final etch in KOH. First, a 3 s dip in 5% HF was done to remove the native silicon oxide, and then the wafers were etched in 30% KOH at 36°C

for 4 to 8 min, depending on the targeted under-etch. Finally, the wafers were washed in DI water for 3 min and dried with N_2 .

III. EXPERIMENTAL RESULTS AND DISCUSSION

The 2-layer structures shown in Figure 2 consist of four raised Si platforms, with cantilevers extending out from the platforms. Indicated in Figure 2 a) is an enlarged area shown in Figure 2 b) and the line height profiles of figure 2 d). The suspended beams, shown in in Figure 2 b), have a width of 500 nm, a thickness of 40 nm and a length of up to $4 \mu\text{m}$. The KOH etch has freed the narrow beam, while the wide beam is still supported. Given the high selectivity of the KOH etch (>1000), the wide beam could be freed by extending the etch time. The beams show no signs of stress, and are flat after the free-etch. Figure 2 c) and d) show the height profile of the complete structure, as measured by white light interferometry (Wyko NT9300 from Veeco Instruments Inc. , USA).

The 3-layer structure shown in Figure 3 was fabricated by three implantation steps and two Si deposition steps, performed according to the aforementioned fabrication procedure. The base substrate was a (100) Si substrate (p-type, $14 - 22 \Omega\text{cm}$), and the first layer was patterned in the Si substrate. Thereafter, two Si deposition steps with subsequent FIB implantation steps was performed. The structures demonstrate the different overlaps possible with three layers.

To investigate the limits of the smallest feature size that can be implemented, resolution test structures with narrow line patterns were written in a deposited Si layer. Figure 4 shows Si lines that are 33 nm, 65 nm and 130 nm wide. The results from these resolution test structures clearly demonstrate the potential of the method for fabricating 3D Si devices with dimensions on the nm-scale.

Fig. 1. The process scheme for 3D-patterning of arbitrarily shaped Si micro- and nanostructures, using focused ion beam writing, Si deposition, and selective Si etching in KOH.

Fig. 2. a) An SEM image of the fabricated 2-layer structures. Indicated in the image are the enlarged areas shown in b) and the line height profiles in d). b) An enlarged view of two cantilever beams. The narrower beam is 500 nm wide, and the wider one 2 μ m. The KOH etch has freed the narrow beam, while the wide beam is still supported. c) The height profile of the complete structure, as measured with white light interferometry. d) Height profile along a cantilever beam.

Fig. 3. An SEM image of 3-layer structures, fabricated by three Ga^+ ion implantation steps, and two Si deposition steps, followed by a final KOH release etch.

Fig. 4. An SEM image of lines of widths down to 33 nm, patterned in a deposited Si layer.

IV. CONCLUSION

A straightforward additive layer-by-layer method for the fabrication of 3D Si micro- and nanostructures is reported. We have demonstrated the method by fabricating suspended Si beams with sub-micrometer dimensions, and patterned lines with dimensions on the nanometer scale, in 2- and 3-layer processes. If it is possible to implement Si CVD and FIB writing as switched processes in a single automated tool, this could enable printing of 3D Si micro- and nanostructures directly from 3D CAD models. Thus, the proposed technology could change, and greatly simplify, the fabrication of many Si micro and nano devices, without requiring a fully equipped semiconductor cleanroom.

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