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Analysis of Exponentially Decaying Pulse Shape DACs in Continuous-Time Sigma-Delta Modulators. 
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Analysis of Exponentially Decaying Pulse Shape DACs in Continuous-Time Sigma-Delta Modulators

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Abstract—The performance of continuous-time (CT) sigma-delta (ΣΔ) modulators is severely degraded by the clock jitter induced timing variation in their feedback digital-to-analog converters (DACs). To mitigate this non-ideality, jitter sensitivity reduction techniques that employ exponentially decaying pulse shape DACs have been recently reported. In this paper, exponentially decaying DACs are investigated and generalized expressions are derived. In addition, another exponentially decaying DAC is proposed, which can potentially achieve both good jitter immunity and amplitude efficiency. To validate the theoretical results, the proposed DAC, together with other exponentially decaying DACs, are employed in a 2nd order 1-bit CT ΣΔ modulator test case and evaluated through behavioral simulations.

I. INTRODUCTION

During the past decade, CT ΣΔ ADCs have received a growing interest due to their superior speed/power trade-off over their discrete-time (DT) counterparts [1]. However, one critical non-ideality limiting their performance is the high sensitivity to the clock jitter in the feedback DACs. Clock jitter introduces timing variation to the feedback DAC and consequently induces a statistical integration error. This error, in return, increases the noise floor and, hence, degrades the modulator’s signal-to-noise-ratio (SNDR). One way to reduce this error is through minimizing the amplitude of the tail feedback pulse, as the amount of integration error depends on the pulse shape of the DAC’s feedback signal. Following this strategy, feedback DACs that employ exponentially decaying pulse shape have been proposed in literature. Instead of using a traditional rectangular pulse shape, e.g., the non-return-to-zero (NRZ) feedback (Fig. 1(a)), [2] proposes an exponentially decreasing feedback pulse (Fig. 1(b)) implemented by the switched-capacitor-resistor (SCR) architecture. However, the DAC feedback peak current is largely increased so as to transfer the same amount of charge in one clock period. Consequently, the SCR feedback imposes stringent speed requirements on the 1st integrator. Based on the SCR DAC architecture, several follow-up works have been reported lately: the switched-capacitor switched-resistor (SCSR) [3] (Fig. 1(c)), the full clock period SCR (FSCR) [4] (Fig. 1(d)), and the dual SCR (DSCR) [5] (Fig. 1(e)) architectures. Among them, [3] and [5] focus on relaxing the slew-rate requirement of the amplifier in the 1st integrator; while [4] mainly aims to further reduce the jitter induced noise. In this paper, a full clock period SCSR (FSCSR) DAC feedback waveform is proposed, as illustrated in Fig. 1(f). The proposed waveform is shaped in a way that can transfer feedback charge during the whole clock period $T_S$ while starts decaying after the half clock period. By doing so, this FSCSR DAC can potentially achieve similar jitter immunity performance as the traditional SCR without significantly increasing the DAC output peak current amplitude. It is worth to mention that even though only the single-bit case is treated here, the proposed waveform can be easily applied to multi-bit DACs.

II. FSCSR DAC OPERATION

Fig. 2 depicts one possible implementation of the proposed FSCSR feedback DAC, assuming a $G_{in}$-C based integrator. As it can be appreciated from the figure, the DAC has two replicated circuit cells, which are time-interleaved in order to achieve full clock period charge transferring. The operation of this DAC can be divided into three phases controlled by $\Phi_1$, $\Phi_2$, $\Phi_3$ and $\Phi_4$. For simplicity, the operation of the two cells will be explained together in the fashion of “Cell I (Cell II)”. In the precharge phase, which occurs during $\Phi_1$ ($\Phi_2$), the bottom
In the exponential discharge phase, which occurs during ended jitter induced charge error $\epsilon_j$, differential output, DAC $V_{\text{DAC}}$ factor that refers to the number of jittered edges in one $\gamma T_S$.

de 

is the clock period, $\sigma_j$ is the normalized peak amplitude of each DAC pulse, while $P$ denotes the pulse transition amplitude factor which equals 2 for NRZ and 1 for all the others. Also for NRZ, $\gamma = \beta$ and $\tau \to \infty$. Then, $\sigma_j^2$ can be derived as:

$$
\sigma_j^2 = \int_{-\infty}^{+\infty} [(\epsilon_j - E[\epsilon_j])^2 f(t)] dt
$$

where $f(t)$ is the probability density function (PDF) of $t_j$, and $E[\epsilon_j]$ is the expected value of $\epsilon_j$. It can be appreciated from (4) that the single-ended jitter induced error of SCR, DSCR, SCSR and FSCSR DACs are essentially equal as long as the decoding starts at the same time instant $\gamma$ with the same constant $\tau$.

Recalling from (1), $\sigma_j^2$ can be used to calculate $N_{\sigma_j}$ by relating it to $T_S$ and the corresponding activity factor $A$. Moreover, to calculate the jitter induced in-band-noise, $IBN_{\sigma_j}$, the noise entering in the outermost branch DAC, $N_{\sigma_j}$, needs to be further referred to the modulator input.

$$
IBN_{\sigma_j} \approx \frac{a_1^2 N_{\sigma_j}}{b_1^2 \text{OSR}} = \left(\frac{a_1}{b_1}\right)^2 \frac{\sigma_j^2 \cdot A}{T_S^2 \text{OSR}},
$$

where the oversampling ratio (OSR) and $T_S$ are equal for all the DACs. $A \approx 0.7$ for NRZ and $A = 2$ for all the other DACs. $a_1$ is the feedback coefficient of the outermost DAC and $b_1$ is the feedforward coefficient from the modulator input. Here, all DAC pulses are assumed to transfer the same amount of feedback charge per clock period. We can appreciate from (5) that the jitter induced in-band-noise (IBN) of each DAC feedback is not only dependent on its charge error variance but also on its feedback coefficient. For better comparison, two performance metrics are applied in this work, namely amplitude efficiency $[3]$, $\eta_a$, and jitter immunity, $\eta_j$. 

The single-ended jitter induced charge error $\epsilon_{j,SE}$, which applies to all the DACs in Fig. 1, can be expressed by:

$$
\epsilon_{j,SE} = \frac{\gamma}{T_S} \int_{-T_S/2}^{T_S/2} r_{\text{DAC}}(t) dt + \sum_{n} \frac{\beta}{T_S} \int_{nT_S}^{(n+1)T_S} r_{\text{DAC}}(t) dt,
$$

where $r_{\text{DAC}}(t)$ is the DAC feedback impulse response, $\alpha$ and $\beta$ are the normalized starting and ending time instants of the corresponding DAC pulse, and $\gamma$ is the normalized time instant when the exponential decaying begins. In this calculation, $\gamma$ is assumed as jitter free. This assumption will be further discussed in section III. By applying a 2nd order Taylor expansion, (2) can be solved as:

$$
\epsilon_{j,SE} = -P \cdot I_{\text{DAC}} \cdot \tau \left( e^{(\beta - \gamma) T_S} \cdot e^{-\gamma T_S} - e^{(\beta - \gamma) T_S} \right)
$$

As introduced in section I, the most critical impact of clock jitter on CT $\Sigma\Delta$ modulators is the timing variation in the DAC feedback pulse. The outermost branch DAC will have the most detrimental effect on the modulator’s performance, as no noise shaping will take place. The impact of jitter can be further divided into two categories: 1) a random change in pulse position, and 2) a random change in pulse width. It has been shown that the latter one is more critical than the former one [7], thus, this work will focus on analyzing only the pulse width (PW) jitter. The PW jitter induced sampling uncertainty $t_j$ can be assumed as zero mean Gaussian distributed with variance $\sigma_j^2$. The PW jitter induced noise $N_{\sigma_j}$ that enters in the outermost branch DAC (before its scaling coefficient) can be expressed as [6]:

$$
N_{\sigma_j} = \frac{\sigma_j^2 \cdot A}{T_S^2},
$$

Fig. 2. Schematic and timing diagram of the FSCSR DAC.
The amplitude efficiency, $\eta_a$, measures the ratio of the charge transferred over one clock period between a NRZ pulse and an exponentially decaying pulse:

$$\eta_a = \frac{H_{\text{NRZ}}(z)}{H_{\text{exp}}(z)} = \frac{a_{1,\text{exp}}}{a_{1,\text{NRZ}}},$$  

(6)

where $a_{1,\text{exp}}$ denotes the feedback coefficient of each exponentially decaying DAC, and $a_{1,\text{NRZ}}$ denotes the feedback coefficient of the NRZ DAC. $H_{\text{exp}}(z)$ and $H_{\text{NRZ}}(z)$ are their DT equivalent transfer functions which are derived using the impulse-invariant transformation [1]. The DT equivalent transfer functions of all the DACs can be generalized by a single expression as:

$$H(z) = -\frac{(\alpha + \tau e^{-\frac{(\beta - \gamma)z}{\tau}} - \gamma - \tau)R}{z - 1},$$  

(7)

where $R$ is the repeating factor which denotes the number of times the DAC pulse waveform is repeated over one period. $R = 2$ for the DSCR pulse and $R = 1$ for all the others. Given $H(z)$, the amplitude efficiency of each DAC can be obtained by using (6). Naturally, $\eta_{a, \text{NRZ}} = 1$. The resultant $\eta_a$ for all the other DACs can be generalized as:

$$\eta_{a, \text{exp}} = -\frac{1}{(\alpha + \tau e^{-\frac{(\beta - \gamma)z}{\tau}} - \gamma - \tau)R}.$$  

(8)

The jitter immunity, $\eta_j$, measures how much the jitter sensitivity is reduced in an exponentially decaying pulse as compared to a NRZ pulse:

$$\eta_j = 10 \log_{10} \left( \frac{\text{IBN}_{\sigma_j, \text{exp}}}{\text{IBN}_{\sigma_j, \text{NRZ}}} \right),$$  

(9)

where $\text{IBN}_{\sigma_j, \text{exp}}$ denotes the jitter induced IBN of each exponentially decaying DAC, while $\text{IBN}_{\sigma_j, \text{NRZ}}$ denotes the jitter induced IBN of the NRZ DAC. It can be seen from (6) that $\eta_a$ is linearly related to $a_{1,\text{exp}}$. By combining (4), (5) and (6), an alternative way to express IBN$_{\sigma_j}$ can be found:

$$\text{IBN}_{\sigma_j} = \eta_a \frac{A}{\text{OSR}} \frac{T^2_{\text{DAC}} (e^{-\frac{(\beta - \gamma)T}{\tau}})^2 \sigma_j^2}{T_S^2}.$$  

(10)

Given IBN$_{\sigma_j}$, the jitter immunity of each DAC can be obtained from (9). Naturally, $\eta_{j, \text{NRZ}} = 0$ dB. The resultant $\eta_j$ for all the other DACs can hence be generalized as:

$$\eta_{j, \text{exp}} = -\frac{5}{7} \eta_a \frac{A}{\text{OSR}} \frac{T^2_{\text{DAC}} (e^{-\frac{(\beta - \gamma)T}{\tau}})^2 \sigma_j^2}{T_S^2}.$$  

(11)

In Fig. 3 and Fig. 4, the amplitude efficiency $\eta_a$ given by (8) and the jitter immunity $\eta_j$ given by (11) are plotted as functions of normalized $\tau$. For a fair comparison, $\gamma$ is fixed as 0.5 $T_S$ for SCR, SCSR and FSCSR. Also noted that here $\gamma = 0$ for FSCR and DSCR, $\alpha = 0.25 T_S$ for SCSR, $\beta = 0.5 T_S$ for DSCR. As it can be appreciated from Fig. 3, the proposed FSCSR pulse shape has better amplitude efficiency than any other exponentially decaying pulse shapes, especially the SCR and FSCR. On the other hand, Fig. 4 suggests that the FSCSR DAC also has better jitter immunity compared to the other exponentially decaying DACs, except the FSCR.

IV. SIMULATION RESULTS

To validate the theoretical results, the DACs are employed in a 3rd order 1-bit CT $\Sigma\Delta$ modulator and behavioral simulations are performed using Matlab/Simulink. The modulator has an OSR = 80 and its topology is illustrated in Fig. 5. The CT loop filter coefficients $c_1$, $c_2$ and $c_3$ are derived for different feedback DACs by using the impulse-invariant transformation. In order to obtain a jitter limited performance, apart from the white clock jitter, other modulator non-idealities such as excess loop delay and process variation are excluded in the model.

The CT $\Sigma\Delta$ modulator with different feedback DACs is simulated under clock jitter influence. The amount of jitter is varied in the range of $\sigma_j = 0.1 - 10\% T_S$. The testing
signal is at -6 dBFS and its frequency is around $f_B/4$. Since the time constant $\tau$ directly determines the jitter sensitivity [2][3], which is also indicated by Fig. 4, a moderate value of $\tau = 0.2 T_S$ is selected in this test case. The simulated SNDR performance of the modulator employing different feedback DACs is shown in Fig. 6. Since for each run the SNDR can be slightly different due to randomly generated jitter, each data point in this plot is averaged from 10 runs of simulations. In addition, the averaged data points are presented together with their standard deviation using error bars. Fig. 6 confirms our observation from theoretical analysis that the modulator employing a FSCSR DAC is less sensitive to clock jitter than any other DACs apart from the FSCR. However, this superior jitter immunity is obtained under the assumption that only starting and ending time instants ($\alpha$ and $\beta$) of the pulse are jitter affected. The jitter effect on $\gamma$ is rarely treated in the CT $\Sigma\Delta$ literature. To the best of our knowledge, only in [3][8] this issue is studied which shows that large delay line jitter can be allowed without significantly decreasing the SNDR. Nevertheless, the readers should be aware that this insensitivity to the delay line jitter, $\gamma$, can be validated by both simulation and measurement results, only in their particular case. As the jitter in $\gamma$ is strongly implementation dependent, special attention is needed in implementing the FSCSR DACs.

In order to investigate the amplitude efficiency, the feedback waveform of each DAC at the $1^{st}$ integrator’s input is plotted and compared in Fig. 7. For better illustration, the modulator is simulated with a jitter free clock. The time constant $\tau$ is again selected as $0.2 T_S$, since $\tau$ has also significant impact on the amplitude efficiency. The simulation results confirm the theoretical results by showing that the proposed FSCSR DAC only slightly increases the feedback peak amplitude compared to the NRZ, while the others have non-trivial increased amplitude. As the slew rate is highly circuit implementation dependent [6], the behavioral simulation used in this study cannot give accurate results in the slew rate estimation. However, it has been shown that reducing the peak amplitude of feedback DAC can consequently reduce the slew rate requirements for the integrating amplifiers [2][3]. This indicates that the proposed FSCSR DAC can potentially relax the stringent design requirements on the $1^{st}$ integrator compared with other exponentially decaying DACs.

V. CONCLUSION

In this paper, various exponentially decaying feedback DACs used in CT $\Sigma\Delta$ modulators have been thoroughly analyzed. All the SCR-based DACs have been generalized in terms of jitter induced charge error and its variance, DT transfer function, IBN, and two performance metrics, i.e., amplitude efficiency and jitter immunity. Moreover, a FSCSR feedback DAC has been proposed whose advantage in both metrics has been demonstrated mathematically and through behavioral simulations.

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