Two-step continuous-time incremental sigma-delta ADC

S. Tao, S. Rodriguez and A. Rusu

A two-step continuous-time (CT) incremental sigma-delta ($\Sigma\Delta$) ADC, which enhances the performance of conventional CT incremental $\Sigma\Delta$ ADCs, is proposed. By pipelining two second-order CT incremental $\Sigma\Delta$ ADCs, the proposed two-step architecture can achieve high resolution without sacrificing the conversion rate. Compared to other alternatives, the two-step CT incremental $\Sigma\Delta$ ADC exhibits the freedom of adjusting its accuracy and speed independently while features quite relaxed circuit specifications.

Introduction: Incremental sigma-delta ($\Sigma\Delta$) ADCs, which reset their memory elements before each conversion, can offer sample-by-sample conversion as Nyquist-rate ADCs [1]. The feature of one-to-one mapping between input and output makes them suitable for processing multiplexed input signals. The $\Sigma\Delta$ ADC designs are dominated by discrete-time implementations. Nevertheless, continuous-time (CT) $\Sigma\Delta$ ADCs have been recently explored, taking advantage of the relaxed settling and bandwidth requirements when using CT loop filters (LFs). In literature, alternative solutions to first-order CT incremental $\Sigma\Delta$ ADCs have been proposed, e.g., the high-order topology [2] and the extended range (ER) [3] architecture. In this letter, a two-step CT $\Sigma\Delta$ ADC is proposed as a new alternative to extend the resolution. Compared to high-order topologies, it requires less coefficient scaling to maintain stability, which indicates better power efficiency. Compared to ER architectures, it induces no extra clock cycles for the second ADC, which avoids the resolution-speed tradeoff.

Proposed two-step CT $\Sigma\Delta$ ADC: Fig. 1 depicts the proposed ADC architecture together with its timing diagram. To handle multi-channel inputs, time-division multiplexing is performed for the input signals through a multiplexer (MUX). At the beginning of each conversion, one of the input channels is selected, sampled and held by SH_1 for the entire conversion period T_S . Then, two second-order CT $\Sigma\Delta$ ADCs are initially reset and then process the sample in a two-step pipelining fashion [4]: one for coarse conversion and the other for fine conversion.

During ϕ_1 , the CT $\Sigma\Delta$ modulator in the 1st step processes $U(z)$ with an internal oversampling clock, Mf_S . At the end of this coarse conversion step, the most significant bits (MSBs), N_1 , are extracted by the digital filter. The modulator and digital filter are then reset, and an analog residue voltage V_{res} is sampled and held by SH_2 with f_S . During ϕ_2 , the sampled residue voltage $V_{res}(M)$ is passed to the CT $\Sigma\Delta$ modulator in the 2nd step, and oversampled again with Mf_S . At the end of this fine conversion step, the least significant bits (LSBs), N_2 , are extracted and the modulator and digital filter are reset. By digitally combining the MSBs and LSBs from the two conversion steps, a resolution of $N_1 + N_2$ can be ideally achieved. Due to the two-step pipelining operation, the coarse conversion can start processing the next sample immediately after the fine conversion starts. The overall sampling rate of the two-step ADC is thus limited by M , which is determined by the resolution of a single conversion step.

The second-order CT $\Sigma\Delta$ modulator employed in each conversion step is shown in Fig. 2. Since this modulator topology processes only the quantisation noise, it alleviates the issue of the wide spread of integrator coefficients when employing CT LFs. Additionally, the quantisation noise is readily available at the 2nd integrator's output and hence no subtraction is needed. A single-bit implementation is chosen to minimise the complexity of both the feedback DAC and the digital filter. The non-return-to-zero (NRZ) coding scheme is selected for the DAC considering the trade-off in timing error suppression and power consumption.

The 2nd integrator's output, X_2 , can be derived through time-domain analysis [1]. After M clock cycles, X_2 can be expressed as:

$$X_2(M) = b_1 c_1 c_2 \frac{M(M-1)}{2} u - a_1 c_1 c_2 \sum_{j=0}^{M-1} \sum_{i=0}^{j-1} z(i) \quad (1)$$

where u is the amplitude of the input sample, and $z(i) = v(i)V_{ref}$ is the DAC output at the end of the i^{th} clock cycle. Here, v denotes the modulator output, and V_{ref} denotes the DAC's reference voltage. Since the input u is constant during each conversion, X_2 , expressed by (1), can be theoretically bounded between $\pm V_{ref}$ [1]. The minimum number of clock cycles, M ,

Fig. 1 Proposed two-step CT $\Sigma\Delta$ ADC for multiplexed inputs: architecture and its timing diagram

Fig. 2 Block diagram of the second-order CT $\Sigma\Delta$ modulator used in both the coarse and fine conversions

required by a target resolution, N_{bits} , can be estimated as:

$$M = 2^{0.5[N_{bits} + \log_2(b_1 c_1 c_2) + \log_2(0.5 u_{max})]} \quad (2)$$

where u_{max} is used to limit the input to a fraction of V_{ref} . The theoretical signal-to-quantisation noise ratio (SQNR) of the two-step CT $\Sigma\Delta$ ADC, $SQNR_{2step}$, when combining the digitised results from the coarse conversion (s_1) and the fine conversion (s_2), can be derived as:

$$\begin{aligned} SQNR_{2step}[dB] &= SQNR_{s1}[dB] + SQNR_{s2}[dB] \\ &= \left| 20 \log_{10} \left[\frac{2V_{ref}}{u_{max} V_{ref}} \frac{1}{M(M-1)} \right] \right|_{s1} \\ &\quad + \left| 20 \log_{10} \left[\frac{2V_{ref}}{V_{res,peak}} \frac{1}{M(M-1)} \right] \right|_{s2} \end{aligned} \quad (3)$$

where $V_{res,peak}$ denotes the peak amplitude of the residue voltage.

The digital filter (DF) used in each conversion step can be obtained by setting the quantisation error of the ADC (in each conversion step) equal to the magnitude of the discrete-time equivalent of X_2 [2]. By applying the impulse-invariant transformation, the digital filter transfer function, $H_{DF}(z)$, can be derived as:

$$H_{DF}(z) = \left[\frac{z^{-2}}{(1-z^{-1})^2} + \frac{1}{2} \frac{z^{-1}}{1-z^{-1}} \right] \frac{2}{M^2} \quad (4)$$

The presence of circuit non-idealities, however, would induce mismatch between the analog and digital transfer function, which inevitably leads to significant performance degradation of the two-step ADC. To counteract this issue, an optimised digital filter can be employed in the 1st step ADC [3]. The basic idea is to employ optimisation algorithms to refine the signal-to-noise and distortion ratio (SNDR). By using the theoretical DF transfer function, i.e., (4) in this case, as a reference, its coefficients are recalculated for optimised SNDR under introduced circuit non-idealities.

Simulation results: The proposed two-step CT $\Sigma\Delta$ ADC is characterised by applying a 200Hz sinusoidal signal. To accommodate the bandwidth of the multiplexed input signal from 16 channels, the sample-and-hold frequency at SH_1 and SH_2 is determined as $f_S = 8kHz$ and the bandwidth of the ADC is $f_B = 4kHz$. Fig. 3 presents the simulated SQNR of the 1st step ADC and the two-step ADC versus the number of clock cycles. Good agreement is achieved between simulation results and theoretical estimations, i.e., $SQNR_{s1}$ and $SQNR_{2step}$ calculated using (3). According to (2), $M \approx 30$ is adequate to achieve an 8-bit ideal resolution in each step. To leave enough margin for compensating the effect of circuit noise and non-idealities, $M = 40$ is selected when targeting an effective number of bits (ENOB) of 14-bit in this test-case.

Fig. 3 Simulated and estimated SQNR vs. M : second-order CT $\Sigma\Delta$ ADC in the 1st step ($s1$), and two-step CT $\Sigma\Delta$ ADC (2step)

Fig. 4 shows the simulated power spectral density (PSD) under ideal conditions and in the presence of circuit noise and non-idealities, respectively. As shown in Fig. 4a, the proposed ADC can achieve a SQNR of 105 dB. As shown in Fig. 4b, when applying an optimised digital filter, the proposed ADC can achieve a SNDR of 85.6 dB, while imposing very relaxed requirements on circuit implementation. The introduced noise and non-idealities are specified in Table 1, where $f_{OS} = Mf_S = 320kHz$ and $T_{OS} = 1/f_{OS}$ are the frequency and period of the internal oversampling clock. Similar to cascaded systems, the ADC in the 1st step is limiting the overall system performance. Thus, as it is shown in Table 1, the circuit specifications for the ADC in the 2nd step are further relaxed. It is worth mentioning that the optimised filter can effectively handle mainly the error induced by the op-amp's finite gain-bandwidth (GBW) product and passive devices' process variations [3]. These two specifications are the main indicators for the circuit power consumption. It is also worth to notice that the requirements on timing errors, i.e., excess-loop-delay (ELD) and clock jitter, are easily achievable using standard circuits and clock generation techniques, due to the relatively low oversampling frequency.

Fig. 4 Simulated PSD of the 14-bit two-step CT $\Sigma\Delta$ ADC with $P_{sig} = -3.5$ dBFS, $f_{sig} \approx 200$ Hz, $f_B = 4$ kHz, and $N_{FFT} = 2048$

a ideal conditions

b with noise and non-idealities while using an optimised digital filter

Table 1: Noise and non-idealities specifications for ENOB = 14-bit

Noise & Nonidealities	CT $\Sigma\Delta$ ADC in step 1	CT $\Sigma\Delta$ ADC in step 2
Circuit Noise	$1\mu V_{rms}$ (input-referred)	$9\mu V_{rms}$ (input-referred)
Finite GBW	int1: f_{OS} , int2: $0.5f_{OS}$	int1: f_{OS} , int2: $0.5f_{OS}$
RC Variation, Δ_{RC}	<10% (both integrators)	<20% (both integrators)
Clock Jitter, σ_j	<0.01% T_{OS}	<0.1% T_{OS}
ELD, τ_d	<1% T_{OS}	<10% T_{OS}

Conclusion: A two-step ADC architecture, consisting of two second-order CT $\Sigma\Delta$ ADCs in a pipeline configuration, has been proposed. This architecture showcases the advantage of achieving high resolution and high speed simultaneously, which has been demonstrated by both analytical analysis and behavioural simulations. It has been also shown that if an optimised digital filter is employed, the proposed ADC is capable of greatly relaxing the circuit specifications at the same time achieving high resolution. This demonstrates its potential for low-power high resolution multi-channel applications.

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References

- Markus, J., Silva, J., and Temes, G.C.: 'Theory and applications of incremental $\Sigma\Delta$ converters', *IEEE Trans. Circuits Syst. I.*, 2004, **51**, (4), pp. 678-690
- Garcia, J., Rodriguez, S., and Rusu, A.: 'A Low-Power CT Incremental 3rd Order Sigma-Delta ADC for Biosensor Applications', *IEEE Trans. Circuits Syst. I.*, 2013, **60**, (1), 2013, pp. 25-36
- Garcia, J., Rodriguez, S., and Rusu, A.: 'On Continuous-Time Incremental Sigma-Delta ADCs with Extended Range', *IEEE Trans. Instrum. Meas.*, 2013, **62**, (1), pp. 60-70
- Razavi, B.: 'Principles of Data Conversion System Design' (Wiley-IEEE Press, 1995)