ROYAL INSTITUTE
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Heterogeneous material integration for MEMS

FREDRIK FORSBERG

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Front cover pictures:
The front cover shows an array of 17 μm pitch microbolometers and an array of 460 $\times$ 460 μm^2 silicon dies.

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Abstract

This thesis describes heterogeneous integration methods for the fabrication of microelectromechanical systems (MEMS). Most MEMS devices reuse the fabrication techniques that are found in the microelectronics integrated circuit industry. This limits the selection of materials and processes that are feasible for the realization of MEMS devices. Heterogeneous integration methods, on the other hand, consist of the separate pre-fabrication of sub-components followed by an assembly step. The pre-fabrication of subcomponents opens up for a wider selection of fabrication technologies and thus potentially better performing and more optimized devices. The first part of the thesis is focused upon an adhesive wafer-level layer transfer method to fabricate resistive microbolometer-based long-wavelength infrared focal plane arrays. This is realized by a CMOS-compatible transfer of monocrystalline silicon with epitaxially grown silicon-germanium quantum wells. Heterogeneous transfer methods are also used for the realization of filtering devices, integration of distributed small dies onto larger wafer formats and to fabricate a graphene-based pressure sensor. The filtering devices consist of very fragile nano-porous membranes that with the presented dry adhesive methods can be transferred without clogging or breaking. Pick-and-place methods for the massive transfer of small dies between different wafer formats are limited by time and die size-considerations. Our presented solution solves these problems by expanding a die array on a flexible tape, followed by adhesive wafer bonding to a target wafer. Furthermore, a gauge pressure sensor is realized by transferring a graphene monolayer grown on a copper foil to a micromachined target wafer with a silicon oxide interface layer. This device is used to extract the gauge factor of graphene. Adhesive bonding is an enabling technology for the presented heterogeneous integration techniques. A blister test method together with an experimental setup to characterize the bond energies between adhesives and bonded substrates is also presented.

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Contents

List of papers

The presented thesis is based on the following *international reviewed journal papers*:

1. *Heterogeneous 3D integration of 17 µm pitch Si/SiGe quantum well bolometer arrays for infrared imaging systems*
   F. Forsberg, A.C. Fischer, N. Roxhed, B. Samel, P Ericsson, G Stemme and F Niklaus
   Journal of Micromechanics and Microengineering, vol. 23, no. 4, pp. 045017, April 2013.

2. *Very large scale heterogeneous integration (VLSHI) and wafer-level vacuum packaging for infrared bolometer focal plane arrays*
   F. Forsberg, N. Roxhed, A.C. Fischer, B. Samel, P. Ericsson, N. Hoivik, A. Lapadatu, M. Bring, G. Kittilsland, G. Stemme and F. Niklaus
   Infrared Physics & Technology, vol. 60, pp. 251-259, Sep. 2013.

3. *Wafer bonding with nano-imprint resists as sacrificial adhesive for fabrication of silicon-on-integrated-circuit (SOIC) wafers in 3D integration of MEMS and ICs*
   F. Niklaus, A. Decharat, **F. Forsberg**, N. Roxhed, M. Lapisa, M. Populin, F. Zimmer, J. Lemm and G. Stemme
   Sensors and Actuators A: Physical, vol. 154, no. 1, pp. 180–186, Aug. 2009.

4. *A comparative study of the bonding energy in adhesive wafer bonding*
   F. Forsberg, F. Saharil, T. Haraldsson, N. Roxhed, G. Stemme, W. van der Wijngaart and F. Niklaus
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5. *Dry adhesive bonding of nanoporous inorganic membranes to microfluidic devices using the OSTE(+) dual-cure polymer*
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   Journal of Micromechanics and Microengineering, vol. 23, no. 2, pp. 025021, Jan. 2013.

6. *Batch Transfer of Radially Expanded Die Arrays for Heterogeneous Integration Using Different Wafer Sizes*
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   Journal of Microelectromechanical Systems, vol. 21, no. 5, pp. 1077-1083, Oct. 2012.

7. *Electromechanical Piezoresistive Sensing in Suspended Graphene Membranes*
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Nano Letters, vol. 13, no. 7, pp. 3237-3242, Jun. 2013.

The *contribution of Fredrik Forsberg* to the different publications:

1. All design, all fabrication, all experiments, major part of the writing
2. All bolometer design, all bolometer fabrication, all bolometer characterization, major part of the writing
3. Minor part of the writing and experiments
4. All design, all fabrication, all experiments, major part of the writing
5. Major part of the design, all fabrication, all experiments and major part of the writing
6. Part of the design, part of the fabrication, part of the experiments, part of the writing
7. Design and fabrication of measurement setup, part of experiments, part of the writing

Also, the work has been presented at the following *international reviewed conferences*:

8. *Far infrared low-cost uncooled bolometer for automotive use*
T. Kvisteroy, H. Jakobsen, C. Vieider, S. Wissmar, P. Ericsson, U. Halldin, F. Niklaus, **F. Forsberg**, G. Stemme, J.E. Källhammer, H. Pettersson, D. Eriksson, J. Franks, J. VanNylen, H. Vercammen and A. VanHulsel
11th International Forum on Advanced Microsystems for Automotive Applications, Berlin, Germany, Sep.5-6, 2007, pp.265–278

9. *High-performance quantum-well silicon-germanium bolometers using IC-compatible integration for low-cost infrared imagers*
   F. Forsberg, N. Roxhed, P. Ericsson, S. Wissmar, F. Niklaus and G. Stemme
   Solid-State Sensors, Actuators and Microsystems Conference, Denver, Colorado, USA, June 21–25, 2009, pp.2214–2217

10. *Low-cost uncooled microbolometers for thermal imaging*
    N. Roxhed, F. Niklaus, A.C. Fischer, **F. Forsberg**, L. Höglund, P. Ericsson, B. Samel, S. Wissmar, A. Elfving, T.I. Simonsen, K. Wang and N. Hoivik
    Conference on Optical Sensing and Detection, Brussels, Belgium, Apr. 12-15, 2010, pp.772611

11. *Heterogeneous Integration for Optical MEMS*
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12. *Heterogeneous Integration Technology for Combination of Different Wafer Sizes using an expandable handle substrate*
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15. *Use of Expandable Handle Substrate for Wafer-Level Transfer of Dies in Heterogeneous Integration and Packaging of MEMS*
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16. *Wafer-level heterogeneous 3D integration for MEMS and NEMS*
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Nomenclature

α-Si	Amorphous silicon
AlGe	Aluminum-Germanium
BCB	Benzocyclobutene
CMP	Chemical-mechanical polishing
Cu	Copper
D^*	Specific detectivity
DRIE	Deep reactive ion etching
FPA	Focal plane array
IC	Integrated circuit
LWIR	Long wavelength infrared
MEMS	Microelectromechanical systems
NEMS	Nanoelectromechanical systems
NEP	Noise-equivalent power
NETD	Noise-equivalent temperature difference
Ni	Nickel
PECVD	Plasma-enhanced chemical vapor deposition
poly-Si	Polycrystalline silicon
PSD	Power spectral density
QW	Quantum-well
SEM	Scanning electron microscopy

Si	Silicon
SiGe	Silicon-Germanium
SiN	Silicon nitride
SiO_x	Silicon oxide
SiP	System in package
Sn	Tin
SNR	Signal-to-noise ratio
SoB	System on board
SoC	System on board
SOI	Silicon on insulator
TCR	Temperature coefficent of resistance
TiW	Titanium Tungsten
VO_x	Vanadium oxide

Chapter 1

Introduction

The last two decades have seen an enormous increase in both the volume and the technological refinement of transducers and sensor systems. The underlying factor in this trend has been the development of microelectromechanical systems (MEMS), which are used to perform the essential new technological feats that have become part of our everyday experience. A modern smart phone, for example, contains accelerometers, gyroscopes, barometric sensors, microphones and oscillators that more often than not are constructed with MEMS microfabrication methods [1, 2]. Other areas where MEMS-based devices proliferate is in inkjet printheads, digital light processors and filters. Most MEMS-based sensors and transducers need to be combined with intelligence in the form of integrated circuits (IC) to be useful. The functionalities that are implemented include analog-to-digital conversion, amplification, filtering, information processing and as the communication interface between the MEMS component and the rest of the system. The increased integration of functionality in sensor systems has evolved the typical system layout from separate components on a printed circuit board (SoB), to integration of the system components (i.e IC and MEMS) into a package (SiP) and to complete integration of a system onto a single microchip (SoC). Figure 1.1 schematically exemplifies the technological development pattern. The technological frontier is pushed forward towards higher levels of integration by the need of smaller form factors, signal speed, lower cost and energy efficiency among others.

The most relevant fabrication methods for the realization of MEMS devices utilize the knowledge and tools that have been developed for the last fifty years for the fabrication of integrated electronic circuits. The strong influence from microelectronics is visible in both the use of materials and the fabrication cycle. Typically, silicon (Si) substrates are used as the base material. The fabrication cycle that follows consists of modifying the surface of the Si substrate. That can be achieved by, for example, doping the Si substrate, surface oxidation of Si or deposition of material on top of the Si substrate. The next step consists of selective removal of unwanted material in patterned areas of the substrate. This is done

by covering the substrate with a photo-sensitive polymer. The photo-sensitive polymer is then photolithographically patterned into the surface structure we want to imprint. The last step consist of a selective removal of unwanted material by etching in the areas not covered by the photo-sensitive polymer. The results of the cycle is a Si substrate with a patterned layer on top. By repeating the deposition-patterning-etching cycle, different material layers and patterns can be formed on top of the Si substrate, which in turn form the wanted devices. There are important differences in the fabrication of MEMS devices and microelectronic devices. The fabrication of ICs is essentially a planar 2D-process where only a very thin surface layer of the Si substrate is needed by the transistors that the ICs are based upon. Presently, typical gate lengths of the transistors used in modern digital ICs are 28 nanometers and below [3]. In comparison MEMS devices are huge. From µm-sized to mm-sized devices. Furthermore, MEMS devices are typically 3D-structures with considerably thicker material layers than what is used in microelectronics. This introduces the need for specialized MEMS fabrication methods. Technologies of considerable importance in MEMS fabrication is deep reactive-ion etching (DRIE) and wafer bonding, which in turn enables the etching of deep structures in Si and the attachment of different substrates to each other. These two fabrication technologies leverage the methods taken from microelectronics to enable the formation of true 3D-devices. Figure 1.2 summarizes the fabrication cycle. The interested reader is referred to dedicated texts for in depth descriptions of established microfabrication methods [4, 5].

Two different approaches are utilized in the fabrication of MEMS SoCs, where the sensor is integrated together with the IC on the same chip. The first method is based on *monolithic integration*. This approach follows closely the deposition-patterning-etch cycle described above where the needed material layers are deposited on top of the wafer substrate, followed by etching. The second method, *which is the focus of this thesis*, instead consists of the separate fabrication of sub-components of the system that in an integration step is attached to each other to form the finished devices. This approach is called *heterogeneous integration*.

1.1 Monolithic integration of MEMS and ICs

There are three ways in which ICs and MEMS can be monolithically integrated into SoCs [7]. The first method consists of processing the MEMS first and the ICs last, typically next to the sensor. The second method interleaves the fabrication of both the MEMS devices and the ICs by processing steps that are used in both fabrication schemes. The last method starts with fabricating the ICs first and the MEMS last, typically on top of the ICs in deposited material layers. All three platforms have been used commercially in the realization of microsystems.

Monolithic integration based on MEMS first processes allows for a very high thermal budget in the fabrication of the MEMS devices. Strict requirements are introduced to the MEMS fabrication since the later fabrication of ICs are made on

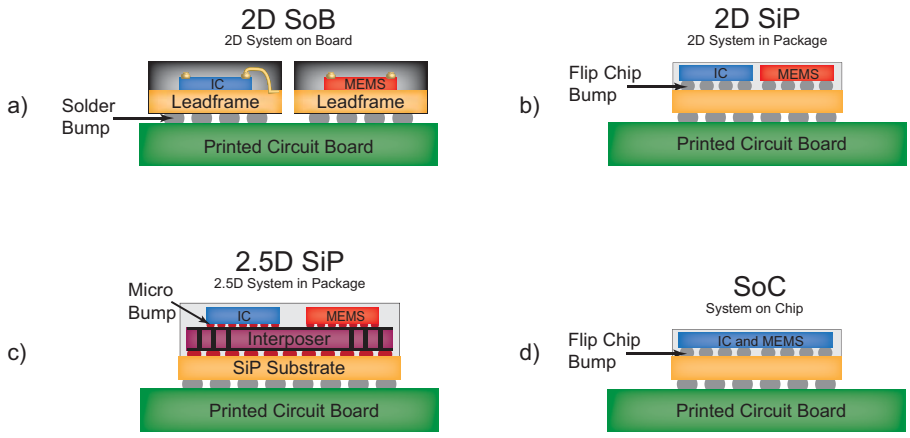

Figure 1.1: Depiction of common packaging approaches for the integration of multiple dies. a) System on Board. Separate electronic components on a circuit board. b) System in Package. Separate chips are integrated into a package. c) 2.5 D System in Package. Separate chips integrated on top of a Si interposer. d) System on Chip. Complete integration of different circuit functions into a chip. The image is a slightly adjusted version from [6].

the same wafer as the MEMS devices. These requirements are planarity, doping levels, device materials, among others [5]. Different technology platforms have been developed to implement MEMS first designs. The basic outline consists of sealing and burying MEMS structures in an appropriate manner. This is followed by chemical mechanical polishing (CMP) to planarize wafers for later IC processing modules. Electrical interconnects are used to electrically connect the finished MEMS sensor with the IC. Examples of MEMS first approaches are Bosch advanced porous silicon membrane (APSM) process to fabricate pressure sensors [8,9] and the SiTime fabrication platform [10] to create vacuum encapsulated micro-resonators. A simplified SiTime fabrication scheme is shown in Figure 1.3. In practise, the MEMS first approach for complete MEMS SoCs is only feasible for companies with access to IC semiconductor fabs that accept pre-processed wafers. This severely limits its attractiveness and neither Bosch nor SiTime (presently) use the possibility to monolithically integrate CMOS ICs with MEMS devices and instead utilize SiP solutions for their commercial products.

MEMS interleaved is defined as processes that have a combination of processing steps either before, after or in the middle of the CMOS IC fabrication. Examples of technology platforms consisting of both pre-CMOS and post-CMOS modules are

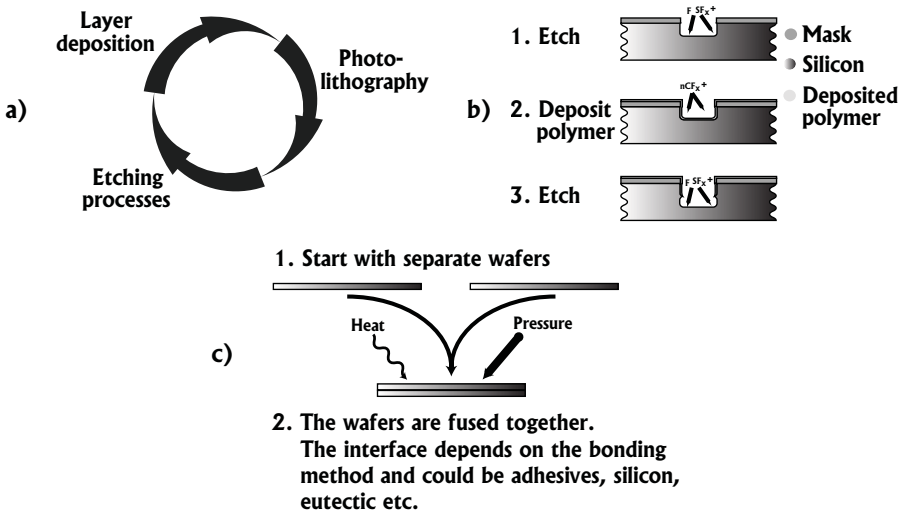

Figure 1.2: a) The microelectronics fabrication cycle. b) Depiction of deep reactive-ion etching. c) Depiction of wafer bonding.

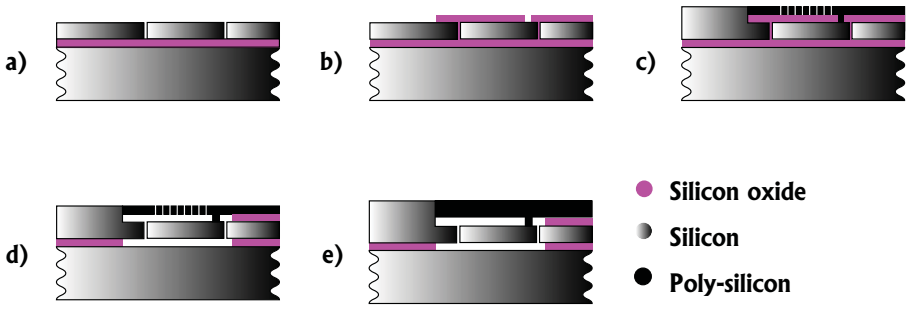

Figure 1.3: SiTime MEMS first platform. a) DRIE of resonator structures in a SOI wafer. b) Encapsulation of structures in SiO_x. Removal of SiO_x where future contacts and CMOS IC is to be formed. c) Epitaxial growth of Si. Si interfaces grow monocrystalline Si, while SiO_x interfaces grow poly-Si. Vent holes are made through the poly-Si to the embedded SiO_x. d) Vapor HF-removal of SiO_x. e) Sealing layer of epitaxially grown Si. Plugs the vent holes and encapsulates the resonator devices in vacuum. Planarization with CMP of the wafer surface. The resonator structure is sealed with poly-Si while monocrystalline areas surrounding the MEMS structure is available for future CMOS electronics fabrication [10].

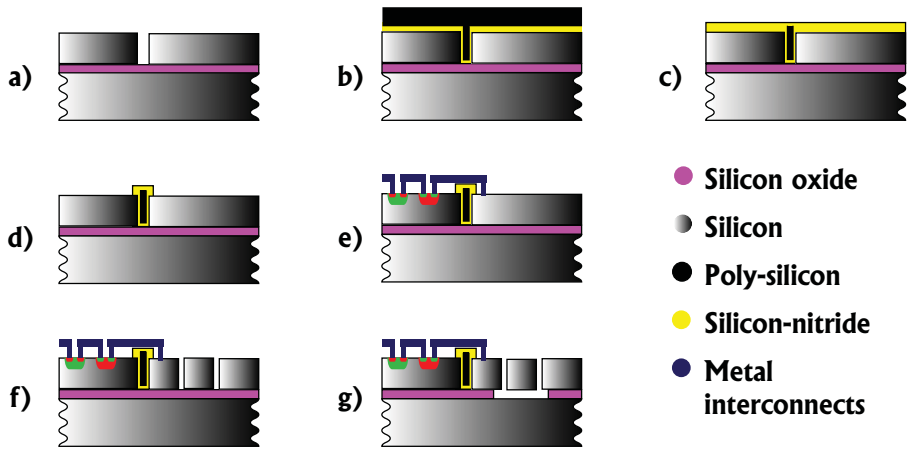

Figure 1.4: Analog Devices SOI-MEMS platform. a) Start with SOI wafer. DRIE trench structures that will be used for isolation between CMOS IC regions and MEMS regions. b) Deposit silicon-nitride followed by poly-silicon. c) Chemical-mechanical polishing of the poly-silicon. Stop on the silicon-nitride. Deposit another silicon nitride layer on top to encapsulate the poly-silicon trench. d) Remove unwanted silicon-nitride. e) Form the CMOS IC together with metal interconnects across the poly-silicon barrier trench to the MEMS region. f) DRIE the MEMS structure. g) Release the MEMS structure by removing the buried SiO_2-layer [11, 12].

M^3EMS, Mod-MEMS and SOIMEMS [11–14]. The fabrication platforms are similar to MEMS first approaches where MEMS structures are created and sealed, followed by a planarization of the wafer surface. This is followed by the IC fabrication. Further MEMS processing is done after the fabrication of the ICs on the wafer substrate to, for example, release mechanical Si structures by sacrificial removal of a buried material (i.e silicon oxide, SiO_x) used to embed the MEMS device during the creation of the circuitry. Analog Devices has successfully used a MEMS interleaved approach to fabricate accelerators and gyroscopes (Figure 1.4). The temperature is limited to below 450 °C in the post-IC fabrication step to avoid damaging the CMOS circuitry [7]. The same limitations as for MEMS first approaches are present and access to fabrication facilities is imperative for the viability of interleaved fabrication platforms.

The most important of the monolithic integration efforts is based on creating the MEMS devices after the ICs have been fabricated on a Si wafer substrate. The IC wafers can then be produced by standard semiconductor foundry services. Two different MEMS last approaches are utilized. The first approach uses the metal-insulator interconnect layers of the circuitry as hard masks that are used

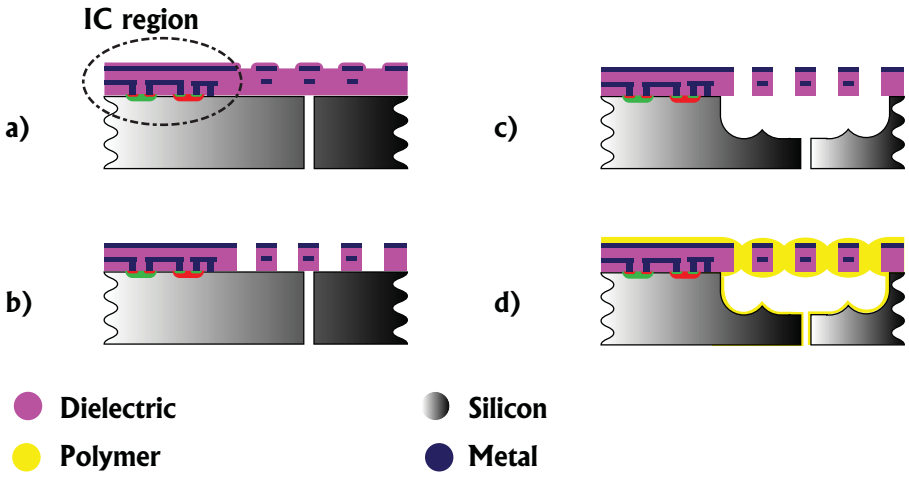

Figure 1.5: Akustica CMOS-MEMS technology platform. a) Vent holes for the microphones are etched from the backside with DRIE. Stops on the interconnect layer. b) Metal layers in the interconnect function as hard masks. The dielectric is etched through to the Si. c) The Si is isotropically etched. This creates a membrane of the interconnect layers. d) The membrane is sealed by deposition of a polymer [7, 15].

in the later MEMS processing steps. This MEMS last approach has been used by the company Akustica to realize SoC MEMS microphones [7, 15], where the MEMS microstructure is placed next to the electronic circuitry. Figure 1.5 shows a schematic description of the fabrication sequence. Patterning of a structural layer that is deposited on top of the IC wafer results in SoCs with a smaller footprint compared with placing the IC next to the MEMS structure. The method of depositing material on top of wafers with circuitry has been used to fabricate inertial sensors, oscillators and FPAs for thermal radiation [16–19]. Inertial sensors and oscillators require thick structural layers. SiLabs (Figure 1.6) has developed devices based on firstly depositing a sacrificial layer and secondly a poly-silicon-germanium (SiGe) structural layer on top in which a MEMS device is defined [20,21]. Poly-SiGe is used since the material can be deposited at temperatures that are acceptable to the ICs on the wafer substrate [22]. The temperature budget is limited to below 450 °C for MEMS last methods, as is the case with the final steps in interleaved MEMS fabrication.

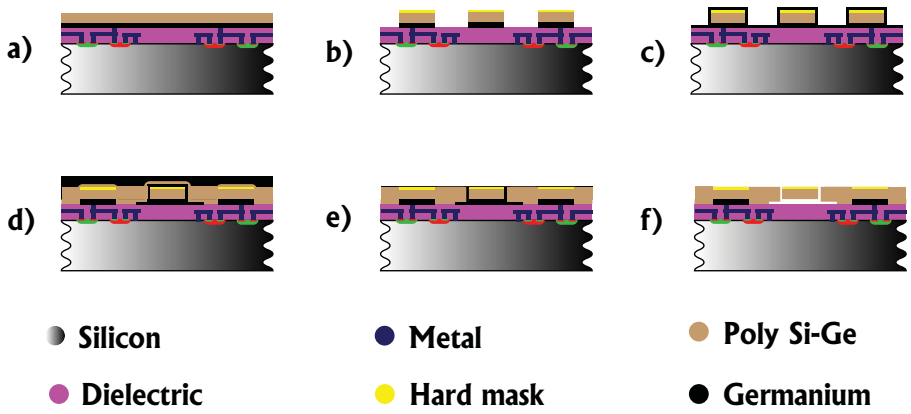

Figure 1.6: SiLabs CMEMS platform. a) A sacrificial Ge layer followed by a structural SiGe layer is deposited on top of a planarized IC wafer. b) Hard mask is deposited and used to define the resonator structures. c) Thin liner of sacrificial Ge is deposited. A masking step removes unwanted Ge. d) Structural SiGe is deposited followed by Ge to fill out cavities. e) The wafer is polished down to the hard mask layer. f) MEMS resonator is released by removing exposed Ge with hydrogen peroxide [20, 21].

1.2 Heterogeneous integration of MEMS and ICs

In heterogeneous integration, different submodules and materials are prepared individually. This is followed by an assembly step that is typically based on wafer bonding and if needed by further definition of the MEMS structures. Wafer bonding involving IC wafers is temperature restricted to below 450 °C due to limitations in the allowable temperature window of the IC wafer [7]. The preparation of the submodules opens up for the use of much more unrestricted choices of materials and processes compared with methods based on monolithic integration. For example, specialized materials that require high temperature processes can be prepared individually and then assembled on top of an IC wafer with a low temperature wafer bonding technique. This is followed by forming of the wanted devices. The higher temperature budget in the subassemblies opens up for advanced epitaxial material depositions, high temperature anneals to release stress and high temperature direct bonding steps in the subassembly before the submodule is integrated with ICs. Non-standard materials that otherwise are hard to integrate with standard microfabrication methods can also be attached to substrate wafers, for example thick shape-memory alloy sheets that are pre-etched into device structures and eutectically wafer bonded to Si wafers [23].

The NF platform by Invensense [24] is an example of heterogeneous integration where a CMOS IC wafer, a MEMS device wafer and a cap wafer is wafer bonded

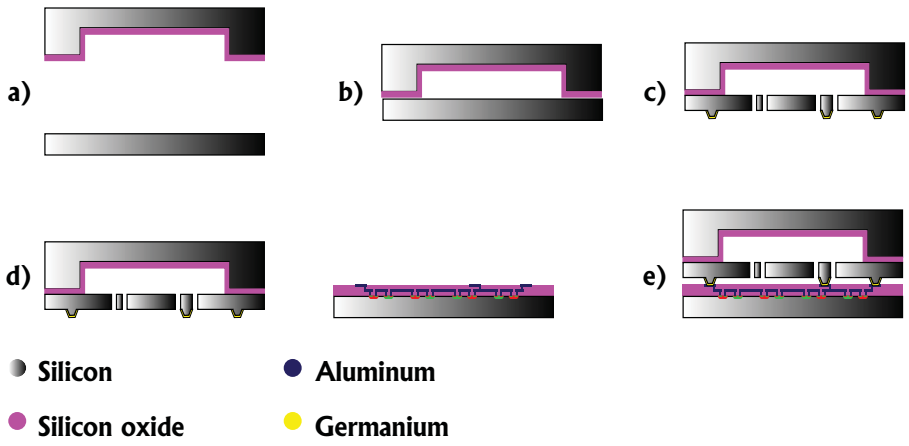

Figure 1.7: InvenSense NF-shuttle platform. a) Deep cavities are etched in a Si wafer. This is followed by thermal oxidation of the wafer. b) The cap wafer is attached to a Si wafer by fusion wafer bonding. c) MEMS structures are etched into the Si wafer together with standoffs to define the sealing ring and electrical contacts to the IC. A Ge-layer is formed over the standoffs. d) An IC wafer with uppermost Al interconnects is prepared. e) The MEMS wafer is bonded to the IC wafer using AlGe eutectic bonding between the Al in the uppermost interconnect layer and the Ge on the MEMS wafer [24].

into finished and assembled devices. The method starts with fastening a Si cap wafer and a Si device layer to each other by direct wafer bonding. The device layer is formed into the MEMS structures. This subassembly is then attached to a CMOS IC wafer by aluminium-germanium (AlGe) eutectic wafer bonding, where deposited Ge on the device layer wafer reacts and forms a bond with the uppermost Al interconnect layer of the CMOS wafer. The end results consist of vacuum packaged MEMS structures that are placed on top of CMOS circuitry. Figure 1.7 depicts the method.

Wafer bonding has also been used by KTH and Sensonor Technologies to integrate monocrystalline Si with SiGe quantum-wells (QW) on top of IC wafers for the creation of thermal radiation FPAs [25, 26]. In these platforms, a silicon-on-insulator (SOI) wafer with an epitaxially grown QW thermistor material is pre-fabricated. A sacrificial layer is deposited on top of both an IC wafer and the SOI wafer. The wafers are bonded to each other and the bulk Si of the SOI wafer is removed. This leaves a thin membrane of thermistor material bonded to the IC wafer. The thin thermistor layer is then processed into the desired sensor arrays. The last step removes the sacrificial bonding material, leaving free-standing membranes on top of the electronic circuitry. The Sensonor platform is described in

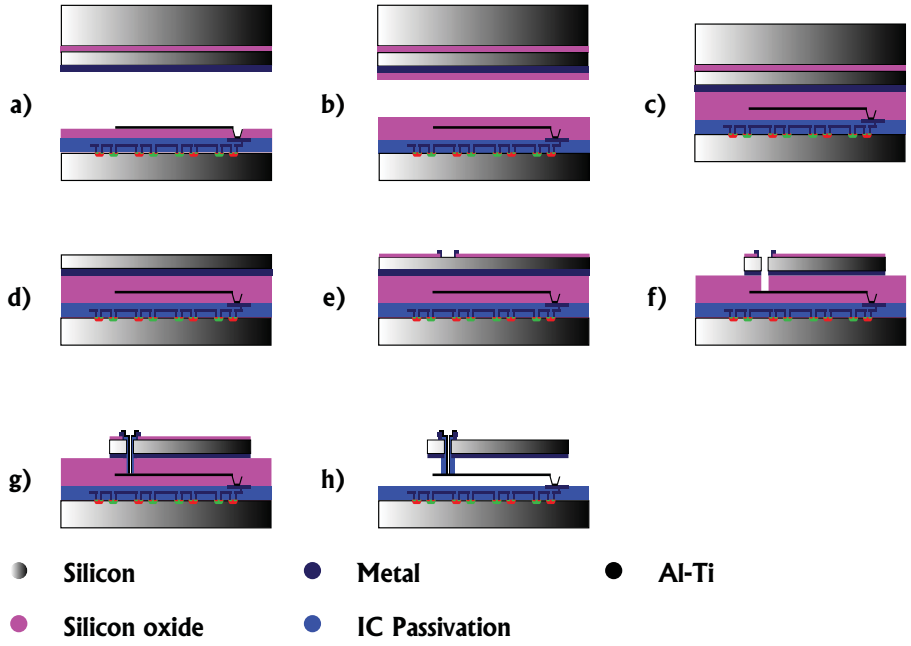

Figure 1.8: FPA integration platform. a) A SOI wafer with epitaxially grown sensor material is deposited with metal. SiO_x is deposited on an IC wafer, followed by formation of Ti-Al leg structures. b) Both the SOI wafer and IC wafer is deposited with SiO_x followed by CMP. c) Low temperature oxide-to-oxide wafer bonding. d)Handle and buried SiO_2 is removed from the SOI wafer. e) Deposition of SiO_x protective layer and formation of upper contact metal. f) Definition and etching of the sensor pixel. Contact hole is formed through the pixel to Ti-Al leg structure. g) Passivation of the contact hole followed by deposition and definition of Ti-Al to electrically connect the IC wafer through the leg structure and to the upper metal contact. h) Removal of the SiO_x to create free-standing sensor membranes above the IC [25].

Figure 1.8 while the KTH platform is presented in chapter 2. A similar integration platform has also been used for the creation of micro-mirrors on top of CMOS electronics [27, 28].

1.3 Comparison of monolithic and heterogeneous integration approaches

One recurring problem of MEMS fabrication can be summarized in the expression 'one product, one process, one package'. This captures the specialized nature of different MEMS sensors that typically require different and product-specific fabrication approaches. This presents multiple problems regarding yield, time-to-market and ease of manufacture since each and every product need to be optimized individually. An ideal and flexible fabrication platform that can be reused for different MEMS devices should allow: a wide selection of materials, a large temperature window, limited investments in fabrication equipments and the use of fabless manufacturing services.

Monolithic MEMS first and MEMS interleaved integration with ICs require ownership of IC manufacturing lines or close cooperation with a semiconductor foundry, due to the non-standard fabrication sequence compared with normal IC production. This limits its viability in practice. The development cost and yield is also potentially problematic compared with standard IC fabrication. MEMS last fabrication techniques opens up for the use of standard IC wafers from semiconductor foundries. This can be followed by MEMS processing steps that potentially can be outsourced to MEMS foundry services. Stress issues and limited choices of acceptable MEMS materials are issues of concern since MEMS last monolithic integration methods require a limited temperature budget below 450 °C to avoid damaging the ICs. Heterogeneous integration methods potentially alleviate many of the concerns that are present with the other methods. It allows for a more unrestricted fabrication of product-specific submodules that are integrated using a standardized integration scheme. The heterogeneous integration scheme preferably also include a standardized wafer-level packaging strategy. The fabrication of different product specific submodules opens up for the reuse of the same heterogeneous integration platform for different devices. This saves development time and potentially increases the yield since all submodules (IC, MEMS, packaging cap wafer etc.) can be prepared with methods that are optimized for quality and manufacturability before the use of a standardized heterogeneous integration method for the device assembly.

1.4 Outline of the thesis

Chapter 2 consists of an introduction to uncooled resistive microbolometers and describes a method based on heterogeneous integration to realize resistive microbolometer focal plane arrays (FPA) in a CMOS IC-compatible process. The

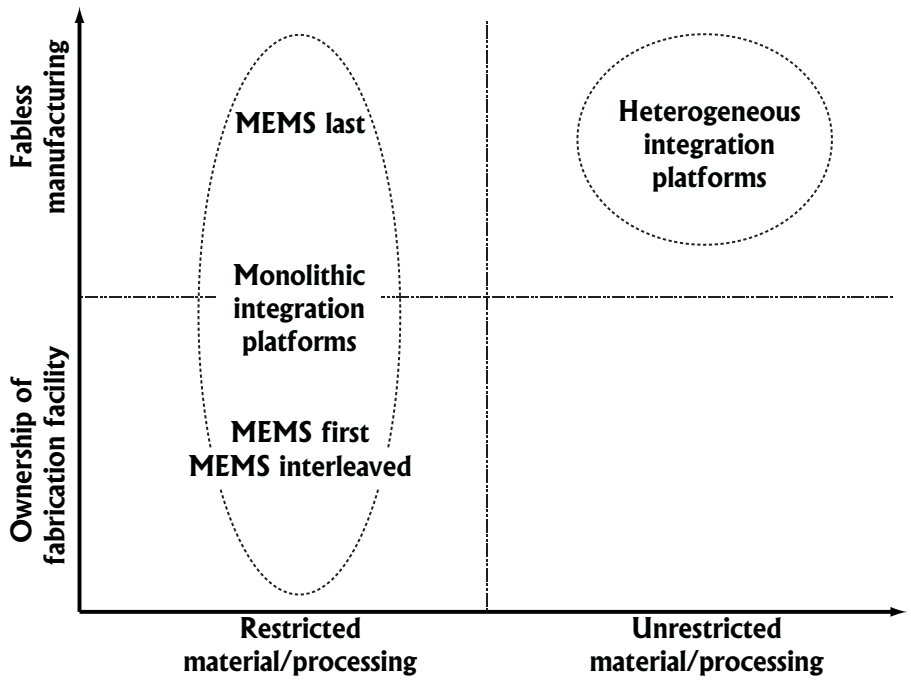

Figure 1.9: Comparison of different fabrication strategies with regards to processing window and access to manufacturing facilities.

basis for the heterogeneous integration of the FPAs is adhesive wafer bonding. The bond energy between the adhesive and the glued layers is of critical importance. A method to evaluate the bond energy is presented in Chapter 3. Heterogeneous integration methods have also been used to fabricate components as diverse as nano-porous membrane filtering devices and graphene pressure sensors. These are described in Chapter 4 and 6, respectively. Chapter 5 describes a novel heterogeneous integration method for the controlled distribution and parallel transfer of a large number of dies between different wafer formats.

Chapter 2

Uncooled microbolometer-based focal plane arrays

2.1 Introduction

Blackbody radiation is emitted by all objects with a non-zero temperature. The electromagnetic spectrum and intensity of an ideal blackbody is given by Planck's radiation law (Figure 2.1). In the real world, objects differ from the ideal blackbody emission. The emissivity of a material is the relative ability of its surface to emit energy by radiation compared with an ideal blackbody. Thus, the emissivity is 1 for an ideal blackbody and down to below 0.1 for polished metal surfaces [29]. The emitted electromagnetic radiation is radiated through the atmosphere, where parts of the radiation is absorbed depending on its wavelength. This creates infrared atmospheric transmission windows (Table 2.1) with a low attenuation of the infrared radiation [30].

Long-wavelength infrared(LWIR) camera systems are designed to detect the blackbody radiation. The radiation is captured by LWIR optics and is focused down onto a sensor array (Figure 2.2). The spectrum of the blackbody radiation that is emitted by objects in ambient temperature has a maximum intensity around a wavelength of 10 μm, which is inside the far infrared (FIR) atmospheric transmission window. Thus, LWIR sensors are usually optimized to absorb thermal radiation between wavelengths of 8-14 μm to maximize the detector signal. In principle, there are two ways to sense incoming infrared radiation. Either photonic sensors are used. These are typically based on photoconductors or photodiodes where incoming photons generate charge carriers. The main limitation of this method is that it requires substantial cooling below ambient temperature to reduce electronic noise due to thermally excited current carriers. Thermal sensors, on the other hand, are sensors that absorb the incoming infrared radiation and experience a change in their temperature. This temperature change is in turn converted into an electric output signal that can be probed. Thermal infrared sensors can,

unlike photonic sensors, be operated uncooled at ambient temperature. This characteristic makes uncooled thermal infrared sensors useful for small, lightweight and portable products [29]. A variety of different physical operating principles are used to realize thermal infrared sensors, although the basic structure of the sensor is the same. A well-isolated detector element absorbs incident LWIR radiant flux and converts it into heat energy that increases the temperature of the detector element. The resulting temperature increase is related to the power of the absorbed LWIR radiation and the responsivity is in theory wavelength-independent [30]. In reality, the design of the LWIR absorbing structure will create a wavelength dependent responsivity of the output signal due to differences in the absorption of different wavelengths. The increase in temperature is sensed by either transducer-based detector elements or parametric sensors, where the temperature of the sensor element modulates an electric signal. Examples of LWIR transducers are pyroelectric sensors [31–33] and thermocouple/thermopile based sensors that utilize the Seebeck effect [34, 35]. Parametric sensors are based on a range of physical effects. Among these are the temperature-dependence of the electrical resistance [36–46], temperature-dependence of the pressure in enclosed gas cavities (i.e Golay cells) [47], temperature-dependence of bimaterial mechanical structures [48, 49] and the temperature-dependence of diode forward voltage drops [50–54].

The commercially most successful of the physical principles to realize FPAs consists of resistive microbolometers, which is also the focus of *the Work* discussed in this Chapter. The change in resistance due to the incident LWIR radiation is measured for each microbolometer in the FPA, which together registers the thermal image information. Figure 2.3 depicts the outlay of a resistive microbolometer. It consists of a free-standing membrane of a thin material that experience a change in resistance with temperature. The membrane is connected to a readout IC through the leg structure. The leg structure functions both as a thermal path between the membrane and the surroundings and as an electrical connection. A maximized output signal requires a minimized thermal conductance from the membrane. That is realized by vacuum encapsulation of the microbolometer together with an optimized leg structure regarding its choice of materials and design. The microbolometer legs and membrane need to be stress compensated to avoid a thermal short circuit between the microbolometer membrane and the bottom substrate. A high signal-to-noise ratio of the electrical output signal depends on the temperature coefficient of resistance (TCR), electrical noise and the thermal insulation of the sensor membrane [30, 55, 56]. Furthermore, optical considerations for the membrane need to be taken in regard to optimize the absorbance of incident LWIR radiation [57, 58]. The next sections will delineate important design parameters to optimize in the realization of LWIR FPAs and show examples of monolithically integrated LWIR FPAs. This is followed by a description of how to realize heterogeneously integrated FPAs. A theoretical treatment of resistive microbolometer-based FPAs is presented in Appendix A.

Table 2.1: Atmospheric transmission windows [30]

Infrared region	Wavelength [μm]
Near infrared (NIR)	1.2-1.3
	1.5-1.7
	2.1-2.4
Mid infrared (MIR)	3.2-4.1
	4.4-5.2
Far infrared (FIR)	8-13

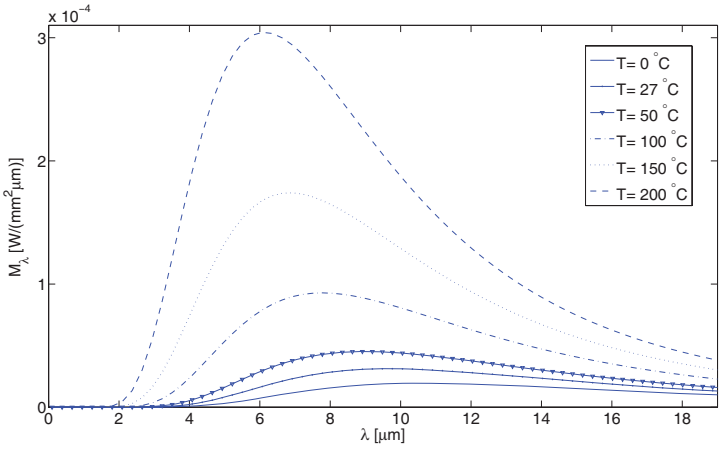

Figure 2.1: Ideal blackbody radiation as given by Planck's radiation law.

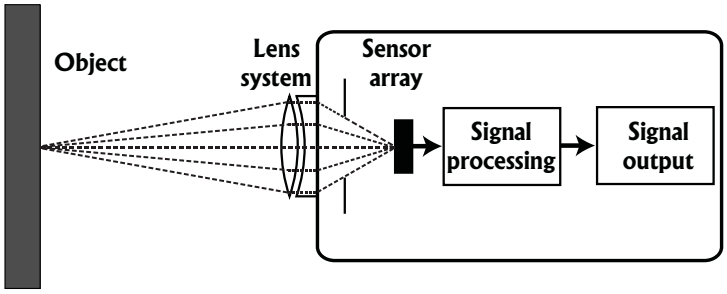

Figure 2.2: Signaling chain of a LWIR camera system.

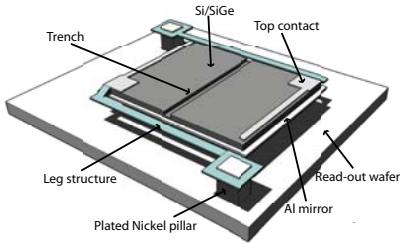

Figure 2.3: Typical outlay of a resistive microbolometer. Taken from [26].

2.2 Optimization parameters for resistive microbolometers

Different measures have been developed to characterize the performance of LWIR sensors. The responsivity is a measure of the output signal (either current, $\Re_I$, or voltage, $\Re_V$) from the sensor per incident radiant power (unit, I/W or V/W). Noise equivalent power (NEP) is a measure of the equivalent incident radiant power to achieve an output signal equal to the root-mean-square noise output (unit, W). The NEP corresponds to a signal-to-noise ratio (SNR) of 1. A similar measure is the noise equivalent temperature difference ($NETD$) which is defined as the temperature difference in the viewed object that generates a SNR of 1 of the LWIR measurement system (unit, K). Larger sensor pixels are generally more sensitive than smaller ones. The measure specific detectivity (D^*) was developed to compare sensors with different pixel areas. This is essentially a rescaled SNR regarding the pixel size and the bandwidth of the sensor system (unit, $(m \cdot \sqrt{Hz})/\mathrm{W}$).

Table 2.2 tabulates the different sensor parameters that are used in the set of equations given below for the scaling laws of $NETD$ [30, 55, 59]. Please, refer to Appendix A for derivations and complete expressions of NEP, D^*, $\Re_V$ and $NETD$.

Scaling laws of LWIR performance parameters:

$$\Re_V \propto \frac{TCR \cdot \beta \cdot \alpha_{\lambda_1-\lambda_2}}{G_{th}}$$

$$NETD \propto \frac{\tilde{\nu_R}}{\Re_V}$$

The smallest possible $NETD$ for a LWIR sensor with a given pixel area and a given optical system requires that the responsivity, $\Re_V$, is maximized and the total electronic noise, $\tilde{\nu_R}$, is minimized. The responsivity in turn can be increased by using materials with a high TCR, a pixel design with a high fill factor (i.e

Table 2.2: Microbolometer parameters

Parameter	Unit	Description
TCR	$\frac{\%}{K}$	Temperature coefficient of resistance.
β	-	Microbolometer fill factor.
$\alpha_{\lambda_1-\lambda_2}$	-	Relative infrared absorbtion in the wavelength interval $\lambda_1 - \lambda_2$.
G_{th}	$\frac{W}{K}$	Thermal conductance.
ν_R	V	Total voltage noise.

the relative area used by the microbolometer absorption structure), high LWIR absorption and a high thermal insulation.

A high thermal insulation is achieved by vacuum encapsulation of the FPA together with leg structures that are as long and thin as possible [60]. Long legs can be achieved by curling them up in meander structures. This increases the area of the pixel that is used by the leg structures compared with the sensor membrane (thermistor) and decreases the pixel fill factor. One method to achieve a high fill factor together with the use of long meander leg structures consists of building two- or three layer structures [37,54]. The bottom layer or layers consists of leg structures that fill the pixel area with curled meander-shaped legs. The top layer consists of an umbrella-shaped absorption structure that enables a high microbolometer fill factor and couples the absorbed heat into a thermistor. This kind of structures increase the microbolometer performance with the cost of increased fabrication complexity.

Electronic noise consists of many different noise components that are weighted together. Contributions to the noise in uncooled thermal LWIR systems arise from the readout IC, the microbolometer sensor and thermal fluctuations in the microbolometer [55, 59]. The readout IC generally contributes less noise compared to the contribution from the microbolometer sensor [59]. Different noise contributions in the microbolometer thermistor material have different spectral properties and magnitudes. Examples of electronic noise in a microbolometer are Johnson-Nyquist noise, shot noise and flicker noise ($1/f$-noise) [61]. Of these, the $1/f$-noise of the microbolometer, in a well-designed system, dominates the total noise in the output signal [56, 59]. Minimization of the microbolometer noise and with that the system noise is thus focused on the minimization of the flicker noise. The flicker noise can be quantified by the equation [62, 63]:

$$\frac{S_I}{I_{bias}^2} = \frac{\alpha}{N f^\gamma}$$

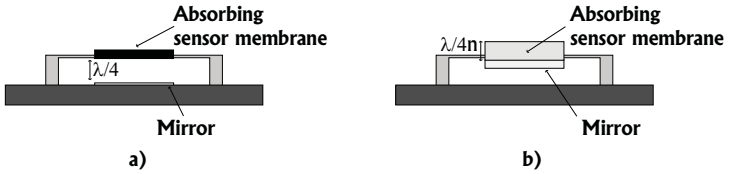

Figure 2.4: $\lambda/4$-wavelength absorption structure arrangements. a) Thin semi-transparent membrane vacuum-separated $\lambda/4$ from an LWIR mirror. b) $\lambda/(4$ n)-thick semitransparent membrane with a directly attached LWIR mirror on the backside of the membrane, where n is the refractive index of the membrane material.

where S_I is the noise power, I_{bias} is the bias current, N is the total number of free charges in the thermistor material, α is known as Hooge's constant and γ is a parameter close to 1. Minimization of the flicker noise is dependent on minimizing $\frac{\alpha}{N}$ which is also known as the K-parameter for the thermistor material [64]. Different electrically contacted thermistor materials have drastically different noise properties. The $1/f$-noise depends on among others the quality of deposition, what thermistor material is used, the quality of electrical contacts and the sidewall passivation [25].

The maximization of LWIR absorption is achieved by designing the microbolometer as an $\lambda/4$-wavelength absorption structure [57, 58], where λ is the wavelength the absorption structure is optimized for. Two typical designs are depicted in Figure 2.4. The first one consists of a thin semi-transparent membrane $\lambda/4$-wavelength above an LWIR mirror and the second structure consists of a semi-transparent membrane with the LWIR mirror directly on the backside.

2.3 Monolithically integrated LWIR FPAs

Monolithic integration of resistive microbolometer FPAs are by far the dominating uncooled LWIR technology. The fabrication procedure is described in Figure 2.5 and consists of depositing materials on top of prefabricated IC wafers. The limitations of this method consist of restricted material choices and a restricted temperature budget to avoid damaging the IC circuitry [7, 26]. The fabrication procedure starts with depositing a sacrificial material layer that in the finishing step will be removed to create free-standing microbolometer membranes. This is followed by deposition of the thermistor material and mechanical support material for the legs. The most commonly used thermistor materials are vanadium oxide (VO_x) [36, 38, 41, 42, 65] and amorphous silicon (α-Si) [45, 66]. Metallic thermistor materials have also been utilized, for example titanium- [67] and atomic layer deposited platinum [46]. Both metal- and VO_x-based microbolometers typically have low sensor resistances compared with α-Si [46, 67, 68]. Metal-based microbolometers are characterized by both low $1/f$-noise and a low TCR [46].

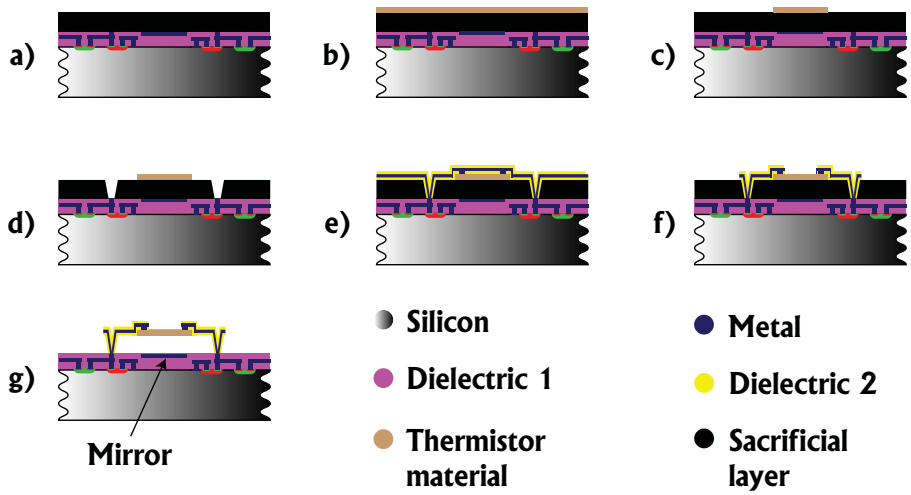

Figure 2.5: Simplified fabrication scheme for resistive monolithic microbolometers. a) Deposition of sacrificial layer on top of an IC wafer. b) Deposition of sensor material. c) Formation of sensor membrane. d) Etching of vias for electrical connections between the sensor membrane and the IC. e) Deposition of leg material stack. f) Definition of the leg structure. g) Removal of the sacrificial layer for the formation of free-standing microbolometer membranes. Author's interpretation of the fabrication sequence for monolithic FPAs.

Microbolometers with semiconductor-based thermistors have in comparison both higher $1/f$-noise and TCR [25, 64]. The thermistor material development for microbolometer applications consists of making an optimized trade-off between these parameters. Modern uncooled LWIR FPAs usually consist of microbolometer-based pixels with sidelengths between 17 µm to 25 µm, although smaller pixel designs down to 12 µm exist [37].

A high fill factor is needed to maximize the absorption of the incoming LWIR radiation. This requires a trade-off with the area occupied by leg structures. That can be alleviated by creating an extra umbrella-shaped absorption structure above the sensor membrane. An example of this can be seen in Figure 2.6, where constant current-biased diodes are used as the sensor element [54, 69]. The diode-based approach to uncooled LWIR FPAs consists of forming the sensor-diodes concurrently with the CMOS electronics fabrication. An underetch of the bulk Si underneath the bolometers are used to form free-standing sensor membranes with a high thermal insulation. Higher responsivity is achieved by coupling multiple sensor diodes in series, since the output signal scales with the number of diodes [51].

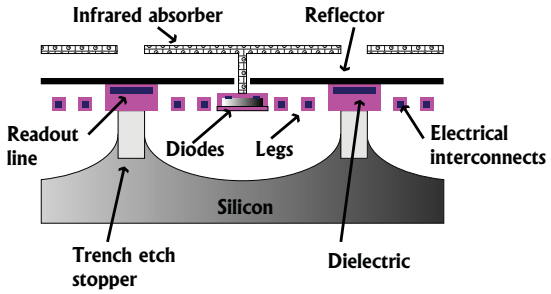

Figure 2.6: Example of a diode-based microbolometer with an umbrella-design to increase the fill factor and LWIR absorption. Taken from [54].

2.4 Heterogeneous integration of LWIR FPAs

In this approach (presented in *Paper 1* and *Paper 2*), a monocrystalline Si/SiGe quantum-well based material is used as the microbolometer thermistor material. This thermistor material is attractive due to its combination of high TCR around 3 %/K [25] and low electronic noise compared with VO_x and α-Si [64, 70]. The monocrystalline structure of the Si/SiGe quantum-well based material decreases the magnitude of 1/f-noise compared with thermistors made from poly-crystalline and amorphous materials and the SiGe quantum wells increase the temperature dependence of resistance [70]. However, the thermistor material is grown with epitaxial methods and requires a high deposition temperature of more than 600 °C [64]. This is above the temperature budget of readout ICs. The only method for SoC-integration of this kind of material with ICs is thus separate fabrication of the thermistor material, followed by heterogeneous integration of the thermistor wafer with an IC wafer. The thermistor is also used as the absorption structure in the microbolometer design.

2.4.1 Microbolometer Design

Heterogeneously integrated microbolometer FPAs are designed for applications in the 8-14 µm wavelength spectral range and the infrared absorption of the microbolometer is optimized by designing it as an optical $\lambda/4$-cavity [57]. The optical cavity consists of a bottom Al mirror, epitaxially grown Si/SiGe and plasma enhanced chemical vapor deposited (PECVD) SiO_x and silicon nitride (SiN) passivation layers. A schematic cross-section of a microbolometer pixel is shown in Figure 2.3. The microbolometer leg structures consist of a sandwich structure SiN, titanium tungsten (TiW) and SiN to both stress compensate the leg and to encapsulate the thin TiW film that provides the electrical contact between electroless plated nickel (Ni) pillars and the thermistor material. The legs connect to deposited Al contacts on the Si/SiGe thermistor material. An etched trench disconnects the two top contacts on the Si/SiGe thermistor material from each other through the uppermost highly doped Si contact layer. This is used to guide the current vertically through the horizontally arranged Si/SiGe quantum wells of the microbolometer membrane [26]. A depiction of the microbolometer cross-section is shown in Figure 2.7 together with the electrical current path.

2.4.2 Fabrication sequence

An overview of the most important steps to realize very large scale heterogeneous integration for LWIR microbolometer arrays is presented in Figure 2.8. The starting materials consist of a readout-wafer with electrical interconnects and a SOI wafer with the epitaxially grown Si/SiGe quantum-well material stack. The wafers are adhesive wafer bonded to each other with a 3 µm thick polymer layer (mr-I 9150, Micro Resist Technology GmbH). This is a sacrificial layer that will be removed

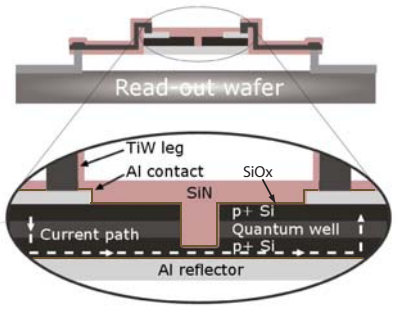

Figure 2.7: Cross-section of a microbolometer. The current path is vertically across the epitaxially grown Si/SiGe quantum well layers as indicated in the close-up. The trench cuts the highly doped Si between the upper contacts, which forces the applied current to travel through the quantum well structure. Taken from [71].

in the last step of the fabrication scheme. Only the epitaxially grown material is needed and the SOI wafer handle is removed together with the buried oxide layer (Figure 2.8 b). Contacts and thermistor pixel are defined and etched (Figure 2.8 c-d) and a PECVD SiN layer is deposited onto the surface. Holes are made through the adhesive and the SiN layer to metal pads on the bottom substrate and electroless plating is used to fill the holes with Ni [72] (Figure 2.8 e-f). This is followed by definition of the legs (Figure 2.8 g-h) and removal of the sacrificial bonding adhesive with an oxygen plasma (Figure 2.8 i).

Scanning electron microscopy (SEM) images of three different designs of 17 μm pitch microbolometers are presented in Figure 2.9. Microbolometer designs A and B were designed with 500 nm wide microbolometer leg structures while design C has a minimum designed microbolometer leg width of 575 nm. The fabricated legs differed in width from the mask design and were measured to be between 75-100 nm below the target value [26].

2.4.3 Stress compensation of microbolometer leg structures

The microbolometer leg structures need to fulfill three requirements. The first requirement is as an electrical connection between the readout IC and the microbolometer thermistor, the second requirement is to thermally decouple the thermistor from the surroundings and the third requirement is as a structural mechanical support of the free-standing microbolometer membrane. The thermal decoupling of the thermistor membrane depends on the design and material choices. Geometrically long and thin legs made out of materials with low thermal conductivity favor a higher thermal insulation. Metals (i.e low electrical resistivity materials), needed for highly reliable electrical connections between the readout

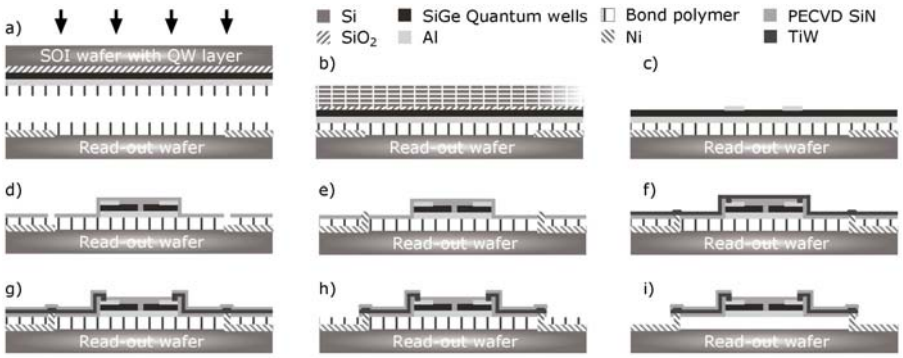

Figure 2.8: Integration scheme with important steps in the microbolometer fabrication process. a) Wafer bonding of SOI wafer to a target wafer. b) Removal of Si handle and buried oxide of the SOI wafer. c) Deposition and definition of Al upper contacts. d) Definition of Si/SiGe thermistors followed by PECVD SiN deposition and etching of via holes. e) Plating of Ni vias. f) Contacting Ni vias and upper Al contacts with deposited TiW. g) Deposition of PECVD SiN. h) Definition of microbolometer legs and membranes followed by etching down to the bonding polymer i) Release microbolometer structures by sacrificially etching the bonding polymer with an isotropic oxygen plasma. Taken from [26].

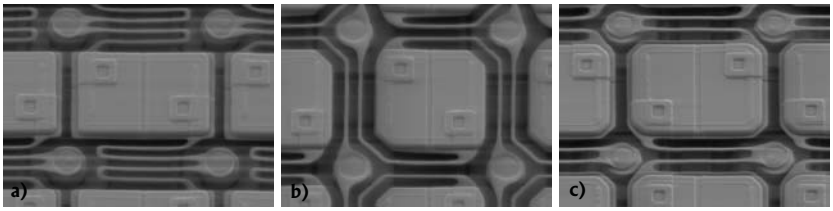

Figure 2.9: Different 17 μm pitch microbolometer designs. a) 500 nm wide meander leg design. b) 500 nm wide surrounding leg design. c) 575 nm wide single leg design. Taken from [26].

IC and the individual bolometers, are characterized by high thermal conductivity since the same mobile electrons that participate in the electrical conduction also participate in the heat transfer. This implies that the leg structures should be designed with as thin metal layer for electrical connections as possible to minimize the thermal conductance from the microbolometer membrane. The requirement for mechanical support of the free-standing thermistor membrane is solved by the introduction of a dielectric support material with a low thermal conductivity. In the design presented in *Paper 1* and *Paper 2* TiW was used as the electrical connection material and SiN as the structural material. Figure 2.10 depicts the fabrication sequence in detail. SiN is deposited in two separate layers around the TiW metal layer in the formation of a three-layer leg structures. This is due to the different internal stress properties of the deposited layers, where a symmetrical leg-stack composition (SiN/TiW/SiN) is easier to stress-compensate than structures based on two layers with different material properties. The first SiN layer is deposited on top of the bonding polymer, followed by the deposition of a TiW layer. This two-layer structure is sensitive to temperatures above 110 °C and experienced changes in stress properties without proper precaution. Temperatures above 110 °C occurs during the second SiN layer deposition. The TiW layer was therefore etched into smaller stipes of TiW. This alleviated the problem with uncontrolled changes of the stress properties. Figure 2.11 is a microscopy image of a deposited triple stack where a mask design based on too large TiW islands resulted in changed stress properties [26]. Figure 2.12 shows a comparison between two test designs of TiW islands together with the layer thicknesses used in the actual microbolometer array fabrication (150 nm lower SiN, 50 nm TiW, 200 nm upper SiN). The structures in Figure 2.12 a was defined on a large rectangular (170 μm × 230 μm) TiW island between two SiN layers and resulted in test structure fingers bending downwards. The structures in Figure 2.12 b had the same finger design but is instead defined and etched on smaller 4 μm wide stripes of TiW, one for each finger, that avoids too severe bimaterial induced changes of the mechanical properties. This results in fingers bending upwards [26].

2.4.4 Characterization of resistive microbolometers

2.4.4.1 Resistive properties

TCR is recorded by measuring the resistance of individual microbolometers at different temperatures. Resistive heating occurs during readout and the resistance measurement preferably is performed by applying short square-wave voltage pulses in atmospheric pressure to avoid excessive heating. Resistance and TCR for a microbolometer is given by:

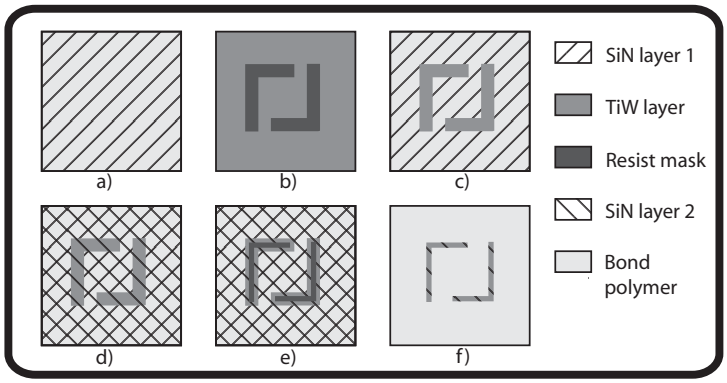

Figure 2.10: Fabrication sequence for microbolometer leg structures. a) SiN layer is deposited on top of bonding polymer. b)-c) TiW is deposited and masked into islands and etched down to the SiN layer. d) Second SiN layer is deposited. e) The TiW islands are masked into the final leg structure design. f) The triple stack is etched to the bonding polymer, forming the final microbolometer leg structure. Taken from [26].

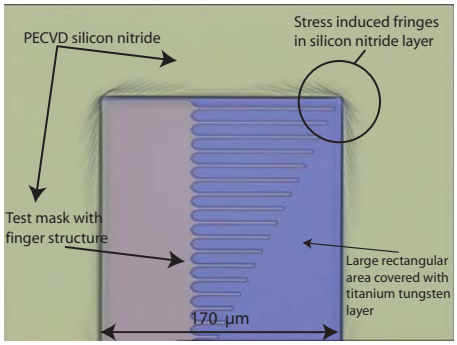

Figure 2.11: Microscopy image of a test structure with changed mechanical properties due to definition of TiW islands above a critical size. The image is taken before the last etching step that defines the finger structure. Fringes can be observed in the edges of TiW islands. Also shown is the masking layer for evaluation finger structures. Taken from [26].

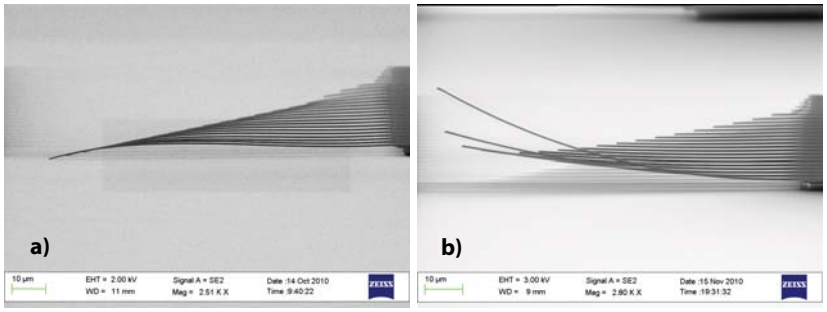

Figure 2.12: Finger test structures fabricated with a 150 nm thick bottom SiN layer, a 50 nm thick TiW layer and 200 nm thick SiN upper layer but defined on differently sized TiW islands. Taken from [26].

$$R = R_{thermistor} \cdot exp\left(\frac{\Delta E}{k_b}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right)$$

$$TCR = -\frac{\Delta E}{k_b T^2}$$

Where R is the resistance, $R_{thermistor}$ is the resistance at 25 °C, k_B is the Boltzmann constant, T is the absolute temperature, T_0 a reference temperature at 298 K and ΔE is the quantum well barrier height [26]. Figure 2.13 shows typical measurement results of the temperature dependent resistance for a microbolometer.

2.4.4.2 Thermal properties

A straight forward method to determine the heat conductance and thermal mass of individual resistive microbolometer pixels is based on applying square-wave voltage pulses to a Wheatstone bridge configuration where one of the four resistances in the bridge consists of a microbolometer [73, 74]. An applied voltage pulse Joule-heats the microbolometer and the resulting resistance change unbalances the Wheatstone bridge. The thermal parameters can be evaluated by measuring the voltage response from the Wheatstone bridge. A typical response for a resistive microbolometer is given in Figure 2.14. The rise time of the voltage response from the Wheatstone bridge is used to determine the thermal mass, where smaller thermal masses corresponds to smaller rise times since less thermal energy is needed to induce temperature changes in the microbolometer thermistor. The voltage response pulse from the Wheatstone bridge saturates after the thermal time constant τ. The saturated voltage signal is used to calculate the thermal conductance from the microbolometer pixel.

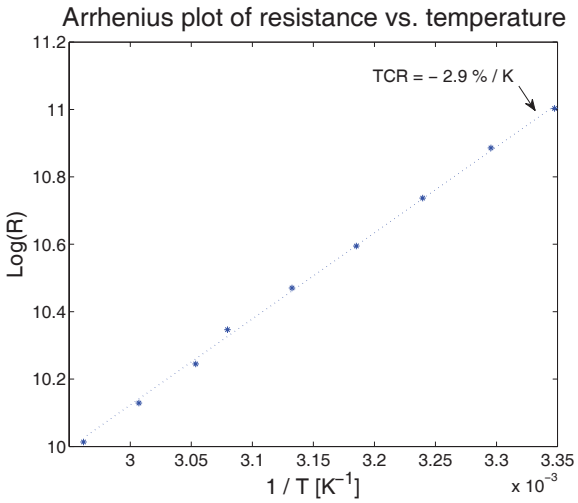

Figure 2.13: Arrhenius plot of the logarithm of resistance as a function of T^{-1} for a 17 µm microbolometer. A TCR of - 2.9%/K was extracted from the data. Taken from [26].

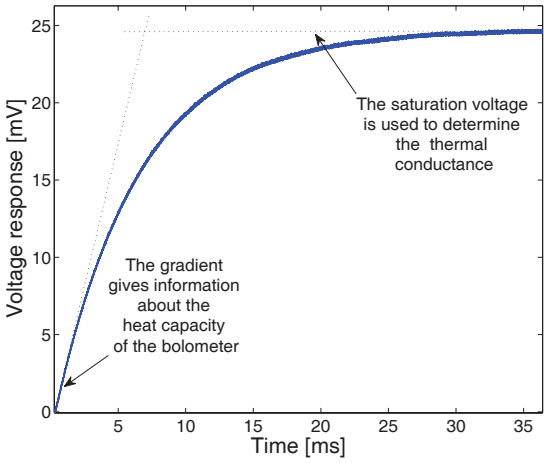

Figure 2.14: Thermal characterization measurement. A 17 µm microbolometer is pulsed with a 300 mV square wave in a Wheatstone bridge configuration. Thermal conductance is estimated by measuring the saturation voltage. The gradient of voltage response is used to determine the heat capacity. Taken from [26].

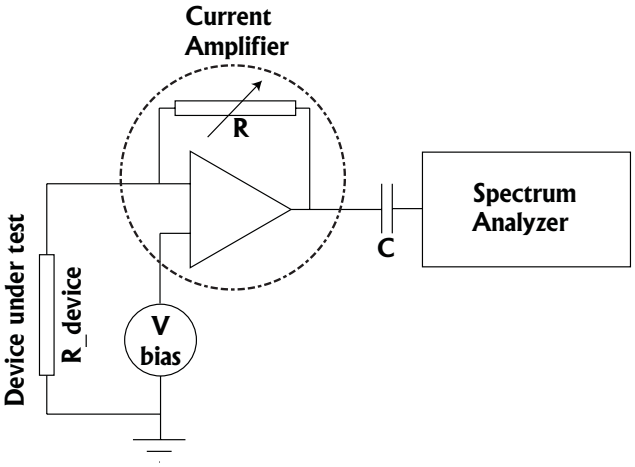

Figure 2.15: Simplified noise measurement setup. The device under test is biased with a DC voltage. A transimpedance amplifier is used to record the output signal. AC signal data is recorded in a spectrum analyzer, which gives information about the PSD of the device. Adapted from [61]

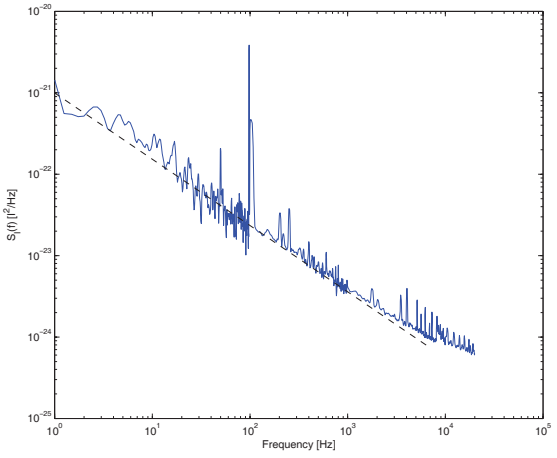

Figure 2.16: Measured noise power spectral density for a 17 µm microbolometer. Taken from [26].

2.4.4.3 Electrical noise measurements

Low-frequency electrical noise measurements are typically done in a frequency-range from 1 Hz to 1 MHz and results in the power spectral density (PSD) of the noise from the device [61]. A typical setup is given in Figure 2.15 and is based on biasing the device we want to measure with a very stable DC voltage source (i.e batteries). The measurements are based on measuring very weak signals and outside disturbances need to be shielded from the measurement setup. The measured noise signal is amplified in a low noise amplifier and fed into a spectrum analyzer which records the spectral composition of the noise. Typical results of the noise PSD from a microbolometer is presented in Figure 2.16. The flicker noise (i.e $1/f$-noise) dominates in this case and resulted in an extracted K-parameter ($\frac{\alpha}{N}$) of $4.5 \cdot 10^{-11}$ when $\gamma = 0.9$ was used as a fitting parameter [26].

2.4.5 Wafer-level vacuum packaging of FPAs

The microbolometer sensitivity is dependent on the temperature response of the incoming electromagnetic radiation. A large sensor temperature response requires minimizing the thermal conductance from the microbolometer thermistor to the surroundings. Hermetic vacuum encapsulation of FPAs minimizes the heat conductance through the surrounding gas which increases the microbolometer sensitivity. The heat transfer through the leg structures start to dominate for vacuum pressures below 10^{-2} mbar [60], and thus high quality vacuum packaging is imperative for both the FPA performance and the reliability over time. The proposed wafer-level vacuum packaging process of FPAs (presented in *Paper 2*) is based on solid-liquid interdiffusion bonding of a Si cap wafer, where an isothermal solidification of copper (Cu) and Tin (Sn) occurs. Figure 2.17 describes the most important steps in the packaging scheme. The basic idea consists of electroplating bond frames of Cu followed by Sn on a lid wafer and an IC wafer with fabricated FPAs. The layer of Sn is electroplated on top of the Cu bond frame to prevent unwanted native oxide on the Cu. The lid wafer, besides the electroplated bond frames, consists of etched cavities to accommodate the FPAs, deposited thin film getters and antireflective coatings. The sputtered and patterned non-evaporative getter structures are deposited for vacuum reliability. The getter structures are not transparent for LWIR and are thus placed beside the active microbolometer pixels. The prepared lid wafer is aligned and pressed together with the IC wafer and the wafer stack is exposed to a controlled temperature ramp to drive an interdiffusion of the Cu and Sn, firstly into a Cu_6Sn_5 phase and subsequently into Cu_3Sn at the Cu-Sn interface [71]. Re-melting of the bond alloy occurs at 415 °C for bonds consisting of a mixture of Cu_3Sn and Cu_6Sn_5 phases and at 713 °C for bonds consisting of pure Cu_3Sn [71]. This ensures a reliable packaging bond, that should be compared with the start of Cu/Sn interdiffusion at temperatures below 232 °C (melting point of Sn). Figure 2.18 shows examples of FPAs packaged with the approach described above.

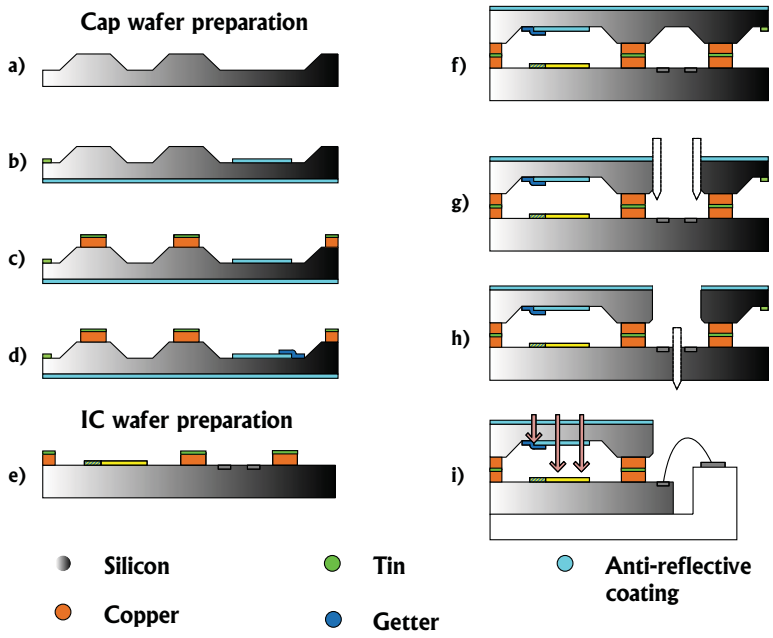

Figure 2.17: a) Formation of cavities into the Si lid wafer. b) Deposition of antireflective coatings. c) Electroplating of Cu and Sn bond frames. d) Deposition of getters. e) Electroplating of Cu and Sn on IC wafer. f) Wafer-level bonding of the lid wafer to the ROIC wafer. Formation of Cu_3Sn in the bond interface. g) Dicing through the lid wafer to expose bonding pads. h) Dicing of ROIC wafer into individual chips. i) The vacuum packaged FPA is mounted into a ceramic package. Adapted from [75].

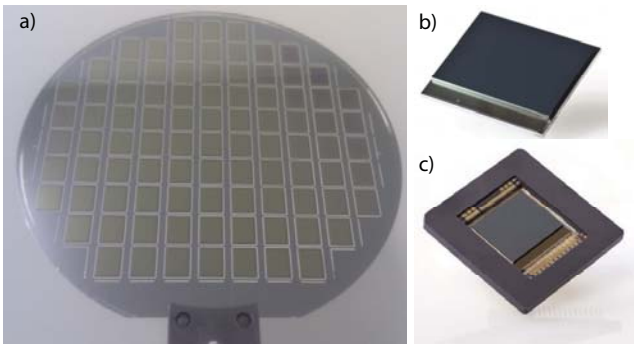

Figure 2.18: a) Wafer-level vacuum packaged FPAs. b)Individual vacuum packaged FPA. c) Vacuum packaged die mounted in ceramic package. Taken from [75]

2.5 Discussion

The heterogeneous integration of uncooled and packaged resistive microbolometer-based LWIR FPAs is a promising approach to both reach aggressive performance targets and potentially low-cost fabrication. The performance of modern uncooled FPAs is typically below 30 mK for 25 µm pixel pitch designs and the use of heterogeneously integrated low noise and high TCR materials opens up for comparable or even better performance. No unorthodox materials or processes are needed in the realization of heterogeneously integrated FPAs. This compares favorably with VO_x-based approaches that requires unconventional deposition and etching processes.

Chapter 3

Evaluation of bond energy in adhesive wafer bonding

3.1 Introduction

In adhesive wafer bonding, an adhesive layer is deposited on one or both of the wafers with a suitable deposition technique (i.e spin coating, laminating, spraying etc.). The wafers are brought into intimate contact and the intermediate adhesive is typically cured by the application of heat and pressure in a specialized wafer bonding tool [76]. Advantages of adhesive wafer bonding include IC compatibility due to relatively low adhesive curing temperatures, a wide design window for the thicknesses of the deposited polymer coating and an insensitivity to particles and surface topology due to plastic reflow and deformation of the polymer adhesive at the bond interface [76]. A large variety of different substrate materials can be joined with adhesive wafer bonding since the typical polymers used adhere to most materials [76]. Adhesive wafer bonding is the enabling technology used in the fabrication of uncooled LWIR FPAs in *Paper 1* and *Paper 2* and is also used to transfer and attach expanded arrays of dies as described in *Paper 6* and alumina filters as described in *Paper 5*. *Paper 3* presents an in-depth description in how a nano-imprint resist can be used as a sacrificial adhesive for the fabrication of MEMS.

There are a vast variety of polymers that have been evaluated for adhesive wafer bonding, such as polyimides [77, 78], epoxies [79–81], benzocyclobutene (BCB) [82–86], UV-curable epoxies (i.e SU8) [87–92] and nano-imprint resists [76, 93]. Ease of application, bond interface quality, bond hermeticity, curing temperature and the bond strength are important parameters to consider when choosing a polymer adhesive [76]. Furthermore, some adhesives are permanent structural layers that are hard to remove (i.e BCB), while other adhesives have the capability to be used as sacrificial material layers (i.e mr-I 9000XP-series).

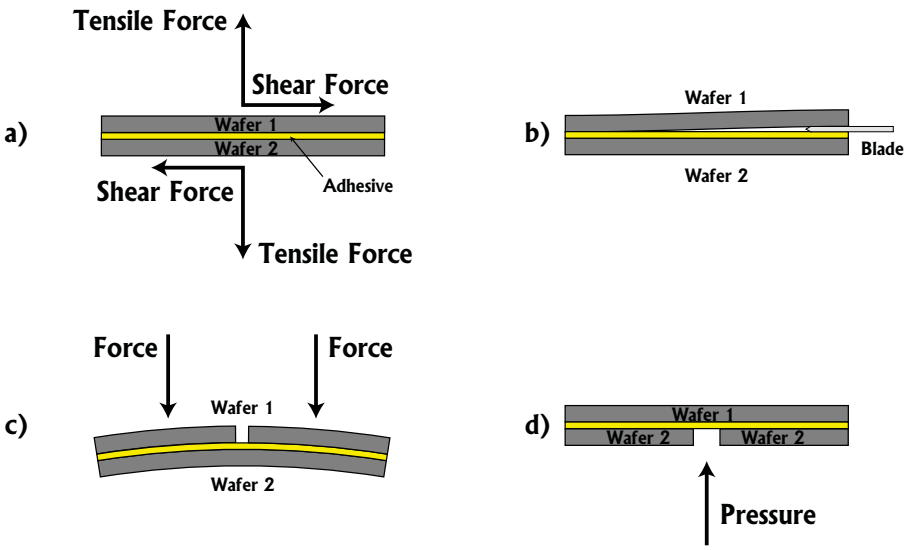

Figure 3.1: a) Tensile and shear load tests. b) Crack opening tests. c) Four-point bending tests. d) Blister tests.

3.2 Methods for evaluating bond energy

Figure 3.1 illustrates four different techniques to estimate the bond strength. These techniques are by their very nature destructive. Tests based on tensile loading of the bond interface measures the tensile strength of a bond while tests based on controlled opening cracks and blister tests measures the surface energies of bonds.

3.2.1 Tensile and shear load measurements

This method is depicted in Figure 3.1 a and is based on pulling apart bonded samples by the application of tensile of shear forces. The tensile strength is defined as the fracture force divided by the sample area (unit, Pa) [76].

3.2.2 Crack opening method

This technique is based on introducing a sharp spacer (i.e razor blade) of a defined thickness into the bond interface of a sample (Figure 3.1 b). The bond will delaminate and the length of the resulting crack is measured. Information about the thicknesses of the bonded plates, the material parameters and the length of the delaminated crack is related to the surface bond energy (unit, J/m^2) [76].

3.2.3 Four-point bending tests

This method is illustrated in Figure 3.1 c and is based on rectangular samples, where one of the substrates contains a pre-fabricated slit. The rectangular sample is put in a fixture and loads are applied on fixed distances from the slit. The load-induced displacement is recorded. As the load is applied, the bending moment in the slit area increases. When the applied load reaches a critical value, a bending-induced crack initiates at the tip of the slit and propagates along the weak interface. The measurement data is used together with mechanical beam theory to derive an expression for the surface bond energy [83].

3.2.4 Blister tests

The test sample consists of a lid, bonded to a substrate with a hole (Figure 3.1 d). The substrate with the hole is fixed and attached to a pressure reservoir. The pressure in the reservoir is increased until the lid is delaminated from the fixed substrate. The critical pressure to drive the delamination is mathematically related to the bond energy [94].

3.3 Blister test evaluation platform

Paper 4 introduces a platform that was used for blister test evaluations of the bond energy for samples bonded with different polymer adhesives. The platform is depicted in Figure 3.2 a and b. It is based upon two Si wafers adhesively bonded to each other, where one of the wafer has pre-etched through holes. The bonded wafer stack is diced and placed into a holder, followed by the application of increased gas pressure from the backside until the lid delaminates.

The pressure at the start of delamination (burst pressure) can be converted into a bond energy per unit area according to [94]:

$$P_{cr} = \left(\frac{32 E \gamma_a h^3}{3a^4(1-\nu^2)} \right)^{\frac{1}{2}}$$

Where P_{cr} is the burst pressure, h is the wafer thickness of the lid, a is the radius of the circular cavity, ν is the Poisson's ratio, E is the Young's modulus for Si and γ_a is the adhesive fracture energy per unit area. The equation is deduced from Clapeiron's theorem [94] and holds for diaphragms that deform elastically and that are thin compared to the diameter of the circular cavity. The critical pressure needed to delaminate the lid decreases with increased diameter of the circular cavity. The highest pressure needed for delamination is thus reached when delamination of the lid starts, thereby driving the delamination to the edges of the lid, where it is torn off from the die.

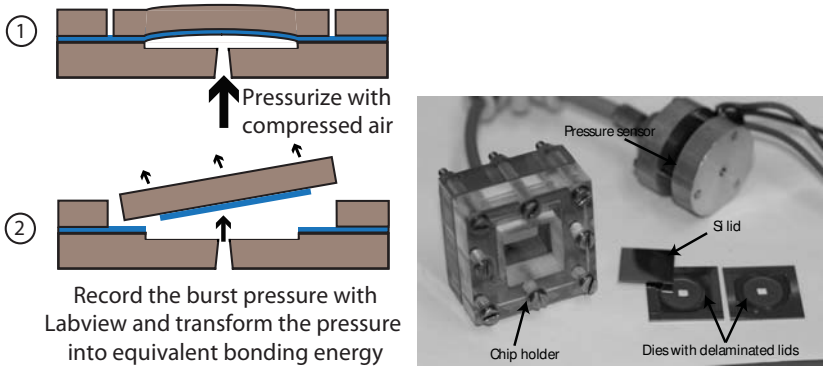

Figure 3.2: Blister test setup. Image to the left: 1) Adhesively bonded Si lids are pressurized from the backside with compressed air. 2) The lids are delaminated and the critical burst pressure is recorded. Image to the right: Fabricated samples together with the fixture used to pressurize the die from the backside. Taken from [95]

3.4 Tabulated bond energies

Estimated bond energies for evaluated adhesive bond polymers are presented in Table 3.1.

3.5 Discussion

A blister test platform has been introduced to evaluate the bond energies of adhesives used in wafer bonding. The results are comparable to values found in literature when evaluating the bond energy with other methods [83]. This verifies the validity of the method and provides the bond energies for adhesive bonding using mr-I 9150XP and OSTE+ as the adhesive. The nano-imprint resist mr-I 9150XP exhibited a bonding energy of around 2 J/m^2 while OSTE+ reached a bond energy of 20 J/m^2 for the best blend. This is less than BCB but still sufficiently strong for most applications.

Specimen	Bond Temperature [°C]	Adhesion promoter	Lid thickness [µm]	Layer thickness [µm]	Number of samples	Mean bond energy [J/m^2]	Standard deviation [J/m^2]
BCB	250	Yes	125	2.4	10	35	7.6
BCB	250	No	306	2.4	11	5.7	0.4
mr-I 9150XP	200	Yes	304	1.5	11	0.2	0.4
mr-I 9150XP	200	No	302	1.2	10	2.4	0.5
mr-I 9150XP	200	No	300	1.5	11	1.5	0.6
mr-I 9150XP	200	No	303	2.3	8	1.7	0.8
OSTE+ (blend 1) undiluted	90	No	302	Not measured	11	20	6.8
OSTE+ (blend 1) diluted 1:1 by weight with toluene	90	No	132	3.9	11	2.2	2.0
OSTE+ (blend 2) undiluted	90	No	304	4.4	11	2.1	0.5
OSTE+ (blend 2) diluted 1:1 by weight with toluene	90	No	306	2.9	11	2.9	0.9

Table 3.1: Adhesive bond energies for different polymers and process parameters. Taken from [95]

Chapter 4

Heterogeneous integration of nanoporous membranes

4.1 Introduction

Controlled electrochemical processing methods have opened up for the fabrication of wafer-sized nano-porous membranes in Si and alumina [96,97]. The electrochemical processes that are utilized enable controlled pore-size tailoring in a range from nm to μm over wafer-scale samples. Nano-porous membranes have found use in numerous applications such as filtering, sequencing, amplification and drug delivery due to their ability to discriminate molecules based on size and interaction [96, 98–100]. Furthermore, nanoporous materials are characterized by a very large internal surface area, which make them suitable for binding surfaces in biosensing [101,102]. However, the specialized electrochemical fabrication method of the membranes is very different from the surface machining of Si and glass or the plastic molding processes that are used for manufacturing typical microfluidic components. This incompatibility limits the appeal of monolithic integration of porous materials into systems, although there are reports of *in situ*-forming of porous Si in microchannels [103].

Transfer bonding of separately fabricated nano-porous membranes onto pre-fabricated microfluidic systems solves this incompatibility problem and opens up for optimal fabrication of the needed sub-components. Heterogeneous integration by transfer bonding has been used for the transfer of porous Si Bragg mirrors onto a flexible polymer sheet using an intermediate PDMS stamp [104] and for the transfer of a porous Si waveguide onto a glass substrate [105, 106]. Presently used methods for heterogeneous integration of separate nano-porous membranes include clamping and gluing [107, 108]. These two methods tend to be low-yielding since the extremely fragile membranes tend to break when they are clamped and they are prone to clogging when glued due to the capillary action of the porous membranes. The method that is presented in *Paper 5* use dry adhesive chip scale

bonding with OSTE+ (from Mercene Labs AB) to transfer fragile nano-porous Si and alumina membranes for filtering applications. This solves the fragility and clogging problem when attaching the membranes on a holder or use them as a component in microfluidic systems. OSTE+ is a dual-cure off-stoichiometry thiol-ene-epoxy polymer material. The first curing step is initiated by UV-exposure and results in a chemical reaction between thiol and allyl monomers in OSTE+. This results in a partially polymerized soft solid material. The surface of the partially cured OSTE+ is ideal for direct dry bonding of different materials, since its softness makes it compliant to surface irregularities [109]. It is this property and mode that is used for the dry bonding of prefabricated nano-porous membranes. A second curing step, where the thiol- and epoxy-components of OSTE+ reacts, hardens the polymer. This reaction starts immediately after mixing, but proceeds slowly at room temperature. The temperature can be increased to 70 °C for 2 h to accelerate the second curing step. After the second cure, the OSTE+ polymer is stiff with a Young's modulus of 1.2 GPa. The OSTE+ chemistry and reaction mechanisms are described in [109].

4.2 OSTE+ enabled transfer bonding of porous membranes

4.2.1 Transfer of nano-porous membranes to OSTE+ chips

One of the heterogeneous transfer methods presented in *Paper 5* is based on molding partially cured OSTE+ chips containing holes. Figure 4.1 b shows the steps needed to realize molded partially cured OSTE+ chips. A PDMS mold is prepared and defines the outer chip dimensions of $15 \times 15 \times 1$ mm^3. 800 µm diameter steel pins are used to define vias through the chip. To avoid the formation of a residual squeeze-film on top of the pins, a matching shadow mask printed onto a 1 mm thick polycarbonate sheet was aligned on top of the mold. The OSTE+ chip was peeled off from the mold after the initial UV curing. At this stage, the surface of the OSTE+ is dry and sticky due to the presence of unreacted epoxy groups.

Both nano-porous alumina membranes and porous Si membranes were bonded to the chips. The basic outline of the transfer is depicted in Figure 4.1 c. The porous Si membranes were created in Si wafers, as shown in Figure 4.1 a and were delivered in the form of 6 mm diameter and 30 µm thick porous Si membranes with 50% porosity and a pore size of 70 nm. The membranes are still partially attached to the Si substrate, although not directly underneath due to electrochemical underetching of the membrane. The membrane was transferred by stamping the OSTE+ chip onto the porous Si and breaking it loose from the Si substrate followed by curing the chips with transferred porous Si membranes. Nano-porous alumina membranes (Whatman Anopore^{TM}) were transferred in a similar way, with the difference that these are less fragile and handled individually. Figure 4.2 shows images of OSTE+ polymer chips with transferred porous Si and alumina membranes.

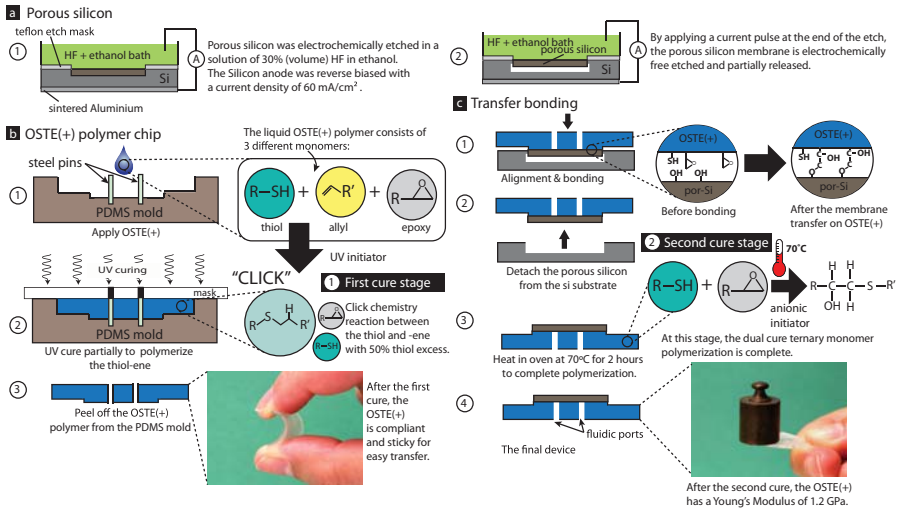

Figure 4.1: The fabrication sequence of OSTE+ polymer chips with dry bonded porous silicon membranes: a) The porous silicon etching. b) Casting of the OSTE+ chip, by the first curing step. c) Dry transfer bonding of the porous silicon membrane onto the OSTE+ chip, and second stage cure. Taken from [109].

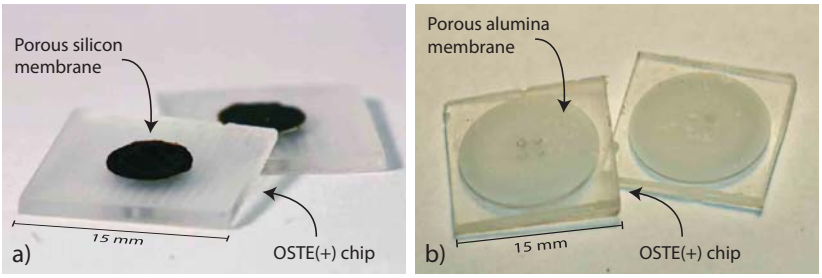

Figure 4.2: Photographs showing OSTE+ polymer chips with bonded: a) porous silicon membranes, and b) porous alumina membranes. Taken from [109].

4.2.2 Transfer bonding of porous alumina membranes to Si chips

Another approach, presented in *Paper 5*, consists of transferring 13 mm diameter porous alumina membranes (Whatman Anopore^{TM} 200) onto a 100 mm diameter and 300 μm thick microstructured Si wafer. This transfer scheme is depicted in Figure 4.3. It starts with KOH etching of through holes in a Si wafer (Figure 4.3 a-c). This creates small arrays of, in total, 16 square vias with a side length of 64 μm and a total membrane flow area of approximately 0.1 mm^2. Next, the wafer was partially diced to create cleaving lines for future separation of individual chips (Figure 4.3 d). The micromachined Si wafer was dipped in isocyanate silane, to improve the wetting of the silicon surface with the OSTE+ prepolymer. This was followed by washing the wafer thoroughly with toluene, and oven baking at 110 °C for 10 minutes (Figure 4.3 e). Blue tape was attached to the backside of the wafer before a 10 μm thick layer of OSTE+ was spin-coated onto the Si surface (Figure 4.3 f). The first curing stage was triggered by exposing the wafer to UV-light in a mask aligner (Figure 4.3 g). A mask was used to avoid exposing the holes to the UV-triggered curing. A development step in toluene removed unwanted OSTE+ from the hole region (Figure 4.3 h). The result after this step is a micromachined Si wafer with a structured layer of partially cured OSTE+ on top. Alumina membranes are batch transferred to the Si wafer by pressing the Si wafer towards a holder with distributed alumina membranes and the second thermal curing step commences by annealing the Si wafer with bonded membranes at 70 °C for 2 h (Figure 4.3 h). Figure 4.4 shows the resulting nano-porous membrane filters together with the holder used in the membrane transfer.

4.3 Filter characterization

The burst pressure and the flow resistance of bonded nano-porous membranes were evaluated. The filter chips were placed in a setup with DI water on one side of the membrane. The water was pressurized, to create a pressure gradient across the membrane, and a flow sensor measured the resulting filter throughput. The burst pressure was defined as the pressure at which the delamination occured between the OSTE+ bond interface and the nano-porous membrane. Figure 4.5 shows a schematic of the evaluation setup.

These results were compared to the flow through reference samples consisting of untreated porous alumina membranes clamped with PDMS gaskets to flat aluminum plates with either 480 or 650 μm diameter drilled apertures. This comparison was done to analyze if any clogging of the membranes had occured during the bonding process. A plot of different bonded alumina membranes and clamped reference membranes is shown in Figure 4.6. The flow rate is normalized with regards to the different opening areas in the samples. Extracted values of the normalized flow conductance of bonded membranes corresponds well with that of the clamped reference membranes, as well as with that specified by the

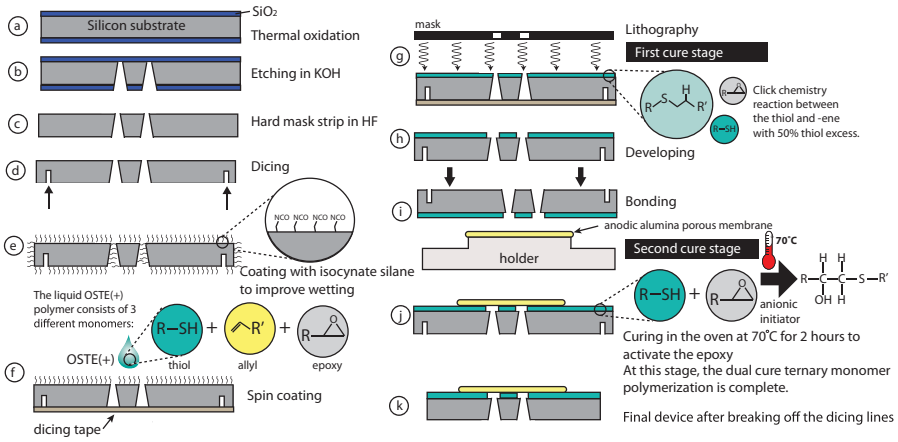

Figure 4.3: The wafer-scale fabrication process for the manufacturing of silicon chips with porous silicon membranes dry bonded using a 10 µm thick OSTE+ bonding layer. Taken from [109].

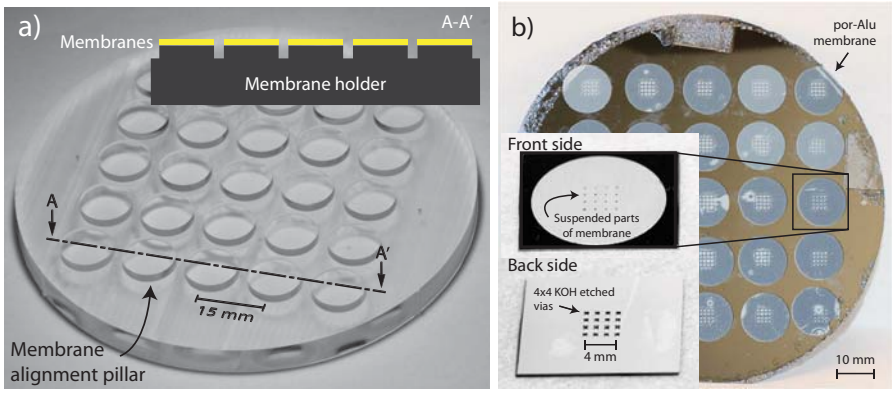

Figure 4.4: a) A photograph of the holder used to align and transfer 25 porous alumina membranes in parallel to a patterned silicon target wafer. The inset shows a schematic cross-section of the holder with aligned membranes. b) A photograph of the final wafer with transfer bonded porous alumina membranes. The insets show the front and the back of a single chip with a bonded porous alumina membrane. On the front side we see the 4×4 suspended areas of the membrane, and on the back side we see the corresponding KOH etched vias. Taken from [109].

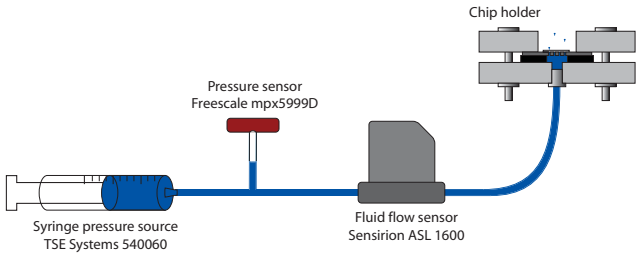

Figure 4.5: A schematic of the membrane flow evaluation setup. A syringe pump (TSE systems model 540060) was used as the liquid pressure source. A water-filled hose connects the pressure source to a gas pressure sensor (Freescale mpx5999D), through a water pillar into an air filled cavity, measuring the differential air pressure resulting from the applied liquid pressure. The pressure-driven flow through the tubing to the chip holder was gauged with a flow sensor (Sensirion ASL1600), and corresponds to the amount emitted through the openings of the porous membrane bonded to the chip. The chips were mounted in such a way that the bond interface was exposed to the applied pressure drop.

Substrate	Porous alumina membrane type	# vias	Via diam. [µm]	Flow area [mm^2]	Normalized flow conductance [$\frac{\mu l}{min \cdot kPa \cdot mm^2}$]	Burst pressure [kPa]
OSTE+	Anopore 100	4	800	0.5	1.3	520
Si	Anopore 200	16	64	0.1	1.8	750
Reference	Anopore 100	1	650	0.3	1.5	
Reference	Anopore 200	1	480	0.2	1.3	

Table 4.1: A summary of the experimental conditions: substrate type, membrane type, number of vias, and total open flow area and the results for: normalized flow conductance, and burst pressure. Taken from [109].

membrane producer (1.2 and 1.5 µ l/(min · kPa · mm^2), for Anopore 100 and 200, respectively) [109].. This indicates that no clogging has occurred during membrane transfer and bonding, thereby confirming the viability of the OSTE+ based dry bonding method.

Table 4.1 summarizes the conditions and results of the experiments.

4.4 Discussion

OSTE+ enabled dry adhesive bonding opens up for easy heterogeneous integration of nano-porous membranes into devices. It solves both the fragility problem (for clamped membranes) and the clogging problem (glued membranes) that has been experienced in the mounting of nano-porous membranes. The bond strength

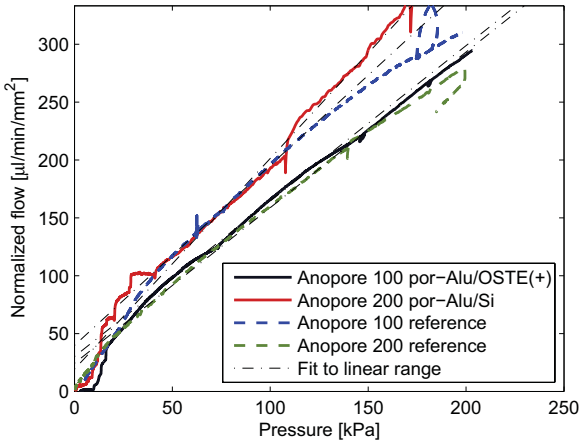

Figure 4.6: The membrane flow normalized by the flow area, as a function of the pressure drop over the membranes. Taken from [109].

of the fastened membranes is high (above 500 kPa) compared with the typical pressures experienced in microfluidic devices. This opens up for the use of similar heterogeneous integration of fragile membranes in microfluidic applications.

Chapter 5

Heterogeneous transfer of distributed die arrays

5.1 Introduction

One problem that is repeatedly confronted in heterogeneous integration is that dissimilar materials and devices are provided in different wafer sizes. For example, photonic components are made from compound semiconductor wafers that are typically less than 100 mm in diameter while commercial CMOS and MEMS production use wafer diameters of 200 mm and above [110]. The wafer size incompatibility limits the efficient use of wafer bonding in heterogeneous integration efforts. Furthermore, specialized materials are typically only needed in a small part of the chip footprint [110]. One solution for this kind of problems is to dice the smaller wafer into individual dies that are transferred to a target substrate, where further processing can commence to form integrated devices. A related technology is used in 2.5D SiP integration as described in Chapter 1, where individual components are flip-chip bonded to a Si interposer with prefabricated electrical interconnects. The placement of dies is accomplished with pick-and-place machines that sequentially pick up individual dies or chips and place them onto larger substrates [85,111–113]. This technique has found use in advanced packaging due to its precision and flexibility. Modern pick-and-place machines are able to place thousands of dies per hour with 10 µm accuracy and more than 10 000 dies per hour with more relaxed placement accuracy requirements [114–116]. Limitations of the method is coupled to the minimum die size that can be handled by the pick-and-place machine and the time requirement for massive die transfer. Surface stiction often dominates over gravitational forces for small sub-mm sized components and the components that need to be placed stick to the placement tool [117]. The total placement time scales linearly with the amount of dies to transfer and limits the pick-and-place viability when massive transfers of tens of thousands to hundreds of thousands of small dies are needed. Two alternative approaches have been

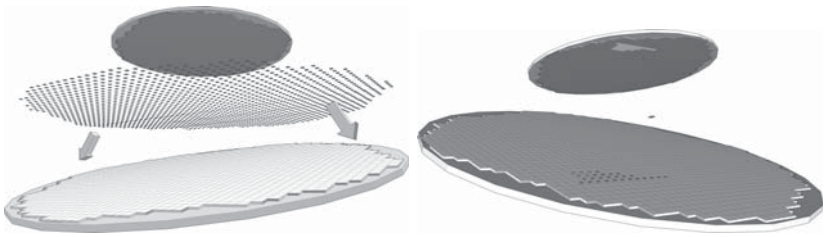

Figure 5.1: a) Parallel transfer of dies. b) Sequential pick-and-place assembly. Taken from [110]

developed for spreading large amounts of small dies onto larger substrates. These are based on either self-assembly methods or parallel transfer methods.

5.2 Self-assembly methods

Self-assembly of dies and components are possible across large substrate areas. Available methods typically utilize either shape-matching, surface energy minimization or magnetic- or electric-field-mediated self-assembly [117]. Methods based on shape-matching and surface energy minimization consist of structuring the dies and substrates in such a way that dies stick to preferred positions on the substrate. The basic arrangement consist of randomly spreading components onto a structured substrate. Shaking the substrate enable the dies to move around until they find preferred positions that minimizes the surface interfacial energy or get placed into structured cavities that fit with the dies size. Substrate structuring methods include: Liquid solder-based self-assembly where specific solder pads on the substrate matches metal pads on the dies [118, 119], recess-based self-assembly methods where only dies with the right size and shape fits into etched recesses in the target substrate [120] and capillary force-directed self-assembly that uses hydrophilic/hydrophobic surface patterns [121]. These methods are also used in combinations. For example, Stauth and Parviz presented a heterogeneous self-assembly process with shape matching where small dies or components are introduced into a liquid medium [122]. Here, a structured wafer with solder inside shaped wells is put into the liquid and self-assembly occurs as the components first fall into complementarily shaped wells and then become bound by the capillary forces with the molten solder. In magnetic- and electric-field-mediated self-assembly, static magnetic and electric fields are used to assist the self-assembly of components on substrates [117, 123–125].

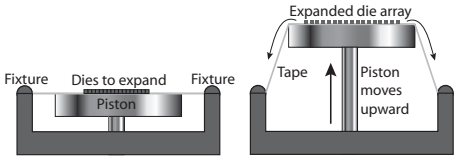

Figure 5.2: The dies are separated using a ULTRON UH-130 matrix expander. A piston moves vertically towards a tape that is attached to a fixture. The piston movement stretches out and expands the tape to the sides and thereby separates the dies. Taken from [110]

5.3 Parallel transfer methods

These methods are based on expanding dies on flexible substrates or dies connected with spring structures from each other. The expanded flexible substrate is fastened to a target substrate, resulting in distributed dies. For example, an elaborate silicon spiral spring transfer method was reported by Huang where small silicon springs connect mechanically and electrically between free-etched dies on the wafer level [126]. All of the dies can then be expanded from each other by extending the spiral springs. Another method that has been reported is based on the expansion of a hemispherically-shaped PDMS sheet so that it is flattened. An array of photodetectors were fastened and the PDMS-sheet was released and regained its hemispherical shape, now with distributed photodetectors attached [127].

Paper 6 reports on a parallel transfer method that is based on the stretchable properties of a regular dicing tape. This opens up for a transfer method that allows for fast and parallel transfer of a large number of dies from a small wafer format to a larger target wafer. First, the smaller wafer consisting of the material to be transferred is diced into individual dies. This is followed by radially stretching the tape to a specific target format (Figure 5.2), which results in a lateral separation of the dies on the tape. The expanded die matrix is then transferred and bonded to a designated target wafer with BCB-based adhesive wafer bonding. Figure 5.3 depicts the detailed process steps. Expanded arrays containing approximately 30 000 dies with a size of 460x460 μm^2 each, are presented in Figure 5.4.

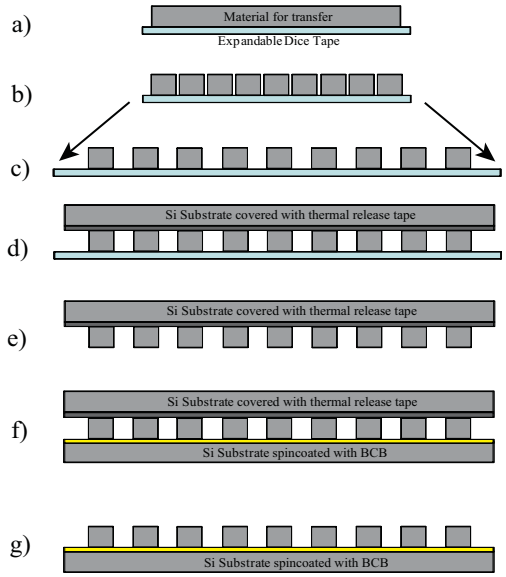

Figure 5.3: Process sequence of the transfer method. a) The wafer is placed on expandable dicing tape. b) The wafer is diced into dies. c) The tape is expanded to increase the distance between the dies. d) The dies are transferred to a temporary silicon substrate covered with thermal release tape. e) The dicing tape is removed. f) The dies are transferred to a 200 mm target wafer with adhesive wafer bonding. g) The temporary silicon substrate is removed from the dies. The results are separated dies that are transferred to a larger target wafer. Taken from [110]

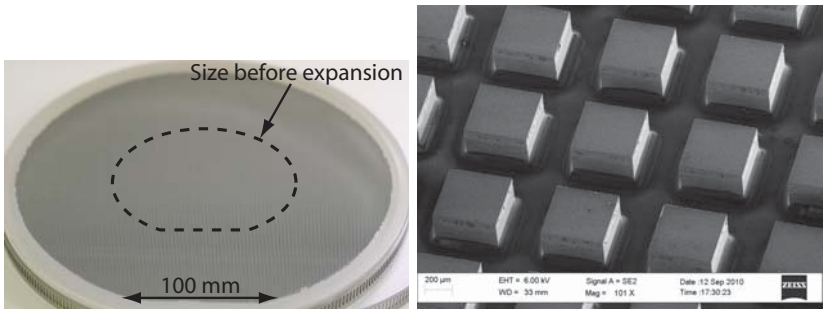

Figure 5.4: a) Image of expanded and diced 100 mm wafer on an expandable UV release dicing tape. The dicing tape is fastened to a plastic carrier ring. The expanded array consists of approximately 30 000 dies. b) SEM image of transferred 460x460 μm^2 on a 200 mm diameter Si wafer using BCB adhesive bonding. Taken from [110]

5.4 Discussion

The expansion and transfer of diced wafers onto a larger wafer, as presented in *Paper 6*, is a simple, fast and potentially cost-efficient heterogeneous integration method to map MEMS or photonic material onto larger target substrates. Further development and improvements on the obtained die positioning accuracies are needed to make the method feasible for commercial manufacturing. This is due to problems with non-uniform expansion of the elastic tape that results in mismatches in the mapping on the target wafer. This could be alleviated, for example, by implementing automatic feedback during the matrix expansion to better control the behavior of the expanding tape.

Chapter 6

Piezoresistive graphene-based pressure sensor

6.1 Introduction

The signal output of micromachined pressure sensors typically depends on the applied pressure (p) as compared to a reference pressure (p_{ref}) across a diaphragm. Three different classifications of pressure sensors are commonly used depending on the arrangement of the reference pressure. *Absolute pressure sensors* are references to a stable vacuum pressure, *gauge pressure sensors* are referenced to a stable ambient atmospheric pressure and *differential pressure sensors* measure the pressure p compared with a freely moving reference pressure p_{ref} on the other side of the diaphragm. Piezoresistive, capacitive, resonant and optical sensing methods have been used to measure the pressure-induced deflections of the diaphragms [128]. Bulk micromachining of monocrystalline Si or surface micromachining of polycrystalline and amorphous materials (poly-Si, metals and SiN) are typically used as diaphragms of pressure sensors [128]. The sensing elements in piezoresistive Si pressure sensors are usually made by ion implantation to form piezoresistive Si strain gauges in the diaphragm. The pressure differential across the diaphragm causes a deflection. The deflection of the diaphragm induces stresses across the piezoresistor and results in a resistance change that is measured.

In *Paper 7* a graphene membrane is used as both the diaphragm and the piezoresistor in a gauge pressure sensor configuration. Larger layers of graphene are either fabricated epitaxially by CVD of hydrocarbons on metal substrates or by thermal decomposition of SiC [129]. These processes take place at temperatures of 800 °C up to above 1000 °C, which makes it incompatible with IC fabrication [130]. Therefore, heterogeneous integration techniques are desired for the use of graphene layers in emerging graphene-based NEMS devices. In *Paper 7*, graphene is placed on a SiO_2-surface above a small (6×64 μm^2) pre-etched cavity. Figure 6.1 c depicts a device with marked layers and Figure 6.1 d shows a SEM image of a fabricated

device.

Monolayer graphene is characterized by its high carrier mobility [131,132] and its high Young's modulus of around 1 TPa for both exfoliated graphene and chemical vapor deposited (CVD) graphene [133, 134]. Furthermore, graphene is stretchable to approximately 20% of its length without breaking [135] and strongly adheres to SiO_2 surfaces [136]. Another useful characteristic is the near impermeability of graphene to gasses, including helium [137]. Graphene exhibit a piezoresistive effect when exposed to strain due to strain-induced changes in its electronic band structure [138].

6.2 Chip-scale heterogeneous transfer of graphene onto SiO_2

Figure 6.1 a and b depict the steps in the fabrication of the pressure sensor. The devices are fabricated in 1.5 μm thermally grown SiO_2 on Si substrates. Rectangular 6×64 μm^2 cavities with a depth of 650 nm are etched into the SiO_2. Next, buried contacts are defined by etching 640 nm deep contact areas into the SiO_2 that are filled with 160 nm Ti and 500 nm Au to create buried gold contacts. Commercially available CVD-based graphene films on Cu-foils are used. For the layer transfer a polymer is spin coated on to the graphene film in order to act as a mediator between the initial and final substrate. The Cu-foil is removed by wet etching, leaving a transferred graphene layer on the polymer. The graphene is pressed towards the SiO_2 on the prepared Si wafer. The graphene strongly adheres to SiO_2 due to a van der Waals bond mechanism [136]. The polymer is stripped, leaving a transferred graphene layer, covering the etched cavities in the SiO_2. The graphene is etched with an O_2 plasma into the desired shape after masking with a photoresist. The photoresist is finally removed with acetone.

6.3 Discussion

Heterogeneous integration of graphene and the evaluation of it as a piezoresistive material resulted in a measured gauge factor of 2.92 [139]. The sensitivity per unit area of the fabricated graphene sensor is about 20 to 100s of times higher than that of conventional piezoresistive Si-based pressure sensors [139]. One problem that was observed in our *Work* is that the electrical properties of the graphene are affected by the level of humidity and the surrounding gas. This is believed to be due to adsorption of molecules on the graphene surface, that since the graphene in essence is a 2-D material drastically influences its electrically conductive properties. This was alleviated by conducting all experiments and characterization in an inert nitrogen atmosphere.

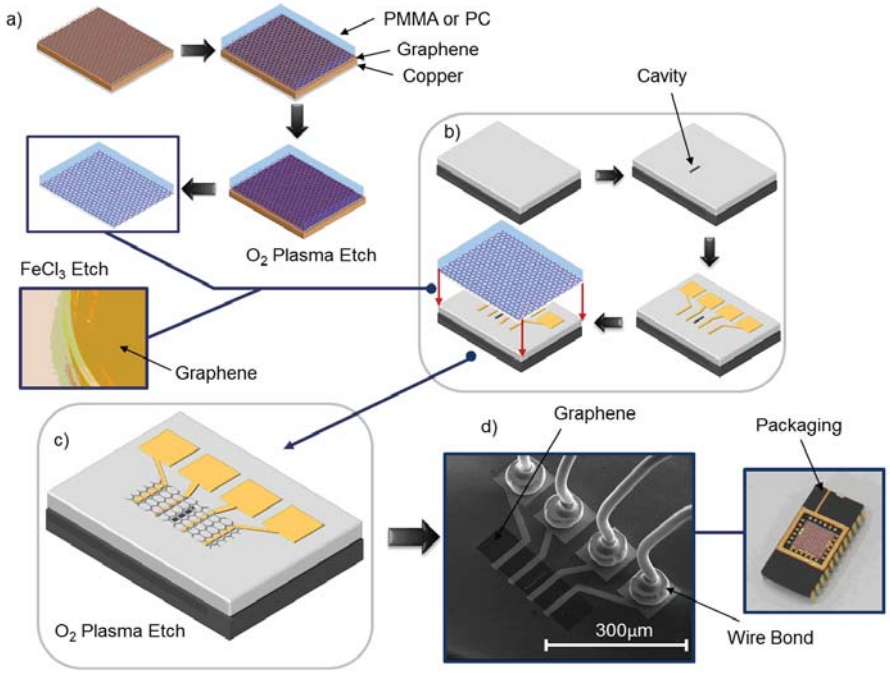

Figure 6.1: a) Depiction of the graphene transfer process. Graphene is grown using chemical vapor deposition (CVD) onto both sides of a copper substrate. A layer of PMMA or polycarbonate is applied to one side of the copper foil. Graphene is etched from the back side of the copper foil using a O_2 plasma. Finally, the copper is removed by etching in $FeCl_3$. b) shows the fabrication sequence of the Si substrate and the corresponding transfer of graphene onto the substrate. c) Depiction of a graphene-based pressure sensor with marked layers. d) The devices are packaged and wire bonded. Taken from [139]

Chapter 7

Conclusions

Different methods for heterogeneous integration of materials into microsystems have been presented.

The first method, based on adhesive wafer bonding, was used for the implementation of LWIR FPAs in an IC-compatible process. The second and third heterogeneous material integration methods presented a non-destructive way to integrate nano-porous membranes into microfluidic components and a way to transfer massive amounts of distributed dies between different wafer formats. Both of these methods use adhesive wafer bonding for the attachment on the target substrate. The last method demonstrates how heterogeneous integration can be used to integrate a mono-layer of graphene into a pressure sensor.

The presented thesis has demonstrated that heterogeneous integration methods are a feasible approach for integrating SiGe QW thermistor material, nano-porous membranes and graphene-layers. In common among these materials and components are the specialized fabrication procedures that limits the viability of monolithic integration approaches. Furthermore, a blister test method to evaluate adhesive bond energies was presented.

Appendix A

Resistive bolometer theory

The goal of this section is to present a derivation of $NETD$ for a resistive microbolometer-based camera system. Only the most important steps are derived. The interested reader is referred to [30] for details.

A.1 Optical system

Figure A.1 depicts the optical system from the viewed object to the infrared sensor. The radiant flux on the entrance pupil from the small area dA_1 is given by [30]:

$$\Phi_1 = dA_1 \pi L_{object} sin(\beta_1)^2 \tag{A.1}$$

Likewise, the projected radiant flux on the small sensor area A_2 is given by:

$$\Phi_2 = dA_2 \pi L_{lens} sin(\beta_2)^2 \tag{A.2}$$

The total radiant flux on both sides of an optical system without losses are equal, $\Phi_1 = \Phi_2$. The optical system is governed by Abbe's sine law (Eq. A.3):

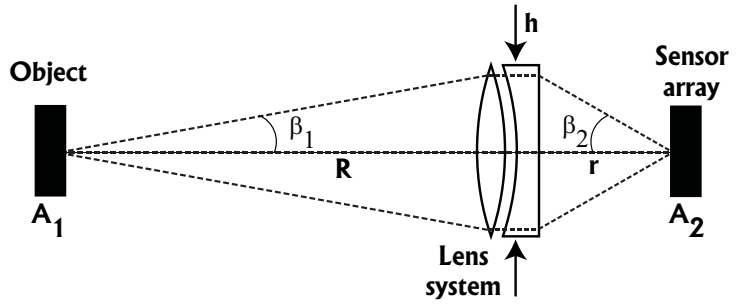

Figure A.1: Depiction of the optical system. Radiation path from object to sensor.

Table A.1: Microbolometer parameters

Parameter	Unit	Description
TCR	$\frac{\%}{K}$	Temperature coefficient of resistance
β	-	Bolometer fill factor
α	-	Relative infrared absorbtion coefficient
R_0	Ω	Resistance of microbolometer at reference temperature
I_{bias}	A	Biasing current
G	$\frac{W}{K}$	Thermal conductance
C	$\frac{J}{K}$	Thermal mass of microbolometer
ω	$rad \cdot s^{-1}$	Modulation frequency
$\tau = \frac{C}{G}$	s	Thermal time constant
$\tilde{\nu_R}$	V	Total noise voltage
$\tilde{\nu_{nR}}$	$\frac{V}{\sqrt{Hz}}$	Normalized total noise voltage
A_{pixel}	m^2	Pixel area
$F_\#$	-	Optics F-number.
τ_{opt}	-	Relative transmission of the IR optics
ϵ	-	Emissivity
L	$\frac{W}{sr \cdot m^2}$	Radiance
Φ	W	Radiant flux
M	$\frac{W}{m^2}$	Radiant exitance
E	$\frac{W}{m^2}$	Irradiance

$$dA_2 sin(\beta_2)^2 = dA_1 sin(\beta_1)^2 \tag{A.3}$$

Equation A.1 to A.3 results in that the radiance, L, is equal on both sides of the optical system:

$$L_{object} = L_{lens} \tag{A.4}$$

The meaning of this result is that the irradiance impinging of the sensor is governed by the radiance L_{object} of the object and the parameters of the optical system. The distance between the object and camera system is of no importance. The radiance of the object is in turn coupled to the temperature dependent blackbody radiant exitance, ϵM, where ϵ is the emissivity. The irradiance, E, is defined as the radiant flux divided by the sensor area and is given in Equation A.6.

$$L_{object} = \frac{\epsilon M}{\pi} \tag{A.5}$$

$$E = \frac{\Phi_2}{dA_2} = \epsilon M sin(\beta_2)^2 \tag{A.6}$$

The f-number, $F_\#$, is defined as r/h (see Figure A.1). We also know that

$$sin(\beta_2)^2 = \frac{\frac{h^2}{4}}{\frac{h^2}{4} + r^2} = \frac{1}{4{F_\#}^2 + 1} \tag{A.7}$$

Assume that the transmission of the optical system is τ_{opt}. Equation A.6 for the irradiance together with Equation A.7 for an optical system with the optical transmission τ_{opt} is then:

$$E = \frac{\tau_{opt}\epsilon M}{4{F_\#}^2 + 1} \tag{A.8}$$

A.1.1 Resistive microbolometer analysis

The responsivity is given by Equation A.9 where ΔV is the voltage response for the exchanged radiant flux $\Delta\Phi$, which is the incoming radiant flux minus the outgoing radiant flux at a reference temperature.

$$\Re_V = \frac{\Delta V}{\Delta\Phi} \tag{A.9}$$

The absorption coefficient α is the amount of the irradiance between the wavelengths λ_1 to λ_2 that is picked up by the small sensor element. The sensor element area βA_{pixel} then absorbs (using Equation A.8):

$$\Phi_{pixel} = \frac{\beta A_{pixel}}{4{F_\#}^2 + 1} \int_{\lambda_1}^{\lambda_2} \tau_{opt}\alpha\epsilon M_\lambda d\lambda \tag{A.10}$$

where the radiant exitance, M, has been replaced with the spectral radiant exitance M_λ. Of interest is the sensor voltage response, $\Re_T$, for changes in the viewed object temperature T. This is given by:

$$\Delta V = \Delta\Phi\Re_V \tag{A.11}$$

$$\Delta\Phi = \Phi_{pixel} - \Phi_{ref} \tag{A.12}$$

$$\Re_T = \frac{\partial\Delta V}{\partial T} = \frac{\beta A_{pixel}\Re_V}{4{F_\#}^2 + 1} \int_{\lambda_1}^{\lambda_2} \tau_{opt}\alpha\epsilon \frac{\partial M_\lambda}{\partial T} d\lambda \tag{A.13}$$

$NETD$ is defined as the object temperature difference that results in a voltage response equal to the voltage noise level. It is described mathematically by using Equation A.13:

$$NETD = \frac{\tilde{\nu_R}}{\Re_T} = \frac{\tilde{\nu_R}(4{F_\#}^2 + 1)}{\beta A_{pixel}\Re_V} \frac{1}{\int_{\lambda_1}^{\lambda_2} \tau_{opt}\alpha\epsilon \frac{\partial M_\lambda}{\partial T} d\lambda} \tag{A.14}$$

while the noise equivalent power NEP and the specific detectivity D^* is given by

$$NEP = \frac{\tilde{\nu_R}}{\Re_V} \tag{A.15}$$

$$D^* = \frac{\sqrt{A_{pixel}}}{\tilde{\nu_{nR}}} \Re_V \tag{A.16}$$

where $\tilde{\nu_{nR}}$ is the total noise voltage, normalized with regards to the system bandwidth.

A.2 Thermal microbolometer model

The microbolometer temperature response due to irradiation is given by the differential equation:

$$C_{th} \frac{\partial \Delta T}{\partial t} = \Delta \Phi_{abs} - G_{th} \Delta T \tag{A.17}$$

where $\Delta \Phi_{abs}$ is the radiant flux that the sensor absorbs. Equation A.17 has the following solution in the frequency domain (assuming harmonic excitation by the radiant flux $\Delta \Phi_{abs} e^{j\omega t}$):

$$\Delta T(\omega) = \frac{\Delta \Phi_{abs}}{G_{th}} \frac{1}{1 + j\omega\tau} \tag{A.18}$$

$$\tau = \frac{C_{th}}{G_{th}} \tag{A.19}$$

$$|\Delta T(\omega)| = \frac{\Delta \Phi_{abs}}{G_{th}} \frac{1}{\sqrt{1 + \omega^2 \tau^2}} \tag{A.20}$$

where the thermal time constant τ is introduced. The temperature response is modulated by the frequency of the irradiation and behaves like a thermal low pass filter of the impinging irradiance on the sensor. The responsivity is defined as the voltage response relative to the irradiance and is given by Equation A.9. The signal response ΔV is a function of TCR, the bolometer resistance R_0, the biasing current I_{bias} and the temperature deviation from the reference temperature ΔT.

$$\Delta V = TCR \; R_0 \; I_{bias} \; \Delta T \tag{A.21}$$

The following expression for $\Re_V$ results by combining Equation A.9, A.20 and A.21.

$$\Re_V = \frac{TCR \; R_0 \; I_{bias}}{G_{th} \sqrt{1 + \omega^2 \tau^2}} \tag{A.22}$$

A.3 Noise equivalent temperature difference

Putting Equation A.14 together with A.22 results in the following expression for the $NETD$ of a microbolometer:

$$NETD = \frac{4{F_{\#}}^2 + 1}{\beta A_{pixel}} \frac{\tilde{\nu_R}}{\int_{\lambda_1}^{\lambda_2} \tau_{opt} \alpha \epsilon \frac{\partial M_\lambda}{\partial T} d\lambda} \frac{G_{th}\sqrt{1+\omega^2\tau^2}}{TCR\ R_0\ I_{bias}} \tag{A.23}$$

It is obvious from Equation A.23 that $NETD$ is minimized by minimizing the total voltage noise $\tilde{\nu_R}$ and the thermal conductance G_{th} while maximizing the TCR, optical transmission τ_{opt} and the absorption coefficient α. A larger biasing current I_{bias} also results in a lower $NETD$ but has the drawback of larger Joule heating of the microbolometer (whose effect is not included in this analysis).

Summary of Appended Papers

Paper 1: *Heterogeneous 3D integration of 17 μm pitch Si/SiGe quantum well bolometer arrays for infrared imaging systems*

This paper reports on the realization of 17 μm × 17 μm pitch bolometer arrays for uncooled infrared imagers. Microbolometer arrays are typically based on deposited thin films on top of CMOS wafers that are surface-machined into sensor pixels. This paper instead focuses on the heterogeneous integration of monocrystalline Si/SiGe quantum-well-based thermistor material in a CMOS-compliant process using adhesive wafer bonding. The high-quality monocrystalline thermistor material opens up for potentially lower noise compared to commercially available uncooled microbolometer arrays together with a competitive temperature coefficient of resistance (TCR). Complications in the fabrication of stress-free bolometer legs and low-noise contacts are discussed and analyzed.

Paper 2: *Very large scale heterogeneous integration (VLSHI) and wafer-level vacuum packaging for infrared bolometer focal plane arrays*

This paper demonstrates new and improved fabrication and packaging technologies for next-generation IR imaging detectors based on uncooled IR bolometer focal plane arrays. The proposed technologies include very large scale heterogeneous integration for combining high-performance, SiGe quantum-well bolometers with electronic integrated read-out circuits and CMOS compatible wafer-level vacuum packing. The fabrication and characterization of bolometers with a pitch of 25 μm × 25 μm that are arranged on read-out-wafers in arrays with 320 × 240 pixels are presented. The proposed CMOS compatible wafer-level vacuum packaging technology uses Cu-Sn solid-liquid interdiffusion bonding. The presented technologies are suitable for implementation in cost-efficient fabless business models with the potential to bring about the cost reduction needed to enable low-cost IR imaging products for industrial, security and automotive applications.

Paper 3: *Wafer bonding with nano-imprint resists as sacrificial adhesive for fabrication of silicon-on-integrated-circuit (SOIC) wafers in 3D integration of MEMS and ICs*

In this paper, we present the use of thermosetting nano-imprint resists in adhesive wafer bonding. Detailed adhesive bonding process parameters are presented to achieve void-free, well-defined and uniform wafer bonding interfaces. Experiments have been performed to optimize the thickness control and uniformity of the nano-imprint resist layer in between the bonded wafers. In contrast to established polymer adhesives such as, e.g., BCB, nano-imprint resists as adhesives for wafer-to-wafer bonding are specifically suitable if the adhesive is intended as sacrificial material. This is often the case, e.g., in fabrication of silicon-on-integrated-circuit(SOIC) wafers for 3D integration of MEMS membrane structures on top of IC wafers.

Paper 4: *A comparative study of the bonding energy in adhesive wafer bonding*

Adhesion energies are determined for three different polymers currently used in adhesive wafer bonding of silicon wafers. The adhesion energies of the polymer off-stoichiometry thiol-ene-epoxy OSTE+ and the nano-imprint resist mr-I 9150XP are determined. The results are compared to the adhesion energies of wafers bonded with benzocyclobutene, both with and without adhesion promoter. The adhesion energies of the bonds are studied by blister tests, consisting of delaminating silicon lids bonded to silicon dies with etched circular cavities. The critical pressure needed for delamination is converted into an estimate of the bond adhesion energy. The fabrication of test dies and the evaluation method are described in detail.

Paper 5: *Dry adhesive bonding of nanoporous inorganic membranes to microfluidic devices using the OSTE(+) dual-cure polymer*

Two transfer bonding schemes are presented for the incorporation of fragile nanoporous inorganic membranes into microdevices. Both schemes rely on a novel dual-cure dry adhesive bonding method, enabled by a new polymer formulation: OSTE+, which can form bonds at room temperature. OSTE+ is a novel dual-cure ternary monomer system containing epoxy. After the first cure, the OSTE+ is soft and suitable for bonding, while during the second cure it stiffens and obtains a Young's modulus of 1.2 GPa. The ability of the epoxy to react with almost any dry surface provides a very versatile fabrication method. We demonstrate the transfer bonding of porous silicon and porous alumina membranes to polymeric microfluidic chips molded into OSTE+, and of porous alumina membranes to microstructured silicon wafers, by using the OSTE+ as a thin bonding layer. The device fabrication is described and the bond strength and membrane flow properties after bonding are evaluated together with a presentation of the OSTE+ dual cure mechanism.

Paper 6: *Batch Transfer of Radially Expanded Die Arrays for Heterogeneous Integration Using Different Wafer Sizes*

This paper reports on the realization of a novel method for batch transfer of multiple separate dies from a smaller substrate onto a larger wafer substrate by using a standard matrix expander in combination with an elastic dicing tape and adhesive wafer bonding. We demonstrate the expansion and transfer of about 30 000 dies from a 100-mm wafer format to a 200-mm wafer. Furthermore, multiple expansions of 100-mm wafers diced into 60 000 dies are evaluated to determine the position accuracy between different expansions. Fabrication, evaluation method, and results are presented.

Paper 7: *Electromechanical Piezoresistive Sensing in Suspended Graphene Membranes*

Monolayer graphene exhibits exceptional electronic and mechanical properties, making it a very promising material for nanoelectromechanical devices. The piezoresistive effect in graphene in a nanoelectromechanical membrane configuration is presented. This provides direct electrical readout of pressure to strain transduction. The device properties are compared with simulations and previously reported gauge factors and simulation values. The membrane in our experiment acts as a strain gauge independent of crystallographic orientation and allows for aggressive size scalability. When compared with conventional pressure sensors, the sensors have orders of magnitude higher sensitivity per unit area.

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