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Postprint

This is the accepted version of a paper presented at *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Transducers'2013, June 16-20, Barcelona.*

Citation for the original published paper:

Schröder, S., Fischer, A., Stemme, G., Niklaus, F. (2013)

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In: (ed.), *Transducers & Euroensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, 2013 (pp. 167-170). IEEE conference proceedings

<http://dx.doi.org/10.1109/Transducers.2013.6626728>

N.B. When citing this work, cite the original published paper.

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VERY HIGH ASPECT RATIO THROUGH SILICON VIAS (TSVS) USING WIRE BONDING

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ABSTRACT

This paper reports a fabrication approach for very high aspect ratio through silicon vias (TSVs). The metal filling of the through via holes is implemented by adapting standard wire bonding technology. TSVs with a diameter of 30 μm and aspect ratios between 10:1 and 20:1 have been fabricated. Basic electrical characterization and optical inspection have been conducted to verify the resistance and integrity of the metal and insulator filling of the TSV.

KEYWORDS

Metal through silicon vias, TSVs, high aspect ratio, wire bonding

INTRODUCTION

Traditional 2D integration approaches, such as Multi Chip Modules (MCM) combine different functional dies side-by-side in a single package or attach those to a common substrate. In contrast to system-on-chip solutions, where the entire functionality of a device is integrated in a single die, hybrid integration of multiple dies offer reduced development costs and faster time to market solutions [1-2]. Increasing demands on packaging in terms of size reduction and compactness, while simultaneously offering greater functionality, is shifting 2D integration towards three dimensional (3D) integration approaches. 3D integration features a great variety of advantages in terms of better performance, reduced power consumption and smaller foot print of the devices. TSVs are often regarded as a fundamental component in 3D integration, because TSVs enable truly vertical and shortest possible interconnection from the top to the bottom of stacked dies [3]. Various research activities are focusing on the development of reliable and cost-effective TSV manufacturing processes. Recently, TSVs are increasingly being implemented in consumer products, such as image sensors, gyroscopes and 3D LEDs [3-5].

The conductive core of TSVs can be fabricated by various techniques, such as electroplating of copper or tungsten, poly- or mono-crystalline silicon, conductive paste and solder filling as well as bulk material filling [6-12]. All these approaches for TSV filling suffer from specific manufacturing related drawbacks. Electroplating is a time consuming process and requires seed layers. Manufacturing of electroplated high aspect ratio TSVs remains a challenge due to imperfect via filling, e.g. void formation [7]. Manufacturing of poly- and mono-crystalline silicon TSVs offers only moderate electrical performance due to the maximum solubility of the dopant concentration in silicon, while mono-crystalline silicon TSVs set additionally restrictions for the resistivity of the silicon substrate [8]. Filling of TSVs using conductive paste is reported as a cost effective alternative approach,

Figure 1: Schematic illustration of the functional elements of a high aspect ratio TSV. The via hole is depicted in (a). The illustration in (b) shows the integrated metal core attached to the top of the substrate with a stitch bond. (c) depicts the final TSV, consisting of the metal core, which is surrounded by the insulator and contacted to a pad on the bottom of the TSV.

but has shown the risk of void and crack formation [9, 10]. Thus, novel and simplified TSV manufacturing approaches are needed to serve the increasing demands of TSV solutions.

Wire bonding is the dominating electrical interconnection method, which features a broad availability, high reliability, flexibility [11] and therefore also has been utilized for a variety of novel integration approaches in MEMS manufacturing [12]. Wire bonding offers a placement accuracy of 2.1 μm and high throughput of more than 20 wires per second [13]. Bond wires are high quality products, inherently void-free and contain only very few impurities.

In this paper, we present a novel concept for the fabrication of TSVs based on wire bonding technology. Our approach is targeting applications that require very high aspect ratio TSVs, such as interposers, MEMS, capping of MEMS devices and RF-MEMS.

VIA CONCEPT

We propose a via metal filling process based on the integration of bulk wire material using standard wire bonding technology. Recently, Fischer et al. have shown two TSV fabrication approaches based on the integration of bulk wire materials. The via cores are integrated by magnetic assembly [14] or by using a modified wire bonder [15]. In the latter case, the via metal core is directly wire bonded to a thin metal membrane at the

bottom of the via hole. Due to the fact that wire bonding is performed inside the via hole, requires this concept comparatively large via diameters and hence is limited to low aspect ratios.

In this work, we propose a standard wire bonding process for the fabrication of TSVs with very high aspect ratios. Wire bonding is used to place metal wire into the via hole and to temporarily attach the wire on the top side of the substrate.

Figure 1 illustrates the functional components of a TSV according to the proposed fabrication scheme. Figure 1a depicts the vertical via hole. Figure 1b shows the via core that is placed with the help of a wire bonder in the via hole and the temporary attachment to a bond pad on top of the substrate. The final TSV is illustrated in Figure 1c, which is composed of the TSV core, surrounded by the insulator in the via hole of the substrate. The insulator is Benzocyclobutene (BCB), which is a ductile polymer, has good dielectric properties and can act as a stress relief for thermo-mechanical stresses between the via metal core and the monocrystalline silicon substrate [16].

FABRICATION

TSV prototypes have been fabricated on 100 mm double-sided polished silicon substrates with two different thicknesses. A 300 μm thick silicon wafer was processed for electrical characterization of the TSVs and a 625 μm thick substrate was processed to investigate the feasibility for very high aspect ratio TSVs (20:1). The fabrication is divided into three processing sequences; The via hole formation, the via core integration then the final via insulation and TSV electrical contacting sequence. These steps are described in detail in the following sub-sections.

Via Hole Formation

The via hole formation is depicted in Figure 2. The wafer is wet oxidized in a furnace at 1150 $^{\circ}\text{C}$ to create a 2 μm thick silicon-dioxide layer, which acts as a hard mask. TSV holes with a diameter of 30 μm are patterned using Megaposit SPR 700 1.2 photoresist. The etching of the top silicon-dioxide layer is performed using a standard dry etching process (Fig. 2a). Then, the via holes are anisotropically dry etched using the Bosch process (Fig. 2b). The remaining silicon-dioxide on the backside of the wafer and the top hard mask are removed in buffered hydrofluoric acid (BHF). A second thermal wet oxidation is performed to remove remaining polymer residues at the sidewalls of the via holes and to provide an electrical insulation of the via sidewalls from the metal core by a 300 nm thick silicon-dioxide layer. To be able to attach the via core by performing a stitch bond on the substrate, a 200 nm thick gold layer is sputtered on top of a titanium-tungsten adhesion layer (Fig. 2c).

Via Core Integration

The via core integration is performed at room temperature, using a semi-automatic gold ball wire bonder, model 5410 from F&K Delvotec Bondtechnik GmbH, Germany. In this work we used a gold wire with a diameter of 20 μm . The integration approach of the TSV

metal core is adapted to a standard ball/stitch wire bonding cycle, which is composed of four steps:

1. Formation of the Free Air Ball (FAB)
2. Ball bond at the first bond position
3. Looping towards the second bond position
4. Stitch bond at the second bond position

The integration of the via core adapts these steps for the metal core placement and temporary attachment of the via core. The via metal core integration is illustrated in Figure 2d-f. During the wire bonding, the substrate is placed on a custom-made chuck that contains recesses. The cavity underneath the substrate is required to feed the tail of the bond wire all the way through the via hole. The free air ball formation is skipped and the ball bond sequence is modified to place the metal core into the via hole. The bond capillary centers the bond wire over the via hole and feeds the wire in the via hole until the bond capillary touches the substrate (Fig 2d). The excessive top part of the bond wire tail is utilized for the looping. Therefore, the bond capillary moves upwards until the required looping length is accessible outside of the via hole (Fig. 2e, step 1). Then, the bond capillary moves laterally to the bond pad (Fig. 2e, step 2). The stitch bond process does not deform any parts of the wire in the via hole. The bond capillary performs a standard stitch bond to attach the via metal core temporarily. In a final step the bond capillary moves upwards. The tail length for the next via core is defined by closing the wire clamp during the vertical movement of the bond capillary and breaking the bond wire at the stitch bond interface (Fig. 2f).

Via Insulator And TSV Contacts

After the integration of the metal via cores, a hollow cavity remains between the via sidewalls and the via cores with a thickness of 5 μm . Benzocyclobutene (BCB), type Cyclotene 3022-46 was used to embed the wire-bonded cores. The substrate was heated to 60 $^{\circ}\text{C}$ to reduce the viscosity of the BCB in order to improve the filling of the via cavities. The BCB is applied on the substrate with a syringe. Then, the substrate is treated in vacuum to minimize void formation. The final hard-cure of the BCB is carried out according to the manufacturer instructions at a maximum temperature of 250 $^{\circ}\text{C}$ (Fig. 2g) [17]. Excess metal from the temporary attachment of the bond wire as well as excess BCB on the surface of the substrate is subsequently removed by a grinding and polishing process. The hardness of the silicon-dioxide on both sides of the substrate acts as a stop layer during grinding. A cleaning step of the front- and backside of the substrate removes remaining BCB residues on the via metal core terminals (Fig. 2h). In a final step, the front- and backside metal contacts are patterned. A 200 nm gold sputtering and lift-off process is utilized to define the metal contact pads (Fig. 2i).

CHARACTERIZATION

The fabricated high aspect ratio TSVs are characterized in terms of metal core placement and BCB

Figure 2: Fabrication scheme for the high aspect ratio TSVs, divided into three process sequences: First, via hole formation, which starts with oxidation, patterning and dry etching of the via hole. A second oxidation follows before metal is deposited on the wafer surface (a – c). Second, integration of the TSV metal cores utilizing a wire bonder by adapting a standard wire bonding cycle (d – f). Third, TSV insulator processing, front and backside grinding of the wafer and contact metallization of the TSV cores (g – i).

embedding. Complete and void-free filling of BCB along the via core can be considered as a reliability criterion of crucial importance. Therefore, cross-sections are prepared to inspect visually the BCB filling along the via core. The inspections of the TSVs have shown that the via core is completely embedded in BCB and no voids have been observed in the BCB. This confirms the feasibility of utilizing BCB or other polymers with similar properties to embed integrated bulk via metal cores, such as the bond wires. To demonstrate the suitability of the integration approach for very high aspect ratio TSVs of 20:1, a bond wire with a diameter of 20 μm was integrated in the via holes of a 625 μm thick silicon substrate. Figure 3 shows a SEM image of the cross-section after the hard cure of the BCB. On the left side of the TSV the temporary stitch bond is visible. It can be seen in Figure 3 that the via core is not centered at the upper part of the TSV hole and touches the sidewall of the via hole. The semi-automatic wire bonder, which is utilized in this proof-of-concept experiment, has limited placement accuracy. A non-centered via core can affect electrical characteristics, such

as capacitive substrate coupling and therefore needs to be optimized. State-of-the-art wire bonding tools offer better placement accuracy and can therefore potentially provide an optimized integration process.

An array of 10 times 10 TSVs with an aspect ratio of 10:1 was characterized in terms of electrical resistance. Kelvin structures on the top side of the wafer were used to contact the TSVs, while the backside of the wafer was entirely metallized. Four-point measurements were performed and the resistance of two TSVs and the backside metallization was measured. The measured resistance of the TSVs varies substantially. Several TSV measurements have shown contact resistances between 0.25 Ω and 1 Ω . However, a few TSVs are found with resistances of less than 0.075 Ω . This is still higher than the theoretical value of resistance of around 0.023 Ω for a gold via of this length, but it nevertheless shows the feasibility of the proposed TSV approach. We believe that the high resistances of the TSV prototypes are caused by polymer residues on the via core terminals, due to insufficient substrate cleaning.

Figure 3: Cross-section of an integrated TSV metal core with an aspect ratio of 20:1, embedded in BCB. The detail shows the stitch bond attachment and the undesired contact of the metal core with the via sidewall, which is the result of a limited placement accuracy of the via core using a semi-automated wire bonder.

CONCLUSION

We have shown a generic approach for the fabrication of TSVs with very high aspect ratios up to 20:1. A wire bonder was utilized to integrate the TSV metal core in the via hole and temporarily attach it to the substrate. This approach is characterized by its simplicity and adaptation of a standard wire bond cycle for the via core integration and is therefore suitable for using state-of-the-art wire bonding tools. The fabricated TSV prototypes are characterized in terms of void-free polymer embedding, core placement and electrical resistance. The wire bonded high aspect ratio TSVs are suitable for application areas such as, interposers, MEMS, RF-MEMS and MEMS capping application. The presented concept can be regarded as a suitable approach for metal filling of TSVs for applications with low to medium via densities.

ACKNOWLEDGEMENTS

This work has been funded from the European Research Council (ERC) under grant agreements 277879 M&M's.

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