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A Study of Low-frequency Noise on High-k/Metal Gate Stacks with In situ SiO_x Interfacial Layer

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Abstract—Low-frequency noise of HfO_2/TiN nMOSFETs with different SiO_x interfacial layer (IL) thicknesses is presented. It is observed that chemically formed thin ILs (0.4 nm, 0.45 nm and 0.5 nm) show a noise level close to a reference thermal IL (1 nm). This is shown to relate to the dominant contribution of the high-k HfO_2 traps in comparison to the IL traps. The average extracted values for effective trap densities in these wafers are $N_t = 7 \times 10^{18}$, 1×10^{19} , 2×10^{19} and 4.8×10^{19} for thermal oxide, 0.5 nm, 0.45 nm and 0.4 nm chemical oxide wafers respectively.

Keywords—Low-frequency noise; high-k dielectric; interfacial layer; chemical oxidized; MOSFET

I. INTRODUCTION

Increased low-frequency noise (LFN) is one of the substantial issues in aggressively scaled MOSFETs with high-k gate dielectric. The study of this type of noise is one of the key tools for analysis of defects in the gate materials [1]-[3]. The $1/f$ noise in high-k devices is mostly caused by the traps located in the high-k layer or at the high-k dielectric and channel interface [4]-[7]. To get a better oxide interface quality, an interfacial layer (IL) is grown between the high-k and the underlying semiconductor [7] [8]. The thickness of this IL influences the level of noise significantly [9][10]. The reported LFN in novel gate stacks follows the unified correlated mobility and number fluctuations [1]. This model is based on the theory that the traps not only cause number fluctuations by filling and emptying of charge carriers, but also contribute to mobility fluctuations through scattering effects of the fluctuating oxide charge. The unified model has been modified since it was introduced by K. Hung et al to fit the high-k technology by B. Min et al [10]. In multilayer gate stacks, the effect of different gate layers needs to be also considered in the noise model. The final model shows that in devices with thin IL the noise level increases as traps contribute from both the IL and the high-k layer. At the point when the IL is very thin, the interface layer traps become negligible comparing to the high-k layer traps. A useful method to evaluate noise in multilayer gate stacks is to study the gate noise [9]. In Si transistors with high-k gate stacks, SiON interlayers are most widely used. In case of SiO_x , the IL can be deposited with different techniques. The ex situ method is growing an oxide layer thermally and etching back to reach to the required thickness. The IL can be also formed in situ, in the same ALD that is used for depositing

high-k dielectrics. In this method, oxidizing agents, based on ozone with a few tweaks, are exposed to the Si substrate at low temperature which forms uniform IL layers [11]. Since the IL and high-k deposition is carried out in the same equipment, the wafer will be less contaminated comparing to the ex situ methods as it will not be exposed to air in between the depositions [12]. The purpose of the paper is to investigate the LFN in HfO_2 MOSFETs with different SiO_x interfacial layer thicknesses which were fabricated with different techniques. Section II contains the device fabrication steps. In section III, experimental details are explained. The results are reported and discussed in section IV. Finally, the work is concluded in section V.

II. DEVICE FABRICATION

Devices were fabricated on bulk Si (100 mm), p-type (B doped) wafers. The fabrication was performed in a gate last process with different gate stack compositions. Dummy gates were used as a mask to form source and drain regions with N-well and P-well doping levels of 10^{17} cm^{-3} . To prevent any native oxide formation, the samples were cleaned in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$, followed by HF dip and rinse/dry. In the reference wafer the IL was grown with an ex situ method, starting with conventional dry oxidation at 750°C followed by timed etch in a diluted HF chemistry. In the three other wafers ILs were fabricated in situ, through chemical processes in an ALD reactor.

Fig. 1. Gate stack schematic of the investigated devices. The SiO_x IL varies from 0.4 nm to 1 nm. A 3.5 nm layer HfO_2 is deposited on top of all wafers.

TABLE I. Gate stack combination

Wafer type	Fabrication method	IL thickness(nm)	EOT(nm)
O ₃	Chemical O ₂ /O ₃ oxidation	0.4	1.1
H ₂ O	Chemical O ₂ /O ₃ and H ₂ O oxidation	0.5	1.2
Pulsed	Chemical O ₂ /O ₃ and H ₂ O oxidation (5sec), Ar purge(5sec)	0.45	1.15
Etchback	Thermal oxidation, etched back in HF.	1	1.7

One in situ wafer received a chemical O₂/O₃ (10% O₃ concentration) oxidation at 1mbar reactor pressure and 350°C reactor temperature. In the other wafer, chemical O₂/O₃ (10% O₃ concentration) and H₂O oxidation was applied at 1mbar reactor pressure and 350°C reactor temperature. Finally, the last wafer was exposed to the same oxidation flows as the previous wafer for 5seconds followed by 5seconds Ar purge, in which the two steps were repeated in the oxidation period. The IL formation steps in these wafers are summarized in Table I. IL thicknesses are derived through Equivalent Oxide Thickness (EOT) values which were calculated through CV measurements and corrected for inversion capacitance per unit area [13]. The gate stack fabrication was continued with 3.5 nm HfO₂ and TiN/TiW deposition. In the next step, the deposition of SiO₂/SiN stack (25/27 nm) as a passivation layer was performed by PECVD followed by TiN/TiW/Al stack (10/100/500 nm) deposition by sputtering. Finally FGA in 10% H₂/N₂ at 400°C was performed for 30 min [12].

III. EXPERIMENTAL DETAILS

Low frequency noise studies were carried out on nMOS transistors with W=10μm L=3 and L=10 μm, in the linear region (V_{DS}=50 mV). The gate voltage V_G varied between 0.6 V to 1.2 V. On-wafer noise measurements were acquired by a spectrum analyzer and a Programmable Biasing Amplifier (PBA) with an external low noise power supply. DC properties of these devices such as gate leakage, transconductance g_m and threshold voltage V_t were extracted with a Keithly 4200-SCS parameter analyzer. DC measurements of these samples show reasonable I_D-V_G characteristics depicted in Fig 2. The on-current of these devices vary between 60 μA and 80 μA. All devices show good subthreshold slope, however the subthreshold slope of the O₃ wafer is influenced by high leakage current. Leakage current measurements exhibit fairly low gate leakage current density (I_G≈10⁻³ A/cm²) at threshold voltage for the ex situ wafer [15], but rather higher leakage in in situ wafers. In the noise measurements V_G was limited so that the drain current was always one magnitude larger than the gate current.

The threshold voltages vary between 0.6V to 0.9V. Most devices showed a positive threshold voltage shift around 10mV at room temperature after the noise measurements. This shift was even observed after an IV sweep with the parameter analyzer. The shift is shown to be due to charging of the traps in HfO₂ [14].

Fig. 2. I_D-V_G on nMOSFETs with W×L=10×3 μm² and V_{DS}=50 mV.

During the noise measurements, as the device was under gate bias for a continuous time, a large degradation in the gate oxide was observed. In some samples it even led to device damage. This was shown as a sudden increase in the noise spectrum. The increased noise was not 1/f type but rather close to 1/f². This problem was mostly observed in the O₃ wafer which has a very thin interlayer. In order to remove any influence of the degraded gate current, IV measurements were performed both before and after LFN measurements. Those devices which were degraded were excluded from the noise studies.

IV. RESULTS AND DISCUSSION

Fig. 3 shows the noise spectrum of an nMOSFET with a pulsed formed interlayer with dimensions L=3 μm and W=10 μm. This noise was measured for a fixed drain voltage V_d=50mV and gate voltage above the devices threshold voltage (V_t=0.66) increasing from 0.6V to 1.2V over a frequency range between 1-10⁴ Hz. The noise spectra of all the devices are of 1/f type with γ close to 1 for the frequency range (1-10⁴ Hz). In Fig.4 the normalized drain current noise over drain current is plotted with circle markers for all four wafers. On the second y-axis, (g_m/I_d)² is depicted with square markers.

Fig. 3. LFN versus frequency for 7 different gate voltage values for n-type pulsed wafer with W×L=10×3 μm² and V_{DS}=50 mV.

Fig. 4. Normalized drain current spectral density and $(g_m/I_d)^2$ over drain current for n-type (a) pulsed, (b) H_2O , (c) O_3 and (d) etchback wafers with $W \times L = 10 \times 3 \mu m^2$, $V_{DS} = 50$ mV and $f = 10$ Hz.

It is shown that the normalized noise follows $(g_m/I_d)^2$ closely which verifies the correlated mobility and number fluctuation noise mechanism in these devices. The devices on two different dies with different gate lengths are compared.

The normalized drain noise data at $f = 10$ Hz over drain current is shown in Fig. 5 for gate lengths ($L = 3 \mu m$ and $L = 10 \mu m$) on the etchback wafer. The plots of two different dies overlap well which confirms the reproducibility of the data. Higher normalized drain noise is observed in the shorter transistors as LFN noise increases inversely with device area.

Fig. 5. Normalized current spectral density versus drain current for nMOSFETs on etchback wafer with $W \times L = 3 \times 10 \mu m^2$ and $W \times L = 10 \times 10 \mu m^2$ at $V_d = 50$ mV and $f = 10$ Hz. The dashed lines are $1/I_d^2$.

In Fig. 6, the input referred voltage spectral density $S_{vg} = S_{id}/g_m^2$ at $f = 10$ Hz as a function of gate voltage overdrive ($V_{GS} - V_T$) is depicted. The results determine fairly close low-frequency noise level for all four wafers, although some sensitivity to IL thickness is observed [10].

The effective density of traps has been extracted from the input referred voltage spectral density at $f = 10$ Hz using this equation [2]

$$N_t = \frac{S_{id}(V_{GS} - V_t)^2 \alpha_t C_{EOT}^2 W L f}{q^2 k T I_D^2} \quad (1)$$

Fig. 6. Input referred voltage spectral density over gate voltage overdrive for O_3 , pulsed, H_2O and etchback samples at $V_d = 50$ mV and $f = 10$ Hz.

Fig. 7. Effective trap density extracted by drain noise measurements over gate voltage overdrive measured at $f = 10$ Hz.

Where α_t is the tunneling parameter, C_{EOT} the gate-dielectric capacitance per unit area, k the Boltzmann's constant and T the absolute temperature. Since g_m depends on the gate voltage overdrive, $g_m = I_D / (V_{GS} - V_t)$ is assumed in equation (1). We have assumed $\alpha_t = 0.5 \times 10^8 \text{ cm}^{-1}$ for HfO_2 [16]. The extracted N_t from extrapolation of the experimental data is shown in Fig. 7. The results show rather good quality HfO_2 comparing to reported values [10][17][18]. N_t values are inversely proportional to the IL thickness and increase from etchback sample to O_3 sample as the interlayer becomes thinner. The extracted N_t values are $N_t = 7 \times 10^{18}$, 1×10^{19} , 2×10^{19} and 4.8×10^{19} for etchback, H_2O , pulsed and O_3 wafers respectively. The results suggest that in situ formed ILs show enhanced number of trap densities comparing to etchback sample which is expected [19]. Moreover, these in situ wafers show lower N_t in comparison with reported ex situ chemical oxide wafers [6] [14]. The variation observed in N_t can be partly due to traps in the IL and different quality HfO_2 samples.

V. CONCLUSION

We have experimentally investigated the drain noise of nMOSFETs with high-k/metal gate stacks with differently fabricated interface layers (IL). The values of effective trap densities have been extracted through modeling of drain current low-frequency noise. It has been observed that wafers with chemical oxide ILs fabricated in situ in the ALD, with 0.4 nm, 0.45 nm and 0.5 nm IL thicknesses show higher N_t values than ex situ thermal oxide IL wafer with a 1 nm thick IL. However, the derived N_t values of these in situ chemical oxide wafers are lower than chemical oxide ILs fabricated with other techniques.

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