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An Efficient Boost Converter Control for Thermoelectric Energy Harvesting

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Abstract—This paper presents an ultra-low power control circuit for a DC-DC boost converter targeting implantable thermoelectric energy harvesting applications. Efficiency of the input converter is enhanced by utilizing zero-current switching technique. Adaptive delay between ON states of switches assures zero-voltage switching of synchronous rectifier and reduces switching losses. The control circuit employing both techniques consumes an average power of 620nW. This allows the converter to operate from harvested power below 5μW. For voltage conversion ratios above 20, the proposed circuits and techniques demonstrate efficiency improvement compared to the state-of-the-art solutions.

I. INTRODUCTION

Implantable biosensors are receiving constantly growing attention nowadays. Recent technology development and device miniaturization have pushed the biosensor size and power consumption to extremely low values. However, most implantable biosensors are still powered by batteries, which have dominant impact on their size and lifetime. Energy harvesting is a very attractive solution to avoid constant battery replacement. From various emerging energy harvesting techniques, only few of them can be used at a micro-scale level [1]. Moreover, human body is a specific environment and a potential energy harvester should be able to extract energy while being completely surrounded by human tissue. Relatively high power density, small size, unlimited lifetime, biocompatibility and ubiquitous temperature difference inside the human body makes the thermal energy harvesting the most promising solution for many applications of autonomous implantable biosensors.

Thermoelectric energy harvester is far from an ideal voltage source. Its output voltage and power vary depending on environmental conditions. Moreover, the human thermoregulatory system controls the core body temperature, so that temperature gradients inside the body are very small. The highest temperature gradient is available just under the surface of the skin in the fat layer, where temperature difference can reach up to 5K. However, the actual difference between the plates of the harvester is expected to be much lower, from 0.5K to 2K [2]. Therefore, the resulting output voltage may be as low as 40mV and the output power only

4μW even when a state-of-the-art thermoelectric device is used [3]. Such an energy source requires a customized power management unit (PMU) in order to supply the biosensor system. The input dc-dc boost converter, which is the main block of the PMU, has to be efficient at ultra-low input power levels. In this operating region, the efficiency of the converter is dominated by the power consumption of control circuitry. Thus, it is crucial to minimize the power consumption of the boost converter's control.

This paper is organized as follows. Section II discusses the necessity of energy storage device, the dc-dc boost converter topology and sources of losses in the converter. Section III introduces the proposed efficiency enhancement techniques, describes their circuit implementations and presents the simulation results. Finally, conclusions are made in Section IV.

II. SYSTEM CONSIDERATIONS

The expected average power obtained from energy harvesting is much lower than the power consumption of biosensor node during its active state. Accordingly, the power management unit should be able to accumulate energy during the sleep state of the biosensor in order to power the biosensor system during its active state. Therefore, an energy storage device is necessary. With appropriate energy storage, the duty cycle of the biosensor system can be reduced in order to meet the power requirements [4]. Supercapacitors are well suited for energy storage in such systems, because of their capability to provide high burst of energy in a very short time frame. Voltage on storage capacitor is usually unregulated, because load currents are very high during the active state of the biosensor. The varying output voltage on storage capacitor (between 1 and 2.5V in this particular case) introduces new challenges to power management system design. Since the input and output voltages are both varying, it is crucial to maintain high efficiency of the converter for very wide range of voltage conversion ratios.

A. DC-DC Boost Converter

The performance requirements for an input step-up converter are very demanding. The boost converter with an

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Figure 1. The simple dc-dc boost converter.

external inductor is the only topology that can maintain high efficiency at a very high voltage conversion ratio and a wide range of ratios at the same time [5]. The boost converter which is used to validate the proposed control circuit is shown in Fig. 1. Similar topology will be utilized in the complete PMU, due to low number of external components and therefore small size.

B. Loss Mechanisms and Efficient Control

Efficiency of the converter depends on its losses and on the power consumption of control circuits. Most of the losses can be classified as conduction or as switching losses. Conduction losses include losses on inductor resistance, switch resistances and equivalent series resistance of capacitors. These types of losses are inevitable and they trade-off with size and cost of the converter. Fortunately, conduction losses scale down with the input power. At low input power, switching losses prevail over conduction losses. They include switch driver losses and switch synchronization losses. Switch driver losses can be minimized by decreasing the frequency at the cost of increased conduction losses. The focus of this work is on minimizing switch synchronization losses which become significant as the input power reaches very low levels. This type of losses can be successfully tackled by utilizing specific techniques in switching control as it will be seen in the next section.

III. CONTROL CIRCUITS IMPLEMENTATION

A. Maximum Power Extraction

Thermoelectric energy harvester can be accurately modeled as a voltage source V_T in series with a resistor R_T , as it can be seen in Fig. 1. In order to extract maximum possible power from such harvester, the resistance seen from the input of the dc-dc converter has to be equal with the internal resistance of the harvester. Depending on the used device, this internal resistance (R_T) varies from 5Ω up to 400Ω in recent state-of-the-art devices [3]. In this work, an intermediate value of 100Ω is adopted. On the other hand, the input resistance of the dc-dc boost converter with high conversion ratio is approximately given by:

$$R_{in} \approx \frac{2Lf_s}{D^2}, \quad (1)$$

where L is inductor value, f_s switching frequency and D is duty ratio of the converter [6]. Considering an inductor of $10\mu\text{H}$ and switching frequency of 50kHz in (1), the resulting duty ratio is 0.1. Although, larger inductor may improve the efficiency, it also increases the system size. On the other hand, higher frequency increases the switching losses and

Figure 2. The control signal generator for the nFET switch.

Figure 3. Waveforms of the ZCS controlled boost converter when the pFET switch is turned-off early (left) and late (right).

control circuit power consumption, so these reasonable values are adopted for the proof of concept.

Note that the input matching fully defines the operating frequency, duty ratio and therefore ON time (τ_N) of the nFET switch control. The control signal (q_N) generator for this switch with 0.1 duty ratio is shown in Fig. 2. The ultra-low power current starved ring oscillator generates two 50% duty cycle clock signals delayed by $1/(10f_s)$ with respect to each other. Those two signals are then combined to generate 0.1 duty cycle q_N signal. The ring oscillator consists of 10 inverter stages and one nand stage for resetting/disabling purposes. Inverters are biased with 30nA current. 3-bit signal $b<2:0>$ controls the resistance of the current reference, so the frequency can be adjusted to correct for process variation.

B. Zero-Current Switching (ZCS)

Since τ_N is fixed by the input matching, and the input and output voltages are variable, pFET ON time (τ_P) has to be adjusted in order to obtain efficient conversion. For the dc-dc boost converter operating in discontinuous conduction mode (DCM), the peak inductor current is given by:

$$I_{Lmax} = \frac{V_{in}}{L} \tau_N = \frac{V_{out}-V_{in}}{L} \tau_P \Rightarrow \tau_P = \frac{\tau_N}{\frac{V_{out}}{V_{in}}-1}. \quad (2)$$

When (2) is satisfied, ZCS of the inductor current is achieved, as it is shown in Fig. 3. If pFET is turned-off early, the

Figure 4. The control signal generator for the pFET switch.

Figure 5. Waveforms of the ZVS controlled boost converter when the pFET switch is turned-on perfectly (left), early (middle) and late (right).

inductor current will continue to flow through the pFET body diode, which results in unwanted losses since the diode resistance is higher than the ON resistance of pFET transistor. On the other hand, if it is turned-off late, the inductor current will reverse and start to discharge the output capacitance. In [7], a simple method is proposed to achieve ZCS condition. The voltage at node X is sampled after turning-off the pFET transistor with a simple D flip-flop (time t_f in Fig. 3). If the sensed signal is high, which corresponds to diode conduction, then the counter value is increased by one and consequently τ_P is increased. Contrary, if the sensed signal is zero, the counter value and τ_P are decreased. Finally, the counter controls the width of τ_P impulse. Although this method is very effective, the nominal value of τ_P is never reached. The transistor will always switch around the nominal point, slightly early or slightly late.

In this paper an improved method is proposed. The voltage at node X is sensed two times, first time immediately after the transistor is turned-off (t_1) and the second time after a fixed delay (t_2). The obtained 2-bit digital signal distinguishes three different states (value 01 is not possible). When this signal is 11, the counter value is increased, 00 decreased and for 10 the counter is stopped. Note that when the counter is stopped, the transistor actually switches slightly early. This is because losses due to conduction of body diode are much lower than losses caused by reverse inductor current. Besides switching losses, the dynamic power consumption of digital circuits is also lowered. The implementation of the proposed method is presented in Fig. 4. The signal q_P is generated using the fixed signal q_N and delay controlled by the counter value.

Figure 6. The adaptive dead time generator.

C. Zero-Voltage Switching (ZVS)

For high efficiency of the converter it is necessary to introduce a delay, or so-called dead time between ON states of the switches. Otherwise, it may happen during switching that both switches are conducting at the same time. This creates a low resistance path from the output capacitor to the ground and high discharge current. Usually, a fixed dead time is utilized to ensure non-overlapping control of switches. However, even when a dead time is introduced, switching losses exist and depend on it, which can be explained as follows. When the nFET switch turns-off, the inductor starts acting as a current source and charges the parasitic capacitance at node X with the constant current I_{Lmax} . In the ideal case, the parasitic capacitance is charged to exactly V_{out} before pFET turns-on. In such case, lossless ZVS of the pFET switch is achieved, as it can be seen in Fig. 5. If the switch is turned-on early, the parasitic capacitance will be charged from the output, through a low ON resistance of the switch, resulting in significant losses. Also, if the switch is turned-on late, the voltage on the parasitic capacitance will exceed the output voltage, which will further result in body diode conduction. To obtain ZVS, the dead time has to be adaptive since it depends on both the input and the output voltage of the converter. The voltage V_X during capacitor charging is given by

Figure 7. The waveform of the voltage V_X .

$$V_X(t) = V_X(0) + \frac{1}{C_X} \int_0^t i(\tau) d\tau, \quad (3)$$

where C_X is the parasitic capacitance at node X, $V_X(0)=0$ and $i(t)=I_{Lmax}$. To obtain ZVS, the following condition should be met:

$$V_X = \frac{I_{Lmax}}{C_X} t_{dead} = V_{out}, \quad (4)$$

where t_{dead} is the desired dead time. Combining (4) with (2) for $V_{out} > V_{in}$, the dead time is:

$$t_{dead} \approx \frac{C_X L}{\tau_P}, \quad (5)$$

which shows that the dead time is inversely proportional to τ_P . In this particular case τ_P , given by (2), is controlled between 20ns and 200ns to meet all different combinations of variable input and output voltages. The value of parasitic capacitance C_X can be easily estimated, and in this case it is approximately 2pF. Consequently, the dead time should be controlled between 1ns and 100ps. Since the counter value defines τ_P , it can also be used to generate the adaptive dead time. According to (5) the dead time changes very slowly for larger values of τ_P and counter (several ps). However, it starts to change significantly (hundreds of ps), as τ_P reaches its minimal values. Therefore, for the counter values from 0 to 3, the dead time is changed accordingly, but for the remaining values it is fixed to the approximate time (200ps in this case).

The circuit implementation of the proposed technique is presented in Fig. 6. The delay is controlled by switch ON resistances and it has the largest value when all the switches are turned-off. Switches are sized such that each one of them is reducing the delay according to (5), when it is ON. The input inverter is sized to have negligible ON resistance compared to switches.

D. Simulation Results

The proposed control is applied to the dc-dc boost converter presented in Fig. 2 in order to validate its performance. The obtained waveform of voltage V_X , presented in Fig. 7, shows that ZCS and ZVS are achieved.

Figure 8. Efficiency comparison between the state-of-the-art presented in [7] and this work.

The efficiency of the converter controlled by the proposed control circuit is compared to the state-of-the-art converter [7], as it is shown in Fig. 8. The converter controlled by the proposed circuit maintains high efficiency for much higher voltage conversion ratios due to very low power consumption of the corresponding circuitry. Efficiency enhancement by using control with improved ZCS and ZVS techniques instead of regular ZCS and fixed dead time is also shown in Fig. 8. At high voltage conversion ratios, the combined techniques provide up to 10% efficiency improvement.

IV. CONCLUSION

An ultra-low power control circuit for thermoelectric energy harvesting within the human body is presented. Complete control circuitry consumes only 620nW. This allows the converter to maintain its high efficiency at very low input power levels. Moreover, the proposed control utilizes ZCS and ZVS techniques simultaneously to further enhance the efficiency of the converter by minimizing switching losses. Consequently, it allows the converter to operate at extremely low input power levels below 5μW, which corresponds to temperature difference below 0.5K. Finally, the converter shows higher efficiency compared to the state-of-the-art at voltage conversion ratios above 20.

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