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Lateral PNP transistor and Complementary SiC Bipolar Technology

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Abstract—Lateral PNP transistors and a complementary bipolar technology have been demonstrated for analog integrated circuit. Besides vertical NPNs, this technology provides lateral PNPs at the cost of one additional lithographic and dry etching step. Both devices share the same epitaxial layers and feature topside contacts to all terminals. The influence on PNP current gain of contact topology (circular vs. rectangular), effective base width, base/emitter doping ratio and temperature was studied in detail. In the range -40 to 300 °C, the current gain of PNP transistor shows a maximum about 35 around 0 °C and it is about 8 at 300 °C, while in the same range the gain of NPN transistors exhibits a negative temperature coefficient.

Index Terms—Bipolar junction transistor (BJT), Silicon Carbide (SiC), complementary bipolar, lateral PNP transistor, current gain temperature dependence, high and low temperature.

I. INTRODUCTION

Silicon carbide (SiC) devices are able to operate at extreme temperature [1], and SiC bipolar transistors (BJTs) are suitable for wide-temperature range integrated circuits (ICs). Compared to CMOS technology, the lack of a gate oxide in bipolar and JFET technologies offers a great advantage in terms of long term operation at elevated temperature [1]. Compared to JFETs, BJT transistors could provide better IC performance. Different 4H-SiC bipolar ICs have been reported based on transistor-transistor logic (TTL) [2] and emitter-coupled logic (ECL) [3], with operating temperature as high as 355 and 500 °C respectively. However, in both cases only NPN transistors were used. In addition, our previous attempts at 4H-SiC PNP transistors showed less than unity gain [4]. Although bipolar logic gates can be designed without PNPs, the availability of both NPN and PNP transistors in the same IC technology would simplify the design of analog ICs [5].

This paper reports on the integration of lateral PNP transistors in a 4H-SiC bipolar IC technology for low-voltage application (supply voltage of 15V). Transistors show current gain (β_{PNP}) of ~ 35 . The effects of contact topology and epitaxial layer design on current gain are evaluated, as well as the gain temperature dependence in the range -40 to 300 °C.

II. DEVICE STRUCTURE AND FABRICATION

Only one additional process step was necessary to integrate

lateral PNP transistors in an ion-implantation free technology suitable for low-voltage bipolar ICs. NPN and PNP cross-sectional views, together with nominal doping concentrations and thicknesses of the epitaxial layers, are shown in Fig. 1. The emitter and collector region of the PNP were formed in the p-doped base layer of the NPN transistor, while the low doped collector layer of the NPN acts as base of the PNP. A total of six epitaxial layers, grown on a 100 mm diameter 4H-SiC n-type substrate, were used in order to ensure top side ohmic contact to the NPN collector region, and to isolate different devices by using a p-type layer between the devices and the substrate.

NPN and PNP mesa structures were defined by means of four plasma etching steps performed in a mixture of Ar and SF_6 with SiO_2 hard mask. After defining the emitter mesa of the NPN, an additional shallow etching step (compared to the NPN process) was performed in order to isolate emitter and collector regions of the PNP, followed by definition of base and collector mesa of the NPN, and simultaneously of collector and base mesa of the PNP respectively. Details about surface passivation, ohmic contact formation and metallization can be found in [3] and [6]. Note that two metal layers were used. One acts as over-layer metallization for device contacts, and the other one as top metal for interconnects. In this way, the first layer can cover the entire top contact area of each device terminal without limiting the final interconnects.

The lateral PNP has a circular contact topology with the emitter located at the center surrounded by the collector region and the base contact, which is in the outer area (see simple circular PNP in Fig. 2). For this topology, two different distances (2 and 4 μm) between emitter and collector mesas (W_{CE} in Fig. 1) were tested, as well as a large area PNP (~ 7 times larger than the simple circular PNP) with two additional emitter and collector rings and $W_{\text{CE}} = 4$ μm (referred to as large circular PNP). In addition, a PNP with rectangular structure and interdigitated emitter and collector fingers with $W_{\text{CE}} = 4$ μm was also tested. Optical images of the fabricated PNPs are shown in Fig. 2.

III. RESULTS AND DISCUSSION

Fig. 3 (a) and (b) show Gummel plot and current gain plot measured at 27 °C on a simple circular PNP with $W_{\text{CE}} = 2$ μm under different base collector voltage (V_{BC}) ranging from 0 to

15V. Note that, independently of V_{BC} , the Gummel plots in Fig. 3 (a) show base current reversal at low V_{EB} . Although this phenomenon, already observed for Si BJTs [7], can lead to extremely high current gain (see Fig. 3 (b)), the peak gains reported in this paper were calculated for bias above the base reversal. At higher reverse bias of the base collector junction significant enhancement of the peak gain was observed: β_{PNP} increases from ~ 35 at $V_{BC} = 0$ V up to 220 at $V_{BC} = 15$ V. This strong dependence can be related to modulation of the base-collector space charge region (SCR), which extending in the base of the PNP and being enlarged by increasing V_{BC} reduces the effective base width of the lateral PNP. The same effect is evident in the device output characteristic shown in Fig. 4 (a), from which an early voltage (V_A) of about 15 V can be extracted. This results in a gain early voltage product of about 550 V, which is similar to the value achieved by circular PNP with $W_{CE} = 4$ μm , for which $\beta \sim 12$ and $V_A \sim 42$ V.

PNP and NPN transistors exhibit lowest breakdown voltage of about 35 V and 22 V respectively, which are compatible with the low-voltage applications this technology is meant for.

Significant variations in doping concentrations of the p- and n-doped regions of the PNPs (referred to as N_A and $N_{D,PNP}$ respectively) were observed across the wafer. N_A was evaluated from measured base intrinsic sheet resistance of NPN transistors (specific transfer length method structures were used), while $N_{D,PNP}$ was extracted from C-V measurement performed across base collector junction of NPN transistors. Note that for both doping concentrations only an estimation of their variations across the wafer was obtained. Nevertheless, it was possible to evaluate the effects of N_A and $N_{D,PNP}$ on β_{PNP} . Estimated doping concentrations, together with current gains of simple circular PNPs ($W_{CE} = 2$ μm) measured in different dice at $V_{BC} = 0$ V, suggest that in order to achieve $\beta_{PNP} > 1$ the acceptor doping concentration has to be quite high and much higher than the donor doping ($N_A \gg N_{D,PNP}$). The current gain is enhanced by high N_A and low $N_{D,PNP}$, since both of them increase the PNP emitter efficiency. In addition, the lower $N_{D,PNP}$ is compared to N_A the wider the SCR of the base collector junction of the PNP (see Fig. 1), hence the smaller the effective base width of the PNP.

Although a high acceptor doping concentration is clearly desirable for β_{PNP} , this can limit the gain of NPN transistors (β_{NPN}). In terms of NPN, high N_A means high base doping, and NPNs located in the same die as the reported PNP ($N_A \sim 3 \times 10^{18} \text{ cm}^{-3}$) exhibit low $\beta_{NPN} \sim 11$ at 27 °C. In order to overcome this issue, the base epitaxial layer of the NPN could be grown with a graded doping profile decreasing towards the emitter layer. In this way, the overall lower base dose of the NPN, compared to the case of constant doping for a given base thickness, allows higher β_{NPN} while the higher doping in the bottom part of the layer leads to highly doped emitter and collector region of the PNP and less resistive base contact of the NPN as additional advantage. In addition, a lightly doped n-layer could be grown before the base layer of the NPN. This would enhance the PNP base region depletion, and hence increase the gain.

A. Effect of PNP geometry on current gain

For a given doping ratio, the current gain of the PNP can be further improved acting on the device geometry. Measurement results suggest that a circular topology should be preferred with respect to a rectangular one, and W_{CE} and the emitter area should be as small as possible given resolution limits of lithography and etching process, which for the reported technology is close to 2 μm . As shown in Fig. 4 (b), for simple circular PNPs gains of 35 and 11 were measured (at $V_{BC} = 0$ V and $T = 27$ °C) for $W_{CE} = 2$ and 4 μm respectively. The gain reduction for larger W_{CE} can be attributed to the corresponding wider effective base width of the lateral PNP. A significant reduction in gain was observed for large area PNPs with both circular and rectangular topology. The large circular PNP exhibits $\beta_{PNP} \sim 7$, while the rectangular PNP shows $\beta_{PNP} \sim 2$. The better performance provided by the circular topology can be related to reduced distances between device contacts and intrinsic regions, leading to smaller parasitic resistances and better charge collecting efficiency. Concerning the emitter area, it is worth noting that the operation of the PNP is affected by the presence of a parasitic vertical base emitter diode. Since this diode contributes to the base current of the PNP, in order to increase the gain the emitter area should be as small as possible.

B. Current gain temperature dependence

A nonmonotonic temperature dependence was observed for β_{PNP} of simple circular PNPs in the temperature range -40 to 300 °C (see Fig. 5 (a)). Specifically, maximum values of ~ 37 and 12 were achieved around 0 °C for W_{CE} equal to 2 and 4 μm respectively; while at 300 °C they exhibit gains of ~ 8 and 2 (see Gummel plot in Fig. 5 (b) for the PNP with $W_{CE} = 2$ μm). This temperature dependence can be related to opposing phenomena affecting the gain and involving ionization degree of acceptor dopants, lifetime and mobility of minority carriers. For increasing temperature the acceptor ionization degree and the lifetime increase, while the mobility decreases [8], and its reduction is stronger at lower doping concentrations [9]. Therefore, the current gain of the PNPs is enhanced by the higher minority carriers lifetime in the base and higher emitter injection efficiency (due to the increased ionization degree of acceptor in the emitter region), but it is reduced by the lower minority carrier mobility, which in the base decreases faster than in the emitter (the doping concentration in the base of the PNPs ranges between 1×10^{15} and $1 \times 10^{16} \text{ cm}^{-3}$ while in the emitter it is $\sim 3 \times 10^{18} \text{ cm}^{-3}$). In the same temperature range β_{NPN} exhibits instead a negative temperature coefficient (see Fig. 5 (a)). In agreement with previous reported results [3], in the range -40 to 300 °C the reduction in emitter efficiency of the NPN, due to the increasing ionization degree of acceptors in the base, is not yet compensated and overcome by the increase of minority carrier lifetime in the base [8], [9].

IV. CONCLUSION

A 4H-SiC complementary bipolar technology, featuring vertical NPN and lateral PNP transistors with current gain ($V_{BC} = 0$ V) of 35 and 8 at 27 °C and 300 °C respectively, has

been demonstrated. Design principles for achieving high PNP current gain have been proposed in terms of device layout and doping concentrations, taking into account also the doping requirements for high gain NPN transistors. Although further improvement of the PNP performance is required especially in terms of current gain and early voltage, reported technology is a promising candidate for developing a complementary bipolar SiC technology for integrated circuits.

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Figure 1 Cross-sectional view of vertical NPN and lateral PNP transistors fabricated in the same IC technology.

Figure 2 Optical images of the fabricated topologies of lateral PNP: (a) simple circular, (b) large circular and (c) rectangular with interdigitated emitter and collector fingers.

Figure 3 Gummel plot (a) and current gain plot (b) of simple circular PNP ($W_{CE} = 2 \mu\text{m}$) measured at different V_{BC} .

Figure 4 (a) Output characteristic (I_C - V_{EC}) of simple circular PNP ($W_{CE} = 2 \mu\text{m}$). (b) Current gain plot of lateral PNPs with different topologies: simple circular (s.c.) with $W_{CE} = 2$ and $4 \mu\text{m}$, large circular and rectangular.

Figure 5 (a) Gain temperature dependence for simple circular PNPs ($W_{CE} = 2$ and $4 \mu\text{m}$) and NPN transistor (with emitter size $24 \mu\text{m} \times 70 \mu\text{m}$) fabricated in the same die. (b) Gummel plot of simple circular PNP ($W_{CE} = 2 \mu\text{m}$) measured at 300°C .