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Paper V

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Silicon nanowires integrated with CMOS circuits for biosensing application

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ABSTRACT

We describe a silicon nanowire (SiNW) biosensor fabricated in a fully depleted SOI CMOS process. The sensor array consists of N by N pixel matrix (N^2 pixels or test sites) and 8 input–output (I/O) pins. In each pixel a single crystalline SiNW with 75 by 20 nm cross-section area is defined using sidewall transfer lithography in the SOI layer. The key advantage of the design is that each individual SiNWs can be read-out sequentially and used for real-time charge based detection of molecules in liquids or gases.

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1. Introduction

In recent years commercialization of devices like blood glucose monitors, handheld blood analyzer [1] and sleep monitors [2] has created new dimensions in the field of bio sensors. Attempts to make lab-on-chip biosensor, have paved the way for many novel forms of detection mechanisms and structures. Silicon nano-ribbons [3], silicon nanowires (SiNWs) and carbon nanotubes [4] are structures currently in the limelight as they offer very high sensitivity due to their high surface to volume ratio. Particularly, SiNWs have recently attracted attention in the research community due to label-free detection with scope for mass production, multi detection, CMOS compatibility and portability [5]. Contemporary DNA sensors employ optical readout techniques and use labels for hybridization thus making them expensive and bulky [6]. By eliminating optical readout-hybridization techniques and enabling direct electrical detection it is possible to make DNA sensing label free. Efforts to make system on chip (SOC) multi array charge detection architectures have led to complex designs and sensing techniques [7–10]. Even though, the number of test sites was considerably high, these architectures fail to achieve true multi detection. Multidetec-tion can be achieved by having on-chip circuits, that can distinguish and readout individual test sites separately.

SiNW transistors have successfully been used as pH sensors by using a dual gate approach. The shift in the pH was measured

either by sweeping their back gate voltage or liquid potential [11]. Compared to only biasing the back gate to get a response, having a reference electrode to sweep the liquid potential ensures stronger capacitive coupling to the SiNW and a clearer signal for detection [12]. These designs have demonstrated charge detection using single SiNW transistor as sensor. The response times of such a design is slow as the target molecule needs sufficient time to bind to the surface. Further, since the test sites are limited to just one, the binding of the target molecule to the nanowire surface plays crucial and determinental role in the response of the sensor. On the other hand, by having many test sites on a single chip, the response time can be significantly improved. Another key issue to be addressed is monitoring and regulating the sensor-electrolyte interface. To control the bio-chemical reactions on the surface of the electrolyte the liquid potential needs to be monitored [11]. It is therefore important to integrate on-chip reference electrodes within the readout circuitry.

In addition, SiNWs have also been reported to provide high sensitivity and selectivity for detecting molecules in gases and liquids. Recent research hint at single charge detection with threshold voltage shifts on the orders of tens to hundreds of millivolts in electrolyte solutions of low strength [13]. As a result exhaustive research is focused in this domain to make the SiNWs CMOS compatible. Integration with CMOS adds better control to process variations, makes the sensors readout circuitry fully electronic thus increasing the portability, robustness and user friendliness.

To overcome the above drawbacks and with the aim of achieving multidetection, we propose a fully electronic, pixel based SiNW

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Fig. 1. Schematic of SiNW for biosensing. The SiNW is defined in the SOI layer and is contacted by elevated source/drain areas. The SiNW is functionalized with receptors and immersed in a solution containing the electrolyte. The electrostatics of the SiNW is controlled by a back gate in the Si substrate and a fluid gate in the electrolyte. As the charged analytes bind to the receptor, the conductance changes in the SiNW.

biosensor with on-chip fluid gate and back gate. Sidewall transfer lithography (STL) process is chosen to fabricate the nanowires as it is cost and time efficient. In this paper, the design, implementation issues, layout and fabrication steps of the nanowire sensors are addressed in detail.

2. Charge based SiNW sensing

Fig. 1 depicts a schematic of the structure used for biosensing. The SiNW acts as a conducting channel connecting the source and drain contacts. A voltage is applied across the source and the drain (V_{DS}) and the resulting current (I_{DS}) through the SiNW is measured. The conductance of the SiNW is determined by the potential on the fluid gate and the potential on the back gate. The use of both a fluid and a back gate allows an increased freedom to set the desired bias point of the SiNW compared to only using a back gate [14]. The surface of the nanowire can be functionalized with a receptor and provides selectivity to a specific biological species. The conductance in the SiNW depends on the carrier density which is controlled by the fluid and the back gate [15]. As a charged biological species binds to a receptor on the SiNW surface, the carrier density in the SiNW increases or decreases causing the conductance and thus the current I_{DS} to change [16]. The sensitivity of the current change with respect to the amount of charged biomolecules is a function of the SiNW dimensions, doping concentration and the ion concentration of the electrolyte [13].

3. Fabrication

The existing bottom-up nanowire (NW) fabrication techniques are time consuming and difficult for integration. Planar NWs fabricated by top-down processes are appealing for their CMOS com-

Fig. 3. Cross-section schematics of the STL definition of SiNWs using 1-line lithography and cluster tool for PATTERN and PECVD. First a stack of $\text{SiO}_2/\alpha\text{-Si}/\text{SiN}$ is deposited (a) and followed by patterning and etching $\alpha\text{-Si}$ using SiN as a hard mask (b). SiN is deposited (c) and etch backed (d) followed by wet strip of $\alpha\text{-Si}$ (e) to form SiN closed lines on top of the SiO_2 . A lithography step is used to dry etch oxide hard mask (f) and followed by wet etch to remove the SiN STL lines (g). This is followed by another lithography step where one of the SiO_2 line is removed by dry etch (h). Finally the SOI layer is etched to form the SiNW (i).

patibility and potential to fabricate high density integrated sensors. Among them STL is very attractive as it offers high volume

Fig. 2. Process overview of SiNW integrated in fully depleted SOI process.

and throughput of NWs. Fig. 2 shows the process overview of the SiNW integrated in CMOS.

SiNWs were fabricated in the crystalline SOI layer and integrated in a fully depleted SOI CMOS process. The nanowires were defined with STL [17] using 1-line lithography. The key points for reliable and reproducible definition of SiNW using STL are: good control of the thickness of deposited layers, conformal deposition of the sidewall material, anisotropic dry etching and selective etching for removing material. In previous work [17,18], several tools were employed for deposition and dry etching in the STL process. In this work, we have implemented the STL process in a cluster tool equipped with chambers for reactive ion etching (RIE) and plasma enhanced chemical vapor deposition (PECVD). The cluster tool allows for PECVD deposition of SiO₂ and SiN at 400 °C using SiH₄, N₂O for SiO₂ and SiH₄, N₂, NH₃ for SiN deposition as well as RIE of SiO₂ and SiN in one chamber using CHF₃/CF₄/O₂/Ar chemistry and another RIE chamber for Si etching using Cl₂/HBr chemistry. Amorphous Si (α -Si) was deposited using LPCVD furnace at 480 °C. Fig. 3 shows the process flow of the STL process.

First a stack of SiO₂/ α -Si/SiN is deposited (a) and followed by patterning and etching α -Si using SiN as a hard mask (b). SiN is deposited (c) and etch backed (d) followed by wet strip of α -Si (e) to form SiN closed lines on top of the SiO₂. A lithography step is used to dry etch oxide hard mask (f) and followed by wet etch to remove the SiN STL lines (g). This is followed by another lithography step where one of the SiO₂ line is removed by dry etch (h). Finally the SOI layer is etched to form the SiNW (i).

The starting material is SOI wafer with 55 nm Si and 145 nm buried oxide (BOX). First the Si layer is thinned to 20 nm by thermal oxidation and HF etching. Then, a three-layer stack comprising 40 nm thick SiO₂, 150 nm thick α -Si and 40 nm thick SiN was deposited by PECVD (Fig. 3a). The SiN hard mask was patterned and etched using RIE. After removing the resist by oxygen plasma, the α -Si layer was dry etched to form vertical steps. Fig. 4 shows an XSEM of an etched step in the α -Si support material layer. The remaining SiN hard-mask layer was stripped in H₃PO₄ at 145 °C for 2 min. This was followed by conformal SiN spacer deposition in the PECVD chamber over the α -Si support material (Fig. 3c). The thickness of the SiN determines the final width of the SiNWs. Subsequently, the SiN spacer was RIE etched to form spacers on the sidewalls of the α -Si (Fig. 3d). α -Si was selectively etched in 65 °C Tetramethylammonium hydroxide (TMAH) until only the SiN spacers were left behind (Fig. 3e). Fig. 5 shows a top-view SEM picture of formed SiN spacer loops. Next the active area was patterned and the SiO₂ hard mask was dry etched (Fig. 3f). After stripping the

Fig. 4. XSEM of etched α -Si support material displaying vertical sidewalls within the resolution of the XSEM.

resist, the SiN spacers from the STL process were chemically etched using phosphoric acid (H₃PO₄) at 145 °C for 5 min (Fig. 3g). In the next step, one of the SiO₂ hard mask lines was dry etched using lithography and RIE (Fig. 3h) to produce just single oxide spacers. Then SOI layer was finally etched in Cl₂/HBr chemistry to form SiNW (Fig. 3i). Fig. 6 is the top-view SEM of a 75 nm wide SiNW formed in the 20 nm thick SOI layer. After MOSFET gate formation using TiN/polysilicon stack (Fig. 7), a two layer stack consisting of 10 nm PECVD SiO₂ and 20 nm PECVD SiN is deposited uniformly over the SiNW and MOSFET devices. As seen in Fig. 8, this double layer deposition is performed for two reasons: the first is to mask the source and drain areas of the SiNW (Fig. 8c, left), and the second is to create the spacer structure needed for the gates of MOSFET devices used in the biosensing control array (Fig. 8c, right). The source and drain openings are defined using lithography and the

Fig. 5. Top view SEM image of the closed loop SiN spacers.

Fig. 6. Top view SEM image of 75 nm SiNW.

Fig. 7. Top view dark field optical microscope image of SiNW pixel region after gate formation using TiN/poly stack.

Fig. 8. Process flow steps for source drain epitaxy followed by metallization and passivation on SiNW (left) and MOSFET (right).

Fig. 9. Layout of single pixel showing the SiNW, metal layers, PMOSFET and the fluid gate. The orange dotted area in the figure depicts the open area in the SiO₂ dielectric where electrolytes access the SiNW and the fluid gate. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

SiO₂/SiN stack is dry etched (Fig. 8b and c). A 40 nm thick, in situ doped SiGe was selectively deposited on the source and drain regions of the SiNW as well as the MOSFETs (Fig. 8c). The SiO₂ on top of the MOSFET gate and the SiN on top of the SiNW, act as a mask for the selective SiGe growth.

The growth was performed in an ASM Epsilon2000 RPCVD reactor at a stable pressure of 20 torr, in a H₂ ambient environment. The doping level was adjusted to allow for low contact resistivity. The choice of dopant atoms can be done by selecting the appropriate dopant gas source. In this process, the impurities are introduced in the reactor in the form of PH₃ for n + SiGe and B₂H₆ for p + SiGe. Dichlorosilane (DCS) and GeH₄ are the sources of Si and Ge atoms respectively. Following the epitaxy growth, a second two-layer stack consisting of 20 nm PECVD SiO₂ and 60 nm PECVD SiN is deposited uniformly over the wafer (Fig. 8d). This layer will act as a second spacer prior to silicidation.

Fig. 10. A simplified circuit diagram showing each pixels consisting of one SiNW, one fluid gate (not shown) and one PMOSFET to select the SiNW. Vertical and horizontal shift registers is used to sequentially address each pixel and read the current (I_{out}) through the SiNWs.

A 12 nm Ni layer was deposited using a metal evaporation tool, followed by rapid thermal annealing at 450 °C (Fig. 8g). The Ni reacts with the SiGe alloy to form the NiSiGe contact silicide and the unreacted Ni is then selectively etched in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ bath. A 400 nm SiO_2 dielectric stack was deposited with PECVD and the contact via was patterned and etched down to the silicide layer. The interconnects were fabricated with metal sputtering of 460 nm Al on top of 100 nm TiW, followed by forming gas anneal (10% H_2 in N_2) at 400 °C for 30 min. After the metallization and the formal gas anneal (FGA), a layer of PECVD SiO_2 is deposited to protect the Al pads during the remaining steps.

To access the formed SiNWs with the electrolyte, a lithography mask was employed and a combined dry and wet etch of the 400 nm thick SiO_2 was performed. Most of the SiO_2 was removed during the dry etch and the remaining SiO_2 was removed in a diluted buffered HF etch (Fig. 8h). After stripping the photoresist, the remaining SiN was etched in H_3PO_4 . Finally, to access the SiNW and remove the protective SiO_2 layer on the Al pads, a short wet etch was employed (Fig. 8i).

4. System architecture

The biosensor consists of an N by N array of pixels. Fig. 9 shows the layout of a single pixel. Each pixel consists of one SiNW, one fluid gate and one PMOSFET for row selection. The pixel size is 16 by 16 μm^2 . Horizontal and vertical shift register is used to select individual SiNW in the matrix by sequentially selecting row and column. The circuitry consists of 8 I/O pins, V_{dd} and V_{ss} for supply voltage, clock signal, enable signal to the shift registers, fluid gate, back gate and V_{ref} is used to set V_{ds} of the SiNW. The output pin I_{out} is the current through the SiNW. The fluid gate and the back gate set the bias point of each SiNW. The shift registers select the pixels in a sequential manner and the current in each SiNW is read out by sensing the current I_{out} in the time domain. Since typical response times of charge based biosensors is of second order, the sensor will in practice be able to read all individual SiNW in real time (see Fig. 10).

An N by N array needs an N-bit horizontal and vertical shift register to select the individual pixel. For example, a 32 by 32 array

Fig. 12. Layout of a 32 by 32 pixel array with shift registers to address individual SiNWs in each pixel. The total area is 1.35 mm^2 . At the bottom are the I/O pads, about 2.5 mm away from the test sites ensuring good passivation.

needs a 32-bit horizontal and 32-bit vertical shift register as shown in Fig. 12. The shift register is realized using a positive edge triggered D-type flip (DFF) with set and reset. The design of the flip flop is based on transmission gates.

Figs. 11 and 12 show the layout of the 2 by 2, 8 by 8 and 32 by 32 pixel arrays with the shift register circuits respectively. The output of the horizontal shift register is connected to the input of the vertical shift register. Feedback of each shift register is connected back to the input. Yet another key feature of the design is the placement of the I/O pads in the corner of the chip. By doing so, the pixel sensor sites are isolated from the external measurement probes. This ensures clear and accurate signal readout in addition to improving the ease of access to the test sites.

5. Conclusion

A fully integrated CMOS compatible SiNW biosensor is realized using a STL process for SiNW definition. The STL process has been implemented in a cluster tool with chambers for RIE and PECVD using SiO_2 , SiN, and α -Si materials and allow temperature budget of 400 °C. Crystalline SiNW with a 75 by 20 nm cross-section area was fabricated. The sensor consists of 8 I/O pins and the current through individual SiNW is read out in a sequential manner. The sensor design will enable real time monitoring of each individual SiNW.

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Fig. 11. Layout of 2 by 2 and 8 by 8 pixel array showing the I/O pads to the corner of the chip. 2 by 2 pixel needs 2-bit horizontal and 2-bit vertical shift register; similarly the 8 by 8 pixel needs 8-bit horizontal and 8-bit vertical shift register.

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