Horizontal Slot Waveguides for Silicon Photonics Back-End Integration

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Cover image: Right segment, fabricated photonic chip with double slot high-k waveguides and selectively grown germanium mesas. Top left segment, fabricated embedded graphene photodetector. Bottom left segment, cross section of double slot high-k waveguide.

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Abstract

This thesis presents the development of integrated silicon photonic devices. These devices are compatible with the present and near future CMOS technology. High-k horizontal grating couplers and waveguides are proposed. This work consists of simulations and device design, as well as the layout for the fabrication process, device fabrication, process development, characterization instrument development and electro-optical characterizations.

The work demonstrates an alternative solution to costly silicon-on-insulator photonics. The proposed solution uses bulk silicon wafers and thin film deposited waveguides. Back-end deposited horizontal slot grating couplers and waveguides are realized by multi-layers of amorphous silicon and high-k materials.

The achievements of this work include: A theoretical study of fully etched slot grating couplers with Al_2O_3, HfO_2 and AlN, an optical study of the high-k films with spectroscopic ellipsometry, an experimental demonstration of fully etched SiO_2 single slot grating couplers and double slot Al_2O_3 grating couplers, a practical demonstration of horizontal double slot high-k waveguides, partially etched Al_2O_3 single slot grating couplers, a study of a scheme for integration of the double slot Al_2O_3 waveguides with selectively grown germanium PIN photodetectors, realization of test chips for the integrated germanium photodetectors, and study of integration with graphene photodetectors through embedding the graphene into a high-k slot layer.

From an application point of view, these high-k slot waveguides add more functionality to the current silicon photonics. The presented devices can be used for low cost photonics applications. Also alternative optical materials can be used in the context of this photonics platform.

With the robust design, the grating couplers result in improved yield and a more cost effective solution is realized for integration of the waveguides with the germanium and graphene photodetectors.

Keywords: silicon photonics, slot waveguides, grating couplers, CMOS technology, high-k, ALD, germanium photodetectors, graphene photodetectors, photonic integrated circuits.

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Contents

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Maziar A. M. Naiini, Stockholm, December 2014

List of Publications

List of appended papers

I **Fully etched grating couplers for atomic layer deposited horizontal slot waveguides**

M. M. Naiini, B. G. Malm, M. Östling, Proceedings of 12th International Conference on Ultimate Integration on Silicon (ULIS), pp. 1–4, 2011. DOI: 10.1109/ULIS.2011.5758007

II **ALD high-k layer grating couplers for single and double slot on-chip SOI photonics**

M. M. Naiini, C. Henkel, B. G. Malm, M. Östling, Solid State Electronics, v. 74, pp. 58–63, 2012. DOI: 10.1016/j.sse.2012.04.012

III **CMOS compatible ALD high-k double slot grating couplers for on-chip optical interconnects**

M. M. Naiini, C. Henkel, B. G. Malm, M. Östling, Proceeedings of the European Solid-State Device Research Conference (ESSDERC), pp. 93-96 , 2012. DOI: 10.1109/ESSDERC.2012.6343341

IV **Low loss high-k slot waveguides for silicon photonics**

M. M. Naiini, C. Henkel, B. G. Malm, M. Östling, Proceedings of 71st Annual Device Research Conference (DRC), pp. 95-96 , 2013. DOI: 10.1109/DRC.2013.6633810

V **Integrating 3D PIN germanium detectors with high-k ALD fabricated slot waveguides**

M. M. Naiini, H. H. Radamson, B. G. Malm, M. Östling, Proceedings of 15th International Conference on Ultimate Integration on Silicon (ULIS), pp. 45-48 ,2014. DOI: 10.1109/ULIS.2014.6813902

VI **Embedded graphene photodetectors for silicon photonics**

M. M. Naiini S. Vaziri, A. D. Smith, M. C. Lemme, M. Östling. Proceedings of 72nd Annual Device Research Conference (DRC), pp. 43-44 , 2014. DOI: 10.1109/DRC.2014.6872291

List of papers not included in this thesis

1 **Double slot high-k waveguide grating couplers for silicon photonics**

M. M. Naiini, B. G. Malm, M. Östling, Proceedings of 70th Annual Device Research Conference (DRC), pp. 69-70, 2012. DOI: 10.1109/DRC.2012.6256930

2 **ALD high-k layer grating couplers for single and double slot on-chip SOI photonics**

M. M. Naiini, C. Henkel, B. G. Malm, M. Östling, Proceeedings of the European Solid-State Device Research Conference (ESSDERC), pp. 191-194 , 2012. DOI: 10.1109/ESSDERC.2011.6044202

3 **Embedded PIN germanium detectors in ALD slot waveguides**

M. M. Naiini, H. R. Radamson, B. G. Malm, M. Östling, Proceedings of International Semiconductor Device Research Symposium, 2013.

4 **Inkjet Printing of MoS_2**

J. Li, M. M. Naiini, Sam Vaziri, Max C. Lemme, Mikael Östling, Advanced Functional Materials, 2014, DOI: 10.1002/adfm.201400984

Summary of Appeneded Papers

Paper I

In this paper grating coupler structures for single slot high-k atomic layer deposited waveguides are introduced. Finite element simulation for the efficiency of the grating couplers is explained. A fully etched grating coupler structure is chosen to ensure automatic stopping of the etch down to the buried oxide layer. The effect of the slot layer thickness and choice of material on the grating coupler performance was studied. The grating couplers were studied for the slot thickness range of 30 nm to 60 nm. Al_2O_3, AlN and HfO_2 high-k films were studied as the slot material. Simulations shown a coupling efficiency of 24%.

The author performed 100% of the simulations and wrote 90 % of the manuscript. The author suggested this waveguide and grating coupler structure for exploration of high-k thin films in photonics

Paper II

This paper investigates various practical aspects of the single slot horizontal waveguide and grating couplers. The optical properties of Al_2O_3, AlN and HfO_2 are reported. This is done through deposition of the high-k films on bulk silicon substrates and performing ellipsometry characterizations. Since the properties of the thin films differ from the reported values in the literature, the grating couplers in the paper I are studied for the measured optical properties. Fabrication of single SiO_2 slot waveguides is explained and the characterization results are reported. Using chemical vapor deposition the slot waveguide is deposited. The waveguides and the grating couplers were patterned using dry etching. The highest measured coupling efficiency is 18.5% for a 25 nm thick SiO_2 slot layer. In addition to the device fabrication, development of a measurement instrument is presented. This set-up is a photonic wafer-scale probe-station.

The author performed 90% of the ellipsometry measurements, 100% of the simulations, 100% of the fabrications, 100% characterizations and wrote 90% of the manuscript. The author suggested the optical studies on the high-k films to correct the simulations. The author also developed 100% of the characterization set-up.

Paper III

In this paper fabrication and characterization of Al_2O_3 double slot grating couplers are discussed. The slot waveguide has a pair of 25 nm Al_2O_3 layers sandwiched by three amorphous silicon layers. Dry etching of the Al_2O_3 layers are explained in detail. A band reject filter is applied to minimize some of the Fabry-Perot resonance features in the transmission measurements. Using this filtering method the precision of transmission and the bandwidth of the grating coupler is increased. The effect of a top SiO_2 is investigated with simulations and practical results. It is shown that the coupling characteristics are affected by the SiO_2 cladding. The best coupling efficiency for the double slot grating couplers is 22% and the largest 2.5 dB bandwidth is 60 nm.

The author performed 100% layout design, 100% of fabrication, 100% of characterization and wrote 90% of the manuscript. The author suggested increasing the number of slots to have a stronger slot effect.

Paper IV

This paper reports the fabrication and characterization of Al_2O_3 double slot waveguides. The performance of the waveguides is reported for their transmission. Effect of the bulk amorphous absorption on the waveguide attenuation is studied. Effect of the forming gas anneal on the bulk absoption and the waveguide is studied. Annealing at 400 ℃ for 30 min lowers the attenuation from 81 dB/cm to 55 dB/cm and also changes the efficiency of the grating couplers. A method to calculate the waveguide attenuation from the measured bulk material optical properties is discussed. This method is based on finding the imaginary part of the effective refractive index of the waveguides given by mode analysis. Slot waveguides incorporating AlN and HfO_2 are also studied to find a minimized attenuation. Effect of the slot thickness on the attenuation of the slot waveguides is also studied.

The author performed 100% layout design, 100% of fabrication, 100% of characterization and wrote 90% of the manuscript.

Paper V

In this paper integration of the slot waveguides with selectively grown PIN germanium detectors is presented. This integration scheme is essential to realize photonic integrated circuits. The slot waveguide technology as a back-end deposited solution is presented for butt-coupling to the germanium detectors. Using propagation of light with finite element method, the coupling of the light to the detectors is presented. The selective growth of PIN germanium mesas is investigated. Growth of germanium with digermane precurser and hydrochloric acid is studied. A test chip containing high-k slot waveguides and germanium PIN mesas is demonstrated. The fabrication process for the test chip is discussed.

The author performed 90% layout design, 100% of fabrication, and wrote 90% of the manuscript. The author suggested the use of back-end deposited slot waveguides to demonstrate a basic photonic circuit

Paper VI

In this paper a cost effective solution for silicon photonics is presented. Back-end deposited waveguides and graphene as the active material are used. Embedding of the graphene photodetector in the waveguide is investigated. The waveguide design and the device structure is studied. The graphene layer is used as the active material to detect C-band signal. Test chips are fabricated utilizing the high-k slot waveguide technology and the transferring of the graphene. In order to enhance the light matter interaction the graphene layer is placed inside the slot. Basic photonic circuits are realized by fabricating the grating couplers, waveguides, and the detectors. The responsivity of the the integrated detectors is 3.6m A/W at 1.5 V for a 40 μm long detector.

The author performed 90% layout design, 50% of fabrication, 100% of characterization, and wrote 50% of the manuscript. The author suggested having the graphene layer inside the slot layer of the waveguide to have a better light interaction. He also suggested the amorphous waveguides as a cost effective solution for graphene integrated photonic circuits.

List of Symbols and Acronyms

Al_2O_3	Aluminum oxide
ALD	Atomic layer deposition
AlN	Aluminum nitride
a-Si	Amorphous silicon
AWG	Arrayed waveguide gratings
BEOL	Back end of the line
BOX	Buried Oxide
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
CPU	Central processing unit
dB	Decibel
dBm	Decibel-milliwatts
DBR	Distributed bragg reflector
DeMUX	demultiplexer
DI water	distilled water
FEM	Finite element method
FGA	Forming gas anneal
Ge	Germanium
HfO_2	Hafnium dioxide
IR	Infra red
ITRS	International Technology Roadmap for Semiconductors

LPCVD	Low pressure chemical vapor deposition
MUX	multiplexer
MZI	Mach-Zender interferometer
PECVD	Plasma enhanced chemical vapor deposition
PML	Perfectly matched layers
PMMA	Poly methyl metacrylate
RPCVD	Reduced pressure chemical vapor deposition
SEM	Scanning electron microscopy
SiGe	Silicon Germanium
SiO_2	Silicon dioxide
SOI	Silicon on insulator
TE	Transverse electric
TM	Transverse magnetic

Chapter 1

Introduction

1.1 Why Silicon Photonics ?

Transmitting data at the speed of light on circuit boards and microprocessors is the evolution of the short haul communication and semiconductor devices. CMOS technology will be facing a red brick wall for the interconnection of chips and off-chip communications [1–3]. The problem with electrical interconnects is not limited to board-to-board communication in server farms [4]. Optical links are favorable in chip-to-chip and even on-chip architectures [5].

The limiting factor in the systems is the power dissipation. This exists in many layers of the information-processing technology and even the semiconductor chips. In 2004, a study reported 50% of the power consumption in the processor [6]. In the later generations, it was expected that this consumption will be increased. This problem also extends to server systems. An estimate in 2005 showed that 1% of the power consumption worldwide was by the the data centers [7]. The carbon dioxide emission that the information and communication technology is accountable for was estimated to be half of a gigaton in 2002 [8]. The same study suggests that this carbon dioxide emission will rise to 1.4 gigaton in 2020. This is 2.6% of the carbon emission worldwide. Using optical interconnects and silicon photonics can improve the processor speeds and solve some system economics and environmental impact of the data centers.

In this work, the focus will be on the microprocessor interconnects. The high power dissipation in a chip is because of

1. Ever exceeding clock rates for on-chip and off-chip interconnects.

2. Higher density of interconnects per chip due to scaling.

A study has extensively evaluated the feasibility of the silicon photonics and the current status of the electronic interconnects in the information-processing units [9]. This study uses the projected clock rates to do this evaluations. These projections

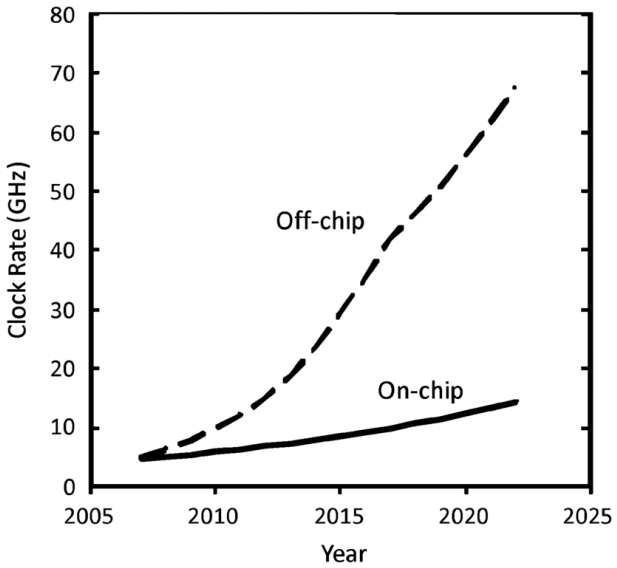

Figure 1.1: The required on-chip and off-chip speeds that are expected by the ITRS road map. Reproduced from [9] (David A. Miller, Stanford)

were done according to the ITRS road map. A 2022 hypothetical processor with this projection needs a 14.3 and 67.5 GHz clock speed for on-chip and off-chip interconnects, respectively. This evaluation finds optical interconnects a suitable replacement for global on-chip and off chip interconnects. The interconnect density issue can be addressed by optical wavelength division multiplexing. Implementing interconnects in the information-processing systems using silicon electro-optical devices has become a motivation for the information and communication technology. This optical "CMOS-based" technology uses the same platform to manufacture the circuits [10].

Silicon photonics on a chip requires a variety of components. A made-simple scenario for optical-chips is as follows: The light signal is generated in a light source which is a continuous wave laser. The generated light is guided and routed during all its travel in the chip by a network of waveguides. The light signals (zeros and ones) are produced by a device called light modulator and the the light is transformed to electricity in a photodetector. The light modulator and the detector are the ports to the electrical part of the processor. In silicon photonics, waveguides, grating couplers arrayed-waveguide grating multiplexer/demultiplexers, spliters, etc are dubbed "passive photonic devices". Devices such as modulators and detectors and emitters are called the "active photonic devices". An optical chip (a more modern wording "photonic integrated circuits") can be a complex system using all the mentioned essential components. The scope of this thesis is focused on grating

couplers and waveguides for the passive photonic devices and detectors for active devices.

1.2 Previous Work in Silicon Photonics

In this chapter the author will make an effort to introduce the current state of the art and developed technologies within the the scope of this thesis. A set of solutions that were implemented during the course work of this research will be proposed. The thesis will be outlined at the ending section of this chapter.

SOI Photonics

Today, a dominant number of publications in this field use SOI photonics as the foundation. Active and passive devices have been demonstrated by other groups. On a system level, chips have been reported using SOI wafers to produce photonic circuits. In 2009, a group demonstrated a photonic chip technology [11]. IBM has shown a nano-photonics chip integrated with a 90 nm CMOS framework [12]. Another work showed a 3D integration scheme for 300mm wafer scale manufacturing [13].

Because of two features, an SOI wafer can be used to make photonic circuits: 1) A thick buried oxide layer 2) Crystalline silicon device layer. For waveguiding purposes the second mentioned feature forms the core and the first one the bottom cladding layer. Waveguides are the basis for passive devices in a photonic circuit. In addition to waveguides, other passive devices have been demonstrated such as arrayed waveguides gratings (AWGs), Distributed bragg reflectors (DBRs), and waveguide crossings [14–16].

Active SOI devices have also been extensively studied in the literature. In 2004 intel corp. published an article reporting a light modulator built on an SOI wafer [17]. A metal-oxide-semiconductor capacitor with a maximum optical modulation speed of 1 GHz was reported. In this structure the real part of the refractive index is altered by the electrical bias, through the free carrier plasma dispersion effect. Since the real part of the refractive index is modulated, a mach-zender structure was used to produce amplitude modulation.

Later on, PIN all-silicon mach-zender modulators were introduced [18]. This study demonstrated a 15 GHz modulation speed. 50 Gb/s PIN modulators were demonstrated [19], and the power consumption was optimized by a traveling-wave contact design [20]. Ring resonator silicon modulators have been reported to have a speed of up to 40 Gb/s [21–23].

High speed photodetectors have also been demonstrated with SOI waveguides. Since the photodetector is one of the subjects focused on by this thesis, the author will extensively go through the state-of-the art with those devices.

Slot Waveguides

Recently slot waveguides have attracted interest in the silicon photonics research field. The main idea with a slot waveguide is to engineer the core of a silicon waveguide. A silicon waveguide has a core of silicon cladded with a low refractive index material such as SiO_2. A study from the Cornell university in 2004 [24] suggested that a low refractive index material inside the silicon core can cause some interesting effects. This study reported a high mode confinement in the low refractive index region of the core. The name of "slot" was coined by the same group as they experimentally demonstrated an SOI waveguide with a carved slot inside it [25].

These findings were the beginning for a variety of devices and applications of the slot waveguides. The progress in the research of slot waveguides is summarized in Table 1.1. What made the slot waveguides a presentable candidate for silicon photonics is the opportunities with active devices. Silicon has weak non-linear optical properties and using other materials with optical non-linearities as the slot region or inside the slot region can solve this problem. By means of filling the slot with optically non-linear polymers [26], light modulation and detection was presented. Another study have demonstrated a hybrid technology using silicon slot waveguides and organic non-linear polymers to fabricate 100 Gb/s MZI modulators [27]. A theoretical study proposed a light emitting device using erbium doped SiO_2 in a slot waveguide ring resonator [28]. Slot waveguides have also been used for bio-photonic applications. A biochemical sensor [29] and a label free optical bio-sensor [30] prototypes have been demonstrated.

The slot waveguide concept has been extended to "horizontal slot waveguides". In this method, instead of carving the silicon layer and filling the void with some low index material, the slot layer is deposited on a silicon layer and interposed by a second silicon layer. First studies on this type of slot waveguides were done presenting a polycrystalline silicon as the top silicon layer [31]. The effect of high optical absorption in the poly-silicon [32] affect the performance of these waveguide. Single and multiple slot waveguides were reported [33]. High quality factor ring resonators have been demonstrated using horizontal slot waveguides [34]. A light modulator [35] and a light emitter [36] were presented as well.

This thesis will focus on the horizontal slot solution. One reason for this choice is that production of the vertical slot waveguide requires a high resolution lithography system. E-beam lithography has been mainly used to make slot waveguides. A horizontal waveguide, on the other hand, is fabricated by means of deposition tools and the waveguides can be produced with an optical lithography stepper.

1.3 Proposed Solution for the Limitations of SOI photonics

Integration of the photonic wafer with the microprocessor requires flip chip bonding. This scheme is explained in [37]. The photonic interconnect layer is transferred from the SOI wafer to the top of the microprocessor layers. This integration scheme can

Details of the research	Year	Device Type	Reference
Theoretical and Experimental demonstration of slot waveguides	2004	Passive	[24, 25]
First light detector and modulator using non-linear optical polymers	2005	Active	[26]
Theoretical study for ring-resonator based erbium doped slot waveguides	2005	Active	[28]
First demonstration of horizontal slot waveguides	2007	Passive	[33]
Slot waveguides demonstrated for label-free biochemical sensors	2008	Passive	[29]
Mach-zender vertical slot waveguides with hybrid polymers as the non-linear material	2009	Active	[27]
High quality factor ring resonator slot waveguides. Silicon rich SiO_2 as the slot filling to produce silicon nano-crystals	2009	Passive	[34]
Ring resonator vertical slot waveguides with hybrid polymers as the non-linear material	2011	Active	[34]
Horizontal slot waveguide light modulator using titanium dioxide and active polymer	2012	Active	[35]
Experimental demonstration of an integrated light emitter using horizontal slot waveguide and erbium doped SiO_2	2013	Active	[36]

Table 1.1: A decade of slot waveguide development in silicon photonics literature and the applications in passive and active devices.

have some drawbacks including alignment precision and cost effectiveness. On the other hand the electrical interconnection technology in a microprocessor or so called "back-end of the line process" has a more straight forward procedure. The metal layers are deposited and patterned to form the interconnects. The photonic solution proposed in this thesis is inspired by the back-end of the line process in the CMOS technology. The main idea with this technology is to be able to deposit the dielectrics that form the waveguides and use growth techniques or 2D materials to realize active devices.

Deposited Horizontal High-k Slot Technology For High Yield and Reproducability

Low loss amorphous silicon layers have been demonstrated [38, 39]. These studies, support the idea that high performance passive photonic devices can be realized using deposited thin films. Optical losses in poly-silicon waveguides and the possible remedies have been also studied [32]. In 2013 two articles reported light modulators with back-end deposited poly-silicon structures [40, 41].

High-k thin films are well known in the CMOS transistor technology. These dielectrics are widely used in the transistor technology to solve the gate leakage problem [42]. In one study high-k layers were used in a graded index setup to enhance the transmission in slot waveguides [43]. In another work erbium doped Al_2O3 were studied to fabricate waveguide integrated amplifiers [44]. Recently, large wavelength light emitters were studied using thulium oxide doped layers [45]. Opportunities with high-k thin films in photonics have not been fully explored. In this work slot waveguides with high-k films as the slot layer are proposed. In order to have the photonic tool box, grating couplers were studied and fabricated.

1.4 SOI Integrated Photodetectors

Integrated Germanium Photodetectors

In order to couple the waveguides and photodetectors, in the SOI photonic technology, evanescent tail coupling and butt coupling solutions have been reported. In both of the methods the silicon device layer of an SOI wafer is used as the seed for the germanium growth. The germanium layers are grown using multi-step epitaxy to compensate for the lattice mismatch betwen silicon and germanium. This method uses a buffer layer that can suppress the dislocations in the grown germanium. Also, in the literature to improve the crystal quality of the grown germanum, cyclic annealing steps have been reported which will enhance the quality of the germanium [46]. This cyclic annealing also introduces strain in the germanium and consequently changes the band gap [47]. The low temperature buffer technology has developed some opportunities with active Ge and GeSn alloys. Light emission [48–52], modulation through the franz-keldysh effect [53–55], and detectors [56] have been shown using strained or highly doped Ge and GeSn alloys.

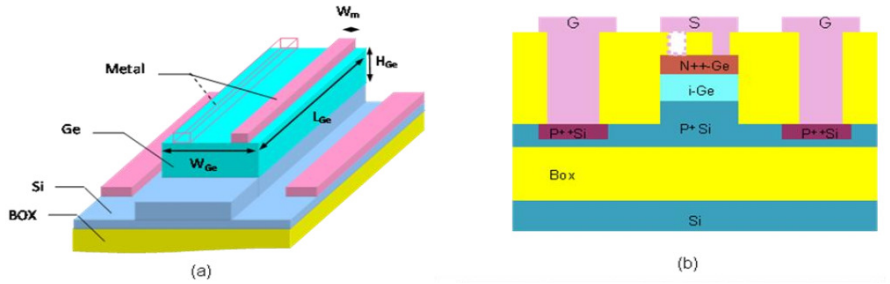

Figure 1.2: Schematics of the evanescent coupled detectors in (a) 3D view showing the growth scheme onto the waveguide and (b) cross section view showing the diode structure. Reproduced from a work by Liao et. al. [57]

Evanescent tail coupling in the SOI technology is implemented by growing the photodetector mesa on top of the silicon waveguide [57]. Fig. 1.2 (a) shows the 3D schematics of the integration using evanescent coupling. Reported photodetectors are mainly PIN germanium diodes [58] and metal-semiconductor-metal junctions [59]. The PIN diode cross section is shown in Fig. 1.2 (b). The p-type silicon device layer is used as the p-type semiconductor in the diode. The holes generated at the active region are collected at the extensions of the crystalline silicon waveguide. An intrinsic germanium is grown on the silicon layer which defines the active region of the photodetector. One benefit with this design is a direct contact between the waveguide and the active region of the photodetector [60,61]. An n-type germanium is grown onto the intrinsic germanium. The electrons are collected through this layer.

The guided mode is effectively coupled to the detector. The principle physics behind the operation of these devices is the high refractive index of germanium. At 1550 nm non-strained germanium has a refractive index of about 4.1. Refractive index of silicon at this wavelength is about 3.45. The guided mode in the silicon waveguide is gradually attracted to the germanium region and remains trapped in that region. This is due to the higher refractive index of germanium. In the areas where the germanium mesa is present the germanium layer becomes the waveguide core. The underlying silicon layer and the top cladding layer act as cladding layers. Due to a high 4 % lattice mismatch between silicon and germanium, a buffer layer is required for the growth of germanium. If graded SiGe layers are grown on the silicon, the buffer will be a low defect region. This is done by gradually increasing the germanium content in the SiGe layers. If a germanium layer is used as the buffer it will have a high defect density.

Another solution for waveguide integration is butt coupling of the photodetectors [62, 63]. Schematics of this solution is depicted in Fig. 1.3 (a). In this method the detector is placed at the end and front of the waveguide. The propagating mode is incident at the ending edge of the waveguide. In order to have a seed layer for

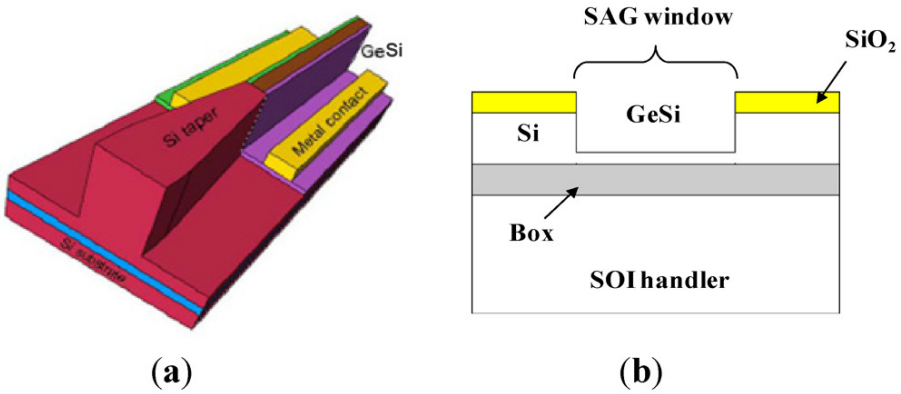

Figure 1.3: Schematics of the butt coupled detectors in (a) 3D view showing the growth scheme onto the waveguide and (b) cross section view showing the diode structure. Reproduced from [64] (Luo et. al. Oracle labs and Kotura)

the germanium growth the end of the waveguide is almost fully etched. Details of the photodiode is illustrated in Fig. 1.3 (b). A thin layer of silicon is left as the seed layer for the germanium growth. Similar to the evanescent tail coupled solution a buffer layer is grown on the silicon layer and an intrinsic Ge layer is grown. The stack is completed by a p-type Ge. The extensions of the silicon waveguide is used as the n-type semiconductor of the PIN stack. In order to make good ohmic contacts this part of the silicon requires a high doping. The doping is done using an ion implantation step and dopant activation annealing. The fabrication process is straight forward if the whole stack could benefit from in-situ doped layers to avoid ion implantation and an extra annealing step in the process. In both of the SOI integration schemes discussed so far the light interacts with the buffer Ge layer. This buffer layer has a low crystalline quality and a high density of defects. With the BEOL deposited solution this can be avoided both for evanescent tail solution or a butt coupled solution.

SOI Integrated Graphene Photodetectors

Graphene is one of the candidates for photonic applications. Prior to the photonic applications electronic graphene devices were demonstrated [65–68]. High speed applications seem to be a realm for graphene's success [69].The promising electro-optical properties of graphene are:

1. High carrier mobility in graphene promise high speed of operation both for detectors and modulators.

2. The Fermi level in graphene can be tuned by electrostatic doping. Being in contact with different metals or dielectrics can alter the Fermi level of the graphene. Using this effect a zero-bias detector can be produced. This can compensate for the high dark current density of graphene photodetectors. The high conductivity of graphene is a cause of a significant dark current in these devices.
3. The Fermi level in the graphene can also be tuned using a second graphene layer. Light modulators can be realised using this effect.
4. In combination using the above effects a multipurpose device can be realized. This device would function as a detector and a modulator. This will allow a monolithic integrated photonic scheme.
5. The absorption in graphene in the near-infrared range is not wavelength dependent. This is due to the zero band gap nature of graphene.

In the literature, photodetectors have been realized using graphene. Vertical incidence solutions have been presented by other groups [70–76]. A waveguide integrated solution is more effective [77–82], because in a vertically incident detector, a small fraction (2.3 %) of the light is absorbed. Even plasmonics applications of graphene have been explored [83]. The schemes that have been demonstrated for waveguide integration, use the SOI photonic wafer platform. Not only costly but in these methods the graphene is laid on the crystalline silicon waveguide.

1.5 Proposed Novel Intgration Schemes

Slot Waveguide and Germanium Photodetector Integration - A Cost Effective Solution

As an application for the high-k slot waveguides a butt-coupled solution is proposed and the fabrication process was investigated. In this solution germanium PIN photoetectors were fabricated using selective epitaxy of germanium.

Embedded Graphene Photodetectors for Enhanched Light-Matter Interaction

Placing the optically active material outside the waveguide will not yield to the highest light-material interaction. This is because the light will only interact with the evanescent tail of the waveguide mode. With a diffrent solution the graphene was placed inside the waveguide. This concept was implemented by means of the high-k ALD slot waveguide technology.

In addition to better light-graphene interaction, this technology does not require costly SOI wafers. The waveguide material stack is deposited using CMOS BEOL compatible temperatures. Using the monolithic scheme mentioned above no crystal epitaxy is required to fabricate active devices.

1.6 Thesis Outline

This thesis is organized in the following five chapters:

Chapter 2 is dedicated to the theoretical models and instrumentation details. The theoretical models used to simulate the devices will be explained in detail. The author has developed a photonic probe-station which is used through out this research. This measurement tool will be discussed. The chapter will continue with the material characterization methods and the equipment used.

Chapter 3 will discuss the design of the high-k slot grating couplers and the further optical studies will be explained.

In chapter 4 two waveguide-photodetector schemes will be introduced. The first solution will present the butt-coupled germanium photodetector scheme. The chapter will also go through the embedded graphene photodetector solution.

The fabrication process of the devices will be explained in chapter 5.

Chapter 6 will summarize the results for optical high-k thin film characterizations, grating couplers and waveguide performance, germanium detector and graphene photodetector properties.

The results of this work will be concluded and future outlook of this technology will be provided.

Chapter 2

Theoretical Models and Experimental Conditions

In this chapter the fundamentals of the simulation of the grating couplers and the waveguides will be explained. Finite element method (FEM) was used to simulate the grating couplers by wave propagation. This method was also used to perform mode analysis for the waveguides. Fundamentals of measurements and device characterizations will be explained. A photonic probe-station that was developed during the course of this work will be presented. Finally this chapter will go through some thin film and material characterization methods that were utilized in the research.

2.1 Finite Element Wave Simulations

Finite Element Method (FEM) is a reliable method for electromagnetic wave simulations. Partial differential equations are numerically solved by the FEM method [84]. Simulating a 2D structure requires less computational resources such as the computer memory and processor. Therefore 2D simulations are more favorable than 3D simulations, if possible. In this work in order to calculate the efficiency of the grating couplers, frequency domain FEM wave propagation method was used. In this method the Helmholtz equation is solved:

$$\boldsymbol{\nabla}^2 E + k^2 E = 0 \tag{2.1}$$

Where 'k' is the wavenumber and 'E' is a field vector. The electromagnetic wave was excited from one boundary and the propagation in the simulation domain was studied. The excitation boundary had a tilt which corresponds to the fiber tilt angle. The optical power in a second boundary can show the transmission or scattering of the wave in the structure.

The structures are rather complex and the propagation of the wave is affected by many different parameters. In case of the grating couplers the efficiency, leakage towards the substrate, back reflection and many more properties can be studied.

In order to avoid internal reflections in the simulation domain perfectly matched layers (PML) were used. Mode analysis simulations are useful for evaluation of the mode confinement, the effective refractive index and the modal attenuation in the waveguides. Effect of the slot layer on the guided mode was studied using 2D modal analysis simulations.

Wave Propagation Analysis For Grating Couplers

A grating coupler is a device to redirect the light from an optical fiber to the waveguides. Grating couplers are fabricated using a periodic structure at the end of the waveguide [85]. Schematics of a grating coupler is shown in fig. 2.1. An optical fiber that carries the signal delivers the incident laser beam to the surface of the grating coupler. Due to diffraction in the grating structure the light is re-oriented to the waveguide.

This device is reciprocal, which means that a propagating mode in the waveguide can be coupled to an optical fiber as well. The 3D simulations can be simplified to 2D simulations because the mode is highly confined in the waveguide. The grating has a width of 15 μm to be large enough to collect the incident beam from the optical fiber with a 10.5 μm diameter. The effective refractive index calculated for this waveguide is almost the same as an infinitely wide waveguide [86].

In fig. 2.2 the simulation of a single slot waveguide is demonstrated. The simulations were done in the RF module of COMSOL Multiphysics [87]. Frequency domain simulations were used to enable a wavelength sweep in efficiency calculations. In order to have the correct physics, the electromagnetic wave was excited from an external boundary that corresponds to the fiber tip facade. A TM-like mode was excited to ensure a slot effect. The only non-zero component of the magnetic field in the wave was in the z-direction. In fig. 2.2, the y-component of the electric field is plotted. For a horizontal slot waveguide the field enhancement is seen for the y-component of the electric field.

A fraction of the incident optical power will propagate in the waveguide. The coupler efficiency is defined by this fraction. The total incident power was calculated by integrating the optical optical power over the fiber tip length. The total coupled optical power was calculated by integrating the optical power over the waveguide cross section which in case of 2D simulations is a line. Further on, the surface reflections and optical leakage through the substrate can be calculated similarly.

Every sub-domain included the information about the optical properties of the materials. The main optical property in this simulation was the refractive index of the material. In this study the absorption in each material was neglected. As a rule of thumb the mesh size for wave simulations in COMSOL should be smaller than a 10th of the wavelength in the material [88]. As an example the maximum mesh size, in a silicon sub-domain, is 0.044 μm at 1.55 μm wavelength. This is due to the refractive index of silicon at 1.55 μm which is 3.45 [89]. In order to optimize the speed of simulation each sub-domain had a mesh density that is appropriate for

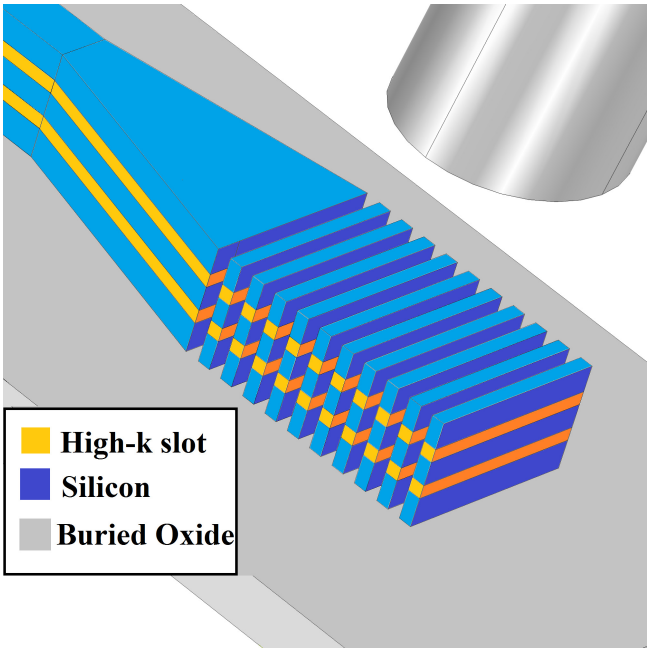

Figure 2.1: Schematics of a grating coupler. The figure is reproduced from paper III of this thesis

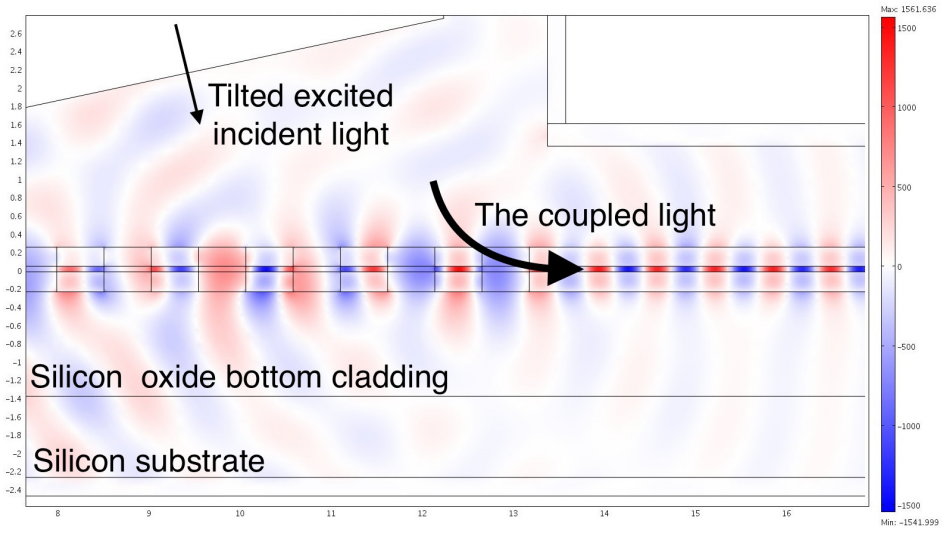

Figure 2.2: Simulation domain of the grating coupler for a single slot waveguide

its material. This way the regions that do not need a high mesh density consumed less computational resources, mainly the memory.

Perfectly Matched layers

The excited wave from the fiber propagates towards different directions in the simulation domain. The default external boundary condition in COMSOL Multiphysics is a perfectly conducting boundary. Because of this boundary condition, the wave will be fully reflected back from the external boundaries of the simulation domain. This will harm the simulations by interfering the propagation of the wave. In order to eliminate the reflections from the external boundaries, perfectly matched layer (PML) boundary condition was used. This way it was ensured that the wave incident at any external boundary leaves the simulation domain with no reflections.

Calling the PML a boundary condition is not an accurate definition. The PML condition is implemented by attaching extra sub-domains to the simulation domain A perfectly matched layer follow two physical principles: 1) it should have the same refractive index as its neighboring sub-domain in the simulation domain. This avoids any reflections at the interface between the simulation domain and the PML domain. 2) it should have an infinite absorption [90]. Although that the PML layer itself is terminated by a perfectly conducting boundary there will be no reflections due to an infinite absorption in the PML. In addition, the coordinate system for the PML must be set. In the case of the grating coupler simulations a Cartesian coordinate system was chosen.

Guided Mode Analysis

Analyzing the guided mode in the waveguide is useful to study the slot waveguides and the grating couplers in detail. Mode analysis was done using the RF module of the COMSOL Multiphysics. The cross section of the waveguide was used as the waveguide sub-domain of the simulation. The optical power is of the main interest since the distribution depend of the geometrical parameters [91].This cross section is basically a stack including silicon and high-k thin film layers. The structure was surrounded by SiO_2 cladding layers. External boundary condition in these simulations was set to perfectly conducting boundary. This simulation is only valid if the external boundaries are far enough from the waveguide region. An example of simulated guided mode is demonstrated in fig. 2.3. As shown in the simulation, the mode is highly confined in the waveguide region. Because of this, the perfectly conducting external boundaries will not affect the simulations. A similar meshing strategy as described in 2.1 was used. The simulator forms a matrix that describes the Helmholtz wave equation. This matrix results in a set of eigen-values. These eigenvalues in the COMSOL Multiphysics are given as the effective refractive indices or effective propagation constants. Every eigen value corresponds to a mode in the waveguide. These modes can be TM, TE or even mixed modes. In this study the TM mode was only of interest because it generates the slot effect [33]. In case of

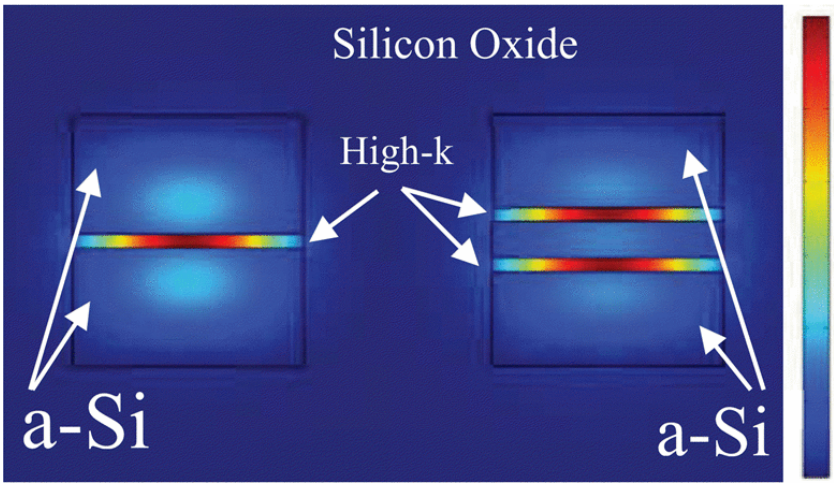

Figure 2.3: Optical power distribution in the mode analysis of slot waveguides. The guided mode in the single and double Al_2O_3 ALD slot waveguides. Presented in paper IV.

a vertical slot waveguide the TE mode will cause the slot effect. Only the eigenvalues (effective refractive indices) for a TM polarization were studied. This means that the x-component of the magnetic field should be zero in the entire simulation domain. A TM guided mode with a high mode concentration in the slot sub-domain is a slot mode. The real and imaginary parts of the effective refractive index can be used to find:

1. The effect of the slot layer thickness on the effective refractive index of the slot waveguides (used in paper I).

2. The effect of the slot layer refractive index on the effective refractive index of the slot waveguides (used in paper II).

3. The waveguide attenuation by the material absorption (in paper IV).

4. The optical power confinement in the slot or the silicon region [33].

Wave Propagation Simulations

Prior to the fabrication of the grating couplers the device characteristics were simulated. A key characteristic of a grating coupler is the coupling efficiency spectrum. This spectrum was simulated by sweeping the incident wave wavelength. Maximum coupling efficiency, peak wavelength and 3dB bandwidth can be extracted from this

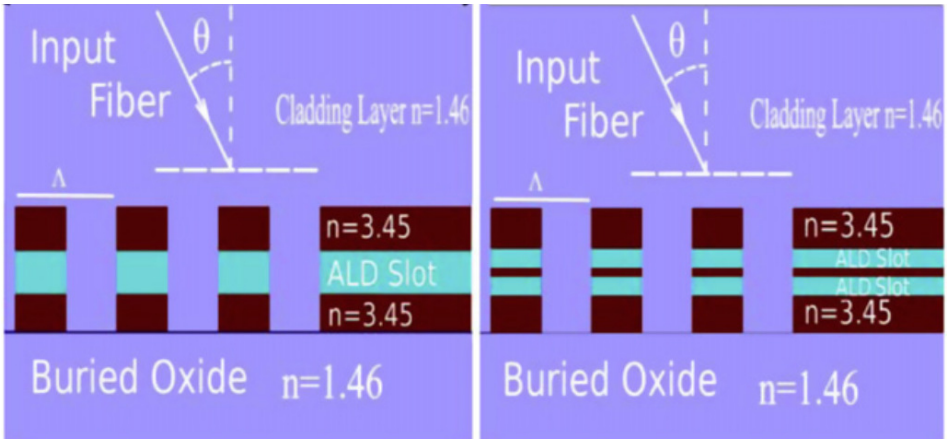

Figure 2.4: Showing side view schematics of the grating couplers. The grating coupler period and the material stack layering are illustrated. Reproduced from paper II [92].

spectrum. Using simulations, the effect of the geometrical parameters and the material stack on the coupling spectrum was studied. The grating coupler schematics is shown in fig. 2.4. (Λ) represents the grating period. Atomic layer deposited slot layers are interposed by silicon layers. The fiber delivering the incident light is tilted at (θ) angle. The multiphysics simulations were organized as below:

1. The effect of the grating period on the coupling efficiency.
2. Slot size effect on the coupling. (Slot size in case of horizontal slot waveguides is the thickness of the deposited slot layer.)
3. The effect of the slot material and refractive index on the coupling efficiency.
4. The effect of the bottom cladding thickness on the coupling efficiency.

2.2 Measurement Setup Features

In order to characterize the fabricated photonic chips, there is a need for a photonic probe-station. Electrical probe-stations are mature in the microelectronics industry. Research and industrial scale electrical probe-stations are commercially available. These probe-stations are facilitated by a number of electrical probes. The probes are connected to source/meter units that can apply or measure voltage and current. The probes can be used to characterize electron devices such as diodes, transistors or even electrical circuits. An important feature of these probe-stations is wafer scale measurements.

Wafer Scale Photonic Probestation

Inspired by the features mentioned above, a wafer-scale photonic probe-station was developed. The setup is presented in fig. 2.5. In order to characterize a photonic integrated circuit at least a pair of optical fibers are required. One optical fiber injects the input signal into a grating coupler while the other picks up the output signal from another grating coupler. A photonic probe-station can have the features as below [92]

1. Enabling wafer scale measurements. One of the benefits with grating couplers is wafer scale measurements. Unlike in the other couplers such as nano-tapers or butt couplers, the wafers do not require dicing.

2. Accommodate optical probes as well as electrical probes. This enables all-in-one electro-optical measurements.

3. Designed for grating couplers. Angled fibers almost touching the surface of the wafer. The position of the fibers need to be mechanically manipulated.

4. Tunable fiber angle. This enables the flexibility of the system for different grating coupler designs.

5. Polarizers to change the polarity of the input signal. In addition to geometrical parameters, grating couplers are sensitive to the polarization of the input light. In case of slot waveguides the TM mode is only of interest.

6. Accurate XYZ positioners to efficiently deliver the guided beam onto the grating coupler surface.

The developed probe-station uses two fiber chucks to accurately point the fiber in a straight direction. The fiber chucks are held by steady fiber chuck holders fig. 2.6 (a) shows the fiber chuck and the fiber chuck holder. The fiber chuck holders are attached to a rotational stage. By means of this rotational stage the angle of the fiber can be tuned, as shown fig. 2.6 (b). The incident angle tuner has a precision of 6 Arc-second. Furthermore, the angle of the fiber can be measured by an accelerometer attached to the fiber chuck holder.

The rotation stages were mounted on XYZ piezo-motor positioners. This type of positioners were used for a maximal optical coupling. The best coupled optical signal is achieved if the beam spot is fitted inside the grating coupler surface. An accurate XY positioner can ensure that the spot is positioned at the most optimal location on grating coupler. The beam injected from the optical fiber is a Gaussian beam. This beam spatially diverges as it travels farther from the fiber tip. This makes the beam waist larger than that of the optical fiber core. In this work optical fibers with cores of 10.4 μm were used.

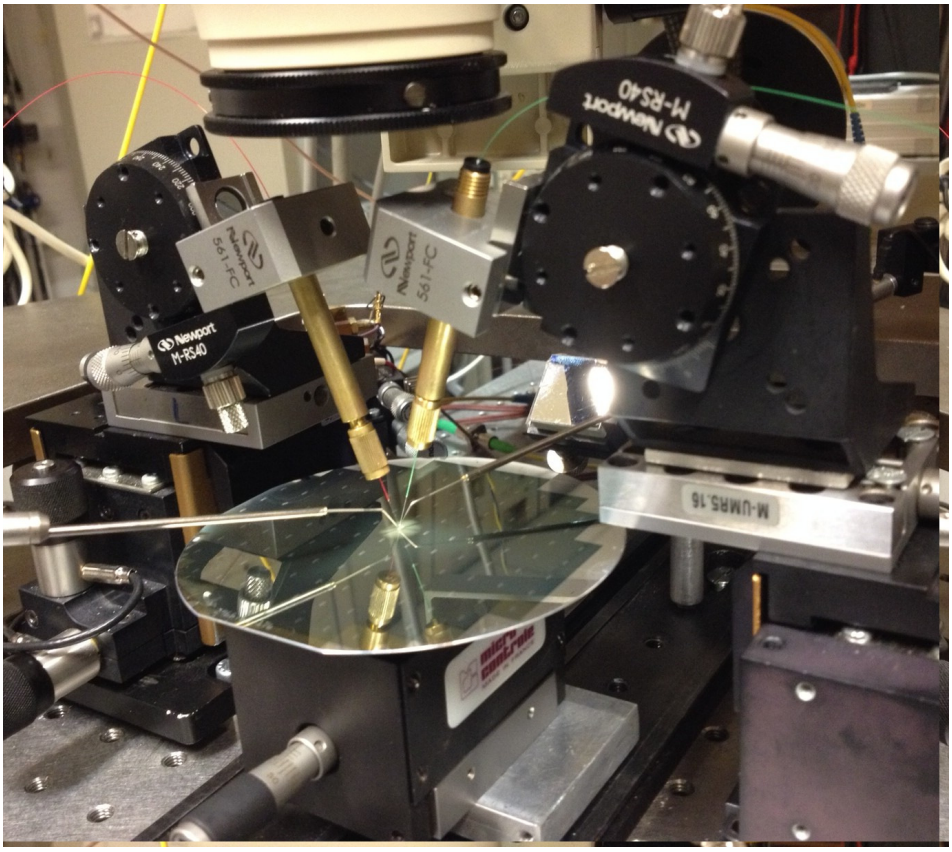

Figure 2.5: The probe-station with two optical fiber probes for light injection and pickup and two electrical probes.

Infra-Red Light Source

The laser beam is delivered from a solid state Agilent 81689A tunable laser. The wavelength can be tuned in the range of 1524 nm to 1576 nm. The highest laser power deliverable in the optical fiber is 5 dBm (0.003 W). The polarization of the input light is set by a polarizer. The picked up output signal from the chip is delivered to an IR detector. In order to measure the bandwidth of photodetectors a light modulator can be used to generate light pulses. This light modulator should be placed behind the polarizer and in front of the angled fiber stage.

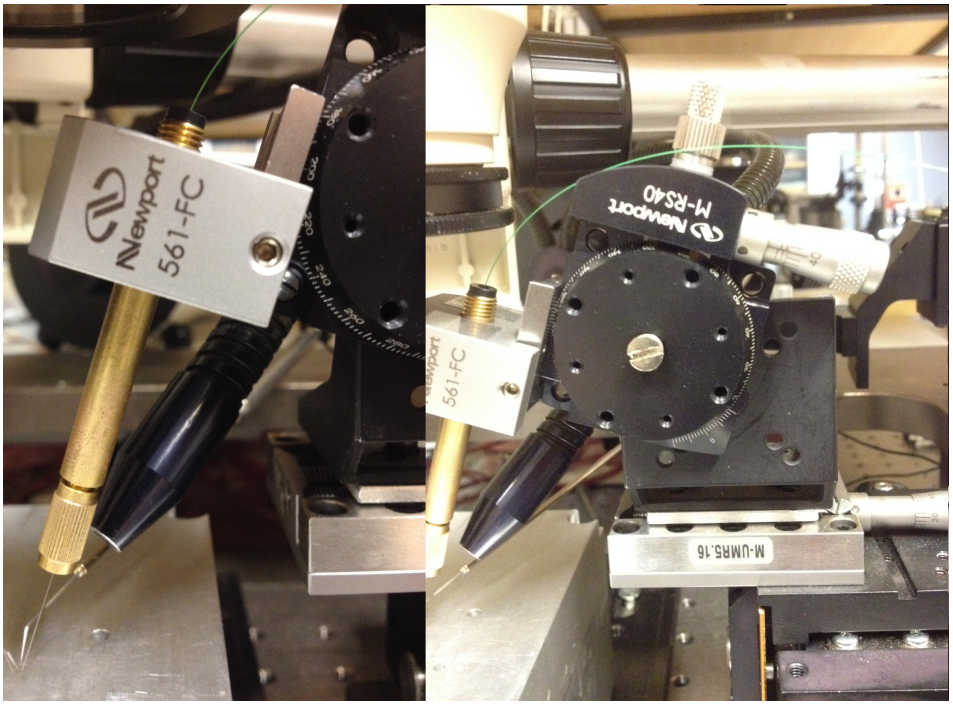

Figure 2.6: (a) The fiber chuck and the fiber chuck holder. (b) Shows the the rotation station that holds the fiber chuck holder and is responsible for setting the angle of incidence.

Characterization Methodology

The chips contained arrays of waveguide sets. Each element of the array contained a waveguide set with the same grating coupler period. The grating coupler period was incremented from 970 nm to 1060 nm with an increment of 10 nm. Each waveguide set had waveguides with incremented lengths. A sample waveguide set is depicted in 2.7. The transmission was measured for all of the waveguides in the set. The total loss in the optical links have two main components. The relation for the loss can be expressed as below if a logarithmic scale is assumed:

$$L_t\ (dB) = L_c\ (dB) + L_w\ (dB) \tag{2.2}$$

Where L_t is the total loss in the optical link, L_c loss in the couplers (also called the insertion lass), and L_w loss in the waveguide. optical loss was calculated by subtracting the power (in dBm) transmitted in a pair of waveguides. This subtraction product was divided by the length difference to give the attenuation

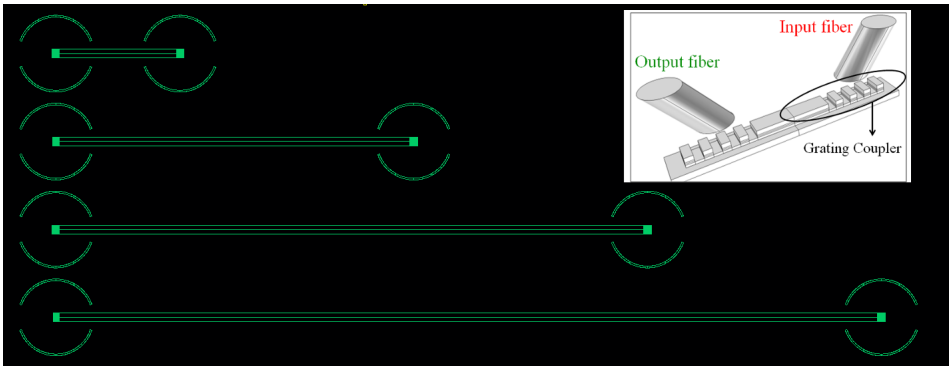

Figure 2.7: The mask for the waveguide/grating characterization set. In every set, identical grating couplers were designed the waveguides had various lengths. This enabled loss measurements.

per unit length.

$$l_w = \frac{(P_2 - P_1)}{L_2 - L_1} \, (\frac{dB}{cm}) \tag{2.3}$$

In the equation above P represents the transmitted optical power and L the length of the waveguides. The measured transmission is a function of the coupling spectrum. The maximum transmission was used for 2.3. The total attenuation in the waveguide was found by multiplying the l_w by the length of the waveguide. This will give L_w in 2.2. Using the total loss L_t and the waveguide loss L_w in 2.2 the grating coupler insertion loss was calculated. This insertion loss corresponds to the insertion loss in a pair of grating couplers (input and output grating couplers). Since the calculations were done in the logarithmic scale the insertion loss in a single coupler is given by

$$l_c = \frac{L_c}{2} \, (dB) \tag{2.4}$$

Where l_c is the insertion loss of a single grating coupler. This relation is based on the reciprocity of the grating couplers [93]. In addition to the losses in the waveguides and the grating couplers, the coupling spectrum was measured for various grating periods.

Transmission Spectra Filtering Method

In order to give a more accurate measure of the coupler insertion loss, a filtering method was developed to suppress the coupling spectrum noise. This noise has interferometric patterns and is caused by resonance cavities. One of the major resonance cavities is formed at the both ends of the waveguide and the back-reflections

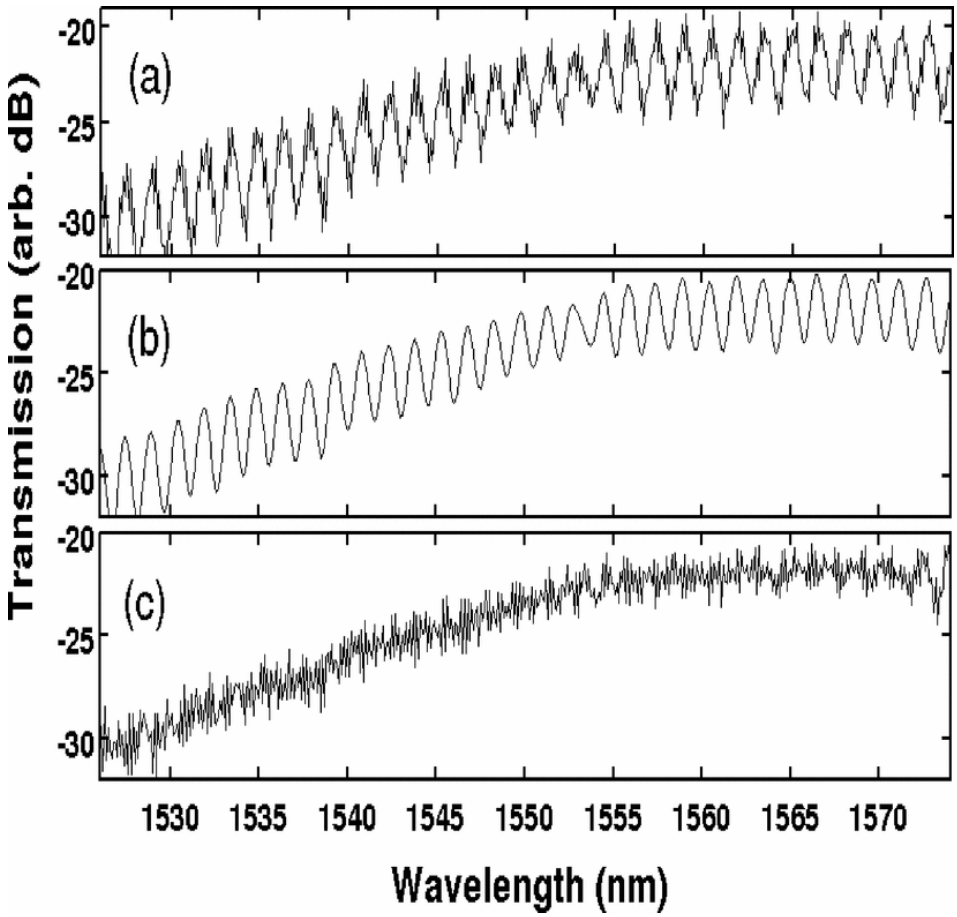

Figure 2.8: The filtering method for the transmission spectrum. (a) The raw measured transmission (b) the resonance features that need to be filtered (c) result of the band reject filter on the original spectrum. Reproduced from paper III in the thesis.

at the grating couplers. This filtering method is illustrated in fig. 2.8. In the measured spectrum, two major type of fluctuations can be seen. In this method the intention is to filter a resonance pattern which corresponds to a rather small cavity. Fig. 2.8 (b) exclusively shows this fluctuation. In order to filter this pattern in the transmission spectrum a band reject filter was used. The result of this filter can be seen in Fig. 2.8 (c).

2.3 Thin Film Characterization Techniques

The high-k thin films were investigated during this work. This was done to optically characterize the slot layers and also evaluate the etching process. Spectroscopic ellipsometry was extensively used to find the optical numbers associated with high-k layers and also etching of the high-k layers. For small features the mechanical profiler was used. This is due to a limit in the spot size of the ellipsometry equipment which is 200 by 200 μm.

Spectroscopic Ellipsometry

Ellipsometry is a contact free characterization technique. Dielectrics, semiconductors, and thin metals can be studied using ellipsometry. Thickness, optical constants, roughness and other material properties can be measured. The physical principle of ellipsometry is to measure the change in the polarization of incident light as it interacts with the film(s) [94]. This change will appear by the reflections from different interfaces in the material stack, absorption in the films and also scattering effects. Spectroscopic ellipsometry uses a wavelength (in other words photon energy) spectrum of measurements to determine the optical constants and the thickness of the layers.

Each material is represented by their dispersion model. In order to measure the optical numbers, dispersion models were developed. An ellipsometric model includes the dispersion relations for each of the materials in the stack. The dispersion relations are already developed and measured for well known and highly used materials in the industry. Crystalline silicon, poly-silicon, silicon dioxide and more are examples of these materials. In this work, the dispersion relation for the thin films, deposited by ALD, was developed. This is due to different film properties than reported in the literature.

The dispersion relation was developed by measuring several samples with deposited high-k films. For each high-k material, samples were prepared with various film thicknesses. For each material a suitable dispersion model was used. For HfO_2, Al_2O_3 and AlN a 'new amorphous','Cauchy absorbent' and 'new amorphous' models were used, respectively [95, 96]. The dispersion relation for each material is determined by the parameters in the dispersion models [92]. In order to find the right model parameters a set of fittings were done.

1. Silicon wafers with deposited high-k films were prepared.

2. The wafers were measured using spectral ellipsometry.

3. The model parameters were swept using initial guesses and the error (deviation from the measurement) was registered.

4. A model with the smallest error is accepted as the best model.

In addition to this procedure, itterations were used to confirm the validity of the model. Assuming that the ALD has a constant deposition rate over time, samples with various thicknesses were prepared. Thickness of the high-k layer is determined by the number of deposition cycles. Therefore, it is expected that the film thickness is scaled with the number of cycles. The model was tested against different film thicknesses and the parameters were fine tuned through iterations. After this cycle the model that can predict a scaled thickness with the lowest error is accepted. Using this stable model, the optical numbers (n, k) were extracted from the ellipsometric dispersion relation.

Mechanical Profilometer

A mechanical profilometer is used to measure step height and roughnesses on a surface. It can also be used for film stress measurements. This technique is operated essentially in a contact mode. By horizontal scanning of a diamond stylus on the surface the variations on the surface are measured. An analog signal is generated by the change in the vertical position of the stylus. In case of small features this method was used to measure the etch depth in high-k layers to find the etch rates. The profilometer was also used to measured the step height of the grown germanium mesas and the etched germanium.

Chapter 3

High-k Slot Grating Couplers

This chapter studies the slot grating coupler design and the theoretical performance of the couplers. Single slot fully etched, double slot fully etched and single slot partially etched coupler designs will be investigated. The effect of the slot layer thickness and material will be also explained.

3.1 Fully Etched Grating Coupler Design

The grating couplers for crystalline silicon waveguides are partially etched. The periodic grating structure is patterned using a different mask than the waveguide and the etching is done triggering an accurate etch depth. The grating coupler operation is sensitive to this etch depth and angle of incidence [97,98]. This can be avoided by a fully etched design. However, the refractive index contrast between silicon and the cladding material (SiO_2) is high. A fully etched grating coupler for crystalline silicon will suffer from high back-reflections [99]. Due to these reflections the efficiency will be very poor.

On the other hand, slot waveguides have a much lower effective refractive index than an all-silicon waveguide. This is due to a high confinement of the guided mode in the low refractive index slot region. Taking advantage of this property of the slot waveguides, it was possible to make fully etched slot grating couplers. A fully etched structure features:

1. A Single mask process. The waveguides and the grating couplers are fabricated through the same mask.

2. A More reproducible device manufacturing process. The grating coupler yield is affected by the variation in the etch depth. This is solved in a fully etched design.

The partially etched grating couplers for the SOI photonics should not be mistaken with the grating couplers introduced in 3.2. The partially etched slot grating

couplers in 3.2 use a single mask step like their fully etched counterparts. This design can be used regardless of the number of the slot layers in the waveguides. In this work single and double slot high-k slot couplers will be presented.

Fabrication Process Considerations

The grating couplers were designed to be compatible with the in-house processing equipment. One of the limitations in the fabrication process was the lithography resolution. In order to pattern the waveguides and the grating couplers an i-line stepper was used. The grating couplers have a filling factor of 50 %. This means that the smallest resolvable grating period is 960 nm. Because of a lowered effective refractive index in the slot waveguides the grating coupler period is not limited by this resolution.

The device structure was designed for an etching endpoint detection system. The etch endpoint detection algorithm in a dry etching equipment is responsible for stopping the etch process [100]. This mechanism is triggered when the etching of the material is finished and another material layer is reached. In the case of the fully etched grating couplers, the last etching step is the bottom silicon etch. This etch step will be stopped by the endpoint detection algorithm at the bottom SiO_2 cladding layer.

Theoretical Grating Coupler Performance

Grating couplers with Al_2O_3, HfO_2, and AlN high-k slot layers were simulated. The bottom SiO_2 layer causes strong reflections at the waveguide and substrate interfaces. These reflections make interference patterns at the grating coupler. Due to this interference pattern, the coupling efficiency can be enhanced or degraded. By using an infinite SiO_2 bottom layer in the simulations an average coupling efficiency was calculated.

The slot waveguide was formed by two 220 nm silicon layers interposing a 50 nm high-k ALD layer. The high-k layer in this simulation was Al_2O_3. For this slot waveguide The grating coupler a 990 nm grating period was required to achieve a peak efficiency at 1.55 μm. Fig. 3.1(a) shows the peak efficiency of 24 % and 80 nm 3dB-bandwidth was calculated. To compare the performance and efficiency tolerance to the variations, a partially etched structure was also simulated. An efficiency peak at 1.55 μm was achieved with a grating period of 935 nm. The coupling efficiency was 30 % and the 3 dB bandwidth was 75 nm. Since an infinite silicon oxide layer was used in the simulations the efficiency has an average value. In all grating coupler designs the bottom and top cladding layer are highly reflective [101].

The simulations showed that a partially etched grating coupler with less etch depth have higher efficiencies. Shallower etch depth creates less perturbations in the waveguide. Less perturbation in the waveguide will have a weaker effect on the effective index. A lower refractive index contrast will cause less back-reflections

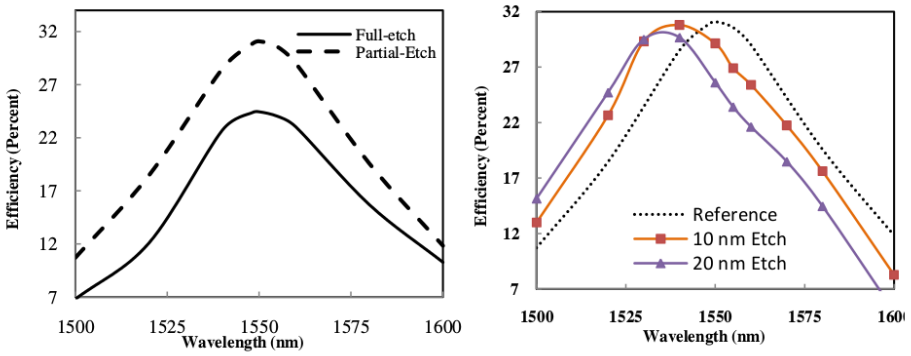

Figure 3.1: (a)Performance of the fully etched grating couplers and comparison with partially etched grating couplers. (b)Sensitivity of partially etched grating couplers to the etch depth. Reproduced from the paper I in the thesis [102].

from the grating coupler to the waveguide and increase the coupling efficiency. However, the calculated grating periods for shallower etch depth required a smaller grating period. The partially etched grating coupler simulated here as an example, had a grating period of 935 nm, which was out of the lithography resolution limits.

The partially etched couplers show a higher efficiency. Despite this higher efficiency, it is worthwhile to study the sensitivity of the grating couplers to the variations in etch-depth. Fig. 3.1(b) shows the performed simulations with varied etch depths. The simulations showed that a 10 nm over-etching of the grating structure degrades efficiency at 1.55 μm by 3 percent. This degradation was even more severe with a 20 nm over-etching. The coupling efficiency was lowered to 23 % at 1.55 μm. In 3.2 a partially etched grating coupler is discussed. This solution solves the variation tolerance problem of the partially etched couplers. In addition, a more suitable grating period was achieved to fit the lithography resolution. This was done by using a thicker slot layer. The effect of the slot thickness on the grating period is discussed in 3.4.

3.2 Novel Partially Etched Coupler Design

The schematics of this grating coupler is shown in Fig. 3.2. One of the main features of this slot coupler is that the slot layer in not at the center of the waveguide. Moving the slot layer towards the bottom silicon layer will result in a grating period which is suitable for the lithography resolution.The fabrication process has the following details

1. The grating couplers and the waveguides are fabricated using a single mask.

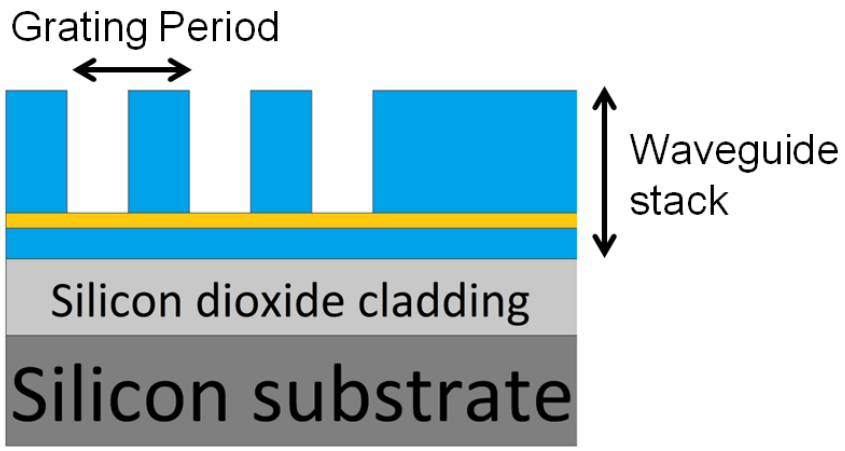

Figure 3.2: Schematics of the partially etched slot waveguide design.

2. It is straightforward to achieve a precise etch depth. The high-k ALD slot layer is a good etch stop and the top silicon etching is stopped by endpoint detection.

This design is specially useful for embedding of 2D materials in the slot waveguide [103]. In chapter 5 embedded graphene photodetectors are introduced. Due to its 2D nature, graphene layers can be harmed during etching steps. In order to embed the graphene inside the waveguide it needs to be buried in a protective film. The high-k slot layer can protect the graphene from unwanted harm during the rest of the fabrication process. The partially etched grating coupler and waveguide is a suitable design for this application.

3.3 Double Slot Vs. Single Slot Waveguides

Increasing the number of slots in a slot waveguide can increase the slot effect [104]. A double slot waveguide will have a higher mode density in the slot region than a single slot waveguide. In case of embedding an optically active material in the slot region a double slot structure is favorable. The interaction between the optical mode and the active material is higher in a double slot structure [105]. Using this effect, active photonic devices with smaller footprints can be manufactured.

50 nm total slot layer thickness		
Slot Material	Single Slot Waveguide	Double Slot Waveguide
AlN	28%	39%
HfO_2	31%	45%
Al_2O_3	32%	50%

Table 3.1: Confinement of the guided mode in high-k single and double slot waveguides. Simulations are done using mode analysis and integrating the optical power in the slot region.

Mode Confinement and Effective Refractive Index

In order to study the mode confinement, mode analysis simulations were done in the RF module of COMSOL multiphysics. The simulations were done according to the specification described in 2.1. In the calculations, a total slot thickness of 50 nm was assumed. The single slot waveguides had a 50 nm high-k layer and the double slot waveguides had a pair of 25 nm high-k slot layers.

In order to calculate the mode confinement, the optical power was integrated over the slot region and the whole waveguide. Optical mode confinement in single and double high-k slot waveguides are compared in Table 3.1. the optical confinement is enhanced from 32% to 50% for Al_2O_3 double slot waveguides. A similar enhancement has also been reported by another work [33].The optical properties of a thin film govern the field enhancement and the confinement factor in a slot waveguide [106]. The effect of the high-k material on the slot grating and field enhancement is extensively discussed in 3.4.

The effective refractive index of the double slot waveguides is also affected by the field enhancement in the slot region. The confinement factor in the slot region determines the effective refractive index of the waveguide. A double slot waveguide has a lower effective refractive index. This is because of a higher mode concentration in the slot region that has a significantly lower refractive index than silicon. Table 3.2 summarizes the effective refractive indices for single and double slot waveguides.

Grating Coupler Design

As it was shown, the waveguide characteristics change by increasing the number of the slots in the waveguide. This will have a direct effect on the grating coupler design. Due to a lower effective refractive index in the double slot waveguides the grating couplers will have a larger suitable grating period [101]. Table 3.3 summarizes the suitable grating coupler period for HfO_2, Al_2O_3 and AlN slot grating couplers. The grating periods calculated here are based on the reference values for the refractive index of the high-k films. In 6.1 it will be shown that the

50 nm total slot layer thickness		
Slot Material	Single Slot Waveguide	Double Slot Waveguide
Al_2O_3	2.48	2.38
HfO_2	2.64	2.52
AlN	2.73	2.59

Table 3.2: Effective refractive index of high-k single and double slot waveguides at 1.55 μm wavelength.

Grating coupler period 50 nm total slot layer thickness		
Slot Material	Single Slot Waveguide	Double Slot Waveguide
AlN	960 nm	975 nm
HfO_2	970 nm	985 nm
Al_2O_3	990 nm	1016 nm

Table 3.3: Suitable grating coupler period to have a peak coupling at 1.55 μm.

optical characterization of the high-k films showed different properties than what is reported in the literature. Therefore, the optical confinement, effective refractive index, and the grating periods should be recalculated using the measured optical numbers.

A double slot grating coupler design will have slightly better efficiency. Due to a lower effective refractive index in the waveguide, the reflections at the perturbed parts of the waveguide are less [100]. The fabrication design for these grating couplers is similar to the single slot grating couplers. A single mask process is used to fabricate the waveguides and the grating couplers.

3.4 High-k Slot Layer

The operation of the grating coupler is sensitive to the high-k slot film. This is because of a high mode confinement in the nano-scale high-k slot film. Design of the grating couplers depending on the slot film thickness and refractive index is studied.

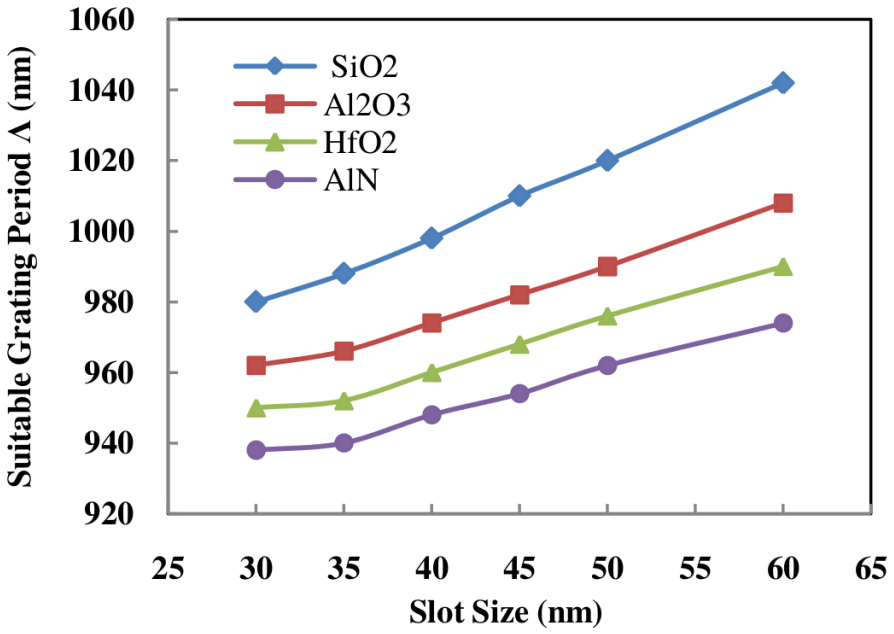

Figure 3.3: Single slot grating coupler design for several high-k dielectric films. Suitable grating coupler period for a peak coupling at 1.55 μm. Grating couplers with SiO_2, Al_2O_3, HfO_2 and AlN slot layers are shown. Paper I [102]

The effect of the Slot Thickness

In order to understand the effect of the slot layer on the grating coupler design a four sets of simulations were done for SiO_2, Al_2O_3, HfO_2 and AlN. Since the structure is fully etched the only parameter that can be changed in the grating coupler is the grating period. The grating couplers were designed to have a peak coupling efficiency at 1.55 μm. Fig. 3.3 summarizes the results for several thicknesses of the slot layers. The total waveguide height is kept constant. The simulations show that in order to maintain the coupling efficiency peak wavelength a larger grating coupler period is required for a thicker slot layer. This is because of a reduction in the effective refractive index of the slot waveguide. A slot waveguide with a larger slot region can accommodate more of the optical mode [24, 25]. Increasing the optical mode in the low refractive index slot region reduces the effective refractive index of the waveguide. The grating period (Λ) suitable for coupling at λ_0 is related through [107]:

$$\Lambda = 2\lambda_0/(n_{eff}^{upurt} + n_{eff}^{purt} + 2n_c \sin\theta^c) \tag{3.1}$$

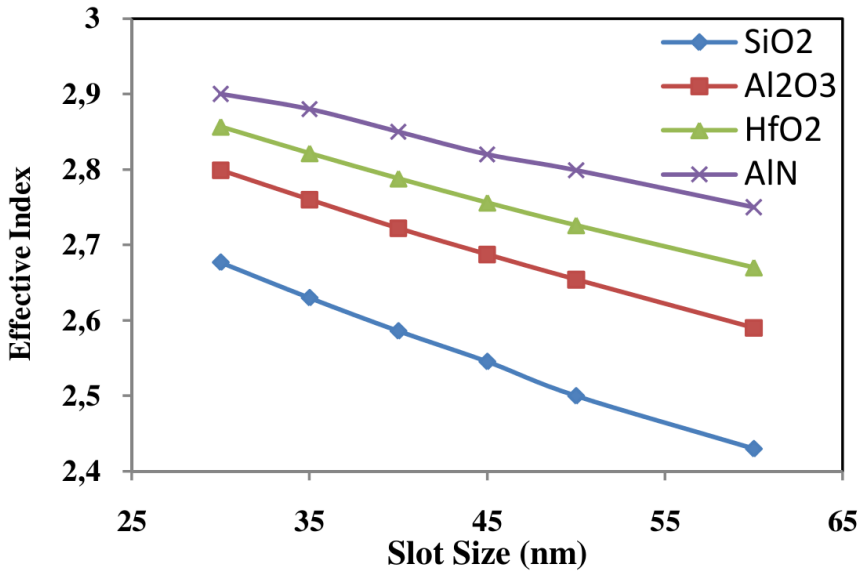

Figure 3.4: Effect of the slot size and material on the effective refractive index of the slot waveguide. In paper I.

Where n_{eff}^{upurt} is the effective refractive index of the unperturbed waveguide. n_{eff}^{purt} is the effective refractive index of the perturbed waveguide. n_c is the refractive index of the top cladding layer of the grating coupler and θ^c is the incident light angle. Since the light is injected using an optical fiber this angle is the fiber tilt in the measurement setup. The fiber tilt is 17 degrees. Disturbing the waveguide geometry defines the perturbation. By etching the waveguides using a periodic pattern, perturbation is applied. n_{eff}^{upurt} is the effective refractive index in the original waveguide. Equation 3.1 shows that a smaller effective refractive index in the unperturbed waveguide increase the suitable grating period (Λ).

In order to understand the unperturbed waveguide effective refractive index, 2D mode analysis simulations were done. The results are summarized in Fig. 3.4 [102]. A thicker slot film will lower the effective refractive index of the waveguide. Decreasing the n_{eff}^{upurt} in equation 3.1 will increase the grating period.

A larger grating coupler period translates to a more reliable lithography process. For the slot waveguides developed in this study (also illustrated in Fig. 3.3) the grating period is in the range of 940-1040 nm. This requires a minimum feature resolution of 470-520 nm in the i-line stepper. Achieving successful lithography results will be more a challenge with smaller features. Therefore it is beneficial to increase the slot layer thickness for a more successful fabrication process.

Slot Material	Reference Refractive Index
Al_2O_3	1.74 [108]
HfO_2	1.9 [110]
AlN	2.1 [109]

Table 3.4: Reference refractive index of high-k films at 1.55 μm.

The effect of the Slot Material

The grating coupler design is also sensitive to the high-k slot material properties. The refractive index of the high-k thin film influences the field enhancement in the slot region. A stronger field enhancement occurs for a high-k material with a lower refractive index. More field enhancement causes a higher mode density of the mode in the slot region. This will decrease the effective refractive index in the waveguide and increase the suitable grating period. Calculations presented in Fig. 3.3 and 3.4 were done using the reference refractive indices for the high-k films [108–110]. These refractive indices are listed in table 3.4. AlN has the smallest grating coupler period among all of the high-k materials studied in this work. Among all of the materials studied, SiO_2 has the lowest refractive index. As it can be seen in Fig. 3.4 slot waveguides with SiO_2 have the lowest effective refractive index.

The refractive index of the high-k films deposited by ALD do not necessarily have the same refractive index as the references. The refractive index of a film depends on the deposition technique.

Chapter 4

Photodetector Integration

In this chapter two integration solutions for the slot waveguides will be presented. First, the integration with germanium PIN photodetectors will be discussed. The chapter will continue with the design of an embedded graphene photodetector that takes advantage of the slot waveguide features.

4.1 Back-End Deposited Waveguide Detector Integration

Integrated photodetectors can be implemented in the amorphous BEOL deposited photonics technology. The growth seed layer for these detectors is the bulk silicon substrate. In this solution, the photodetector active region is placed in front of the waveguide. The guided mode in the slot waveguide is incident to the edge of the detector. The 3D schematics of the device is depicted in Fig. 4.1. A double slot high-k ALD waveguide delivers the light to the detector [111]. Since the diode is epitaxially grown, the placement of the PIN diode layers can be tuned. The p-type germanium should be grown to a thickness that is leveled with the bottom SiO_2 cladding. The intrinsic layer which is the active region for the detector will be aligned in front of the waveguide if it has the same thickness as the waveguide. This will ensure an effective light injection in the detector.

Using COMSOL Multiphysics this solution was simulated. Propagation of a TM mode was simulated in the double slot high-k waveguide. Coupling of the light into the germanium is illustrated in Fig. 4.2 [112]. Reflections at the waveguide-Ge interface is 6%. In this work the butt coupled solution is studied. The fabrication of this solution was studied by the steps below:

1. Waveguide material stack deposition.
2. Single mask lithography and etching of the grating couplers and waveguides.
3. Etching of the diode openings to the silicon substrate.
4. Growth of the PIN Ge mesa.

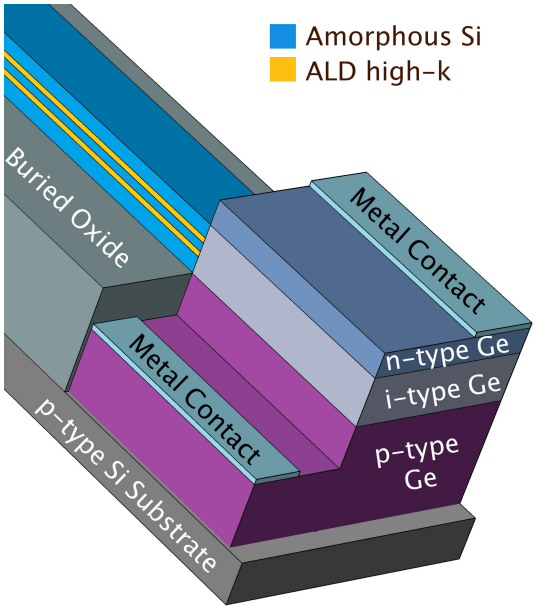

Figure 4.1: Schematics of the BEOL deposited butt coupled detector. A double slot high-k ALD waveguide terminated by a PIN Ge detector. The intrinsic region of the detector has the same thickness as the waveguide. This region should be aligned in front of the waveguide. Reproduced from paper V.

5. germanium etch to access the p-type part of the stack.

6. Metalization of the contact pads.

In the next chapter fabrication of this solution is explained in details.

4.2 Embedded Graphene Photodetectors

This solution was implemented by placing the graphene inside the slot region of single slot waveguide. In Fig. 4.3 the idea is schematically presented. The guided mode for a single slot waveguide was simulated using the mode analysis calculations in COMSOL Multiphysics. In order to present the idea the graphene layer and the metal contacts are shown. Generated electron-hole pairs at the slot region are separated with the electric field in the graphene. The motivation with this design is to enhance the graphene-mode interactions and realize devices with less footprint [113, 114].

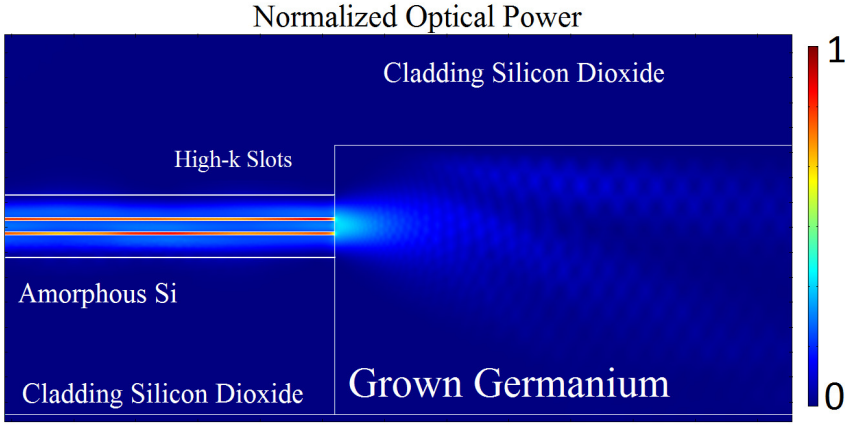

Figure 4.2: TM mode propagation simulation for a double slot high-k slot waveguide and the integrated germanium mesa [112].

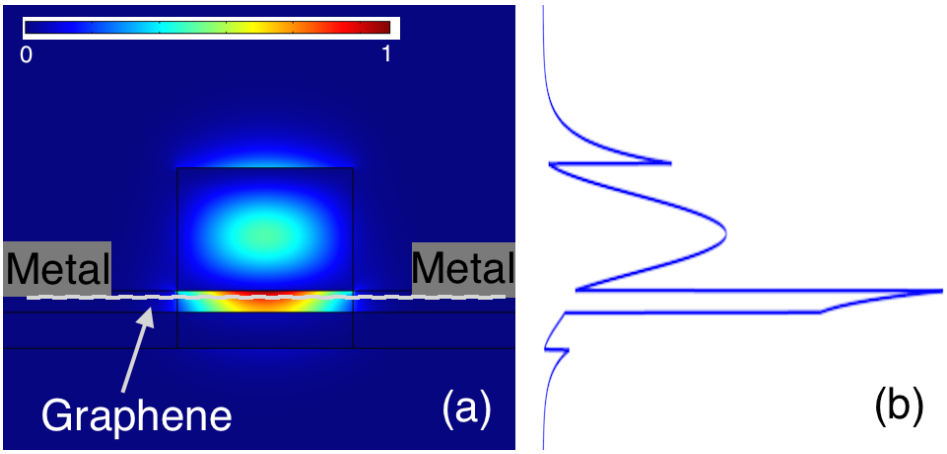

Figure 4.3: TM simulations for the guided mode in an asymmetrical single Al_2O_3 slot waveguide. (a) the optical field ($|E|^2$) distribution in the slot waveguide and the photodetector placement inside the waveguide. (b) the optical field in a vertical cut line placed at the middle of the waveguide.

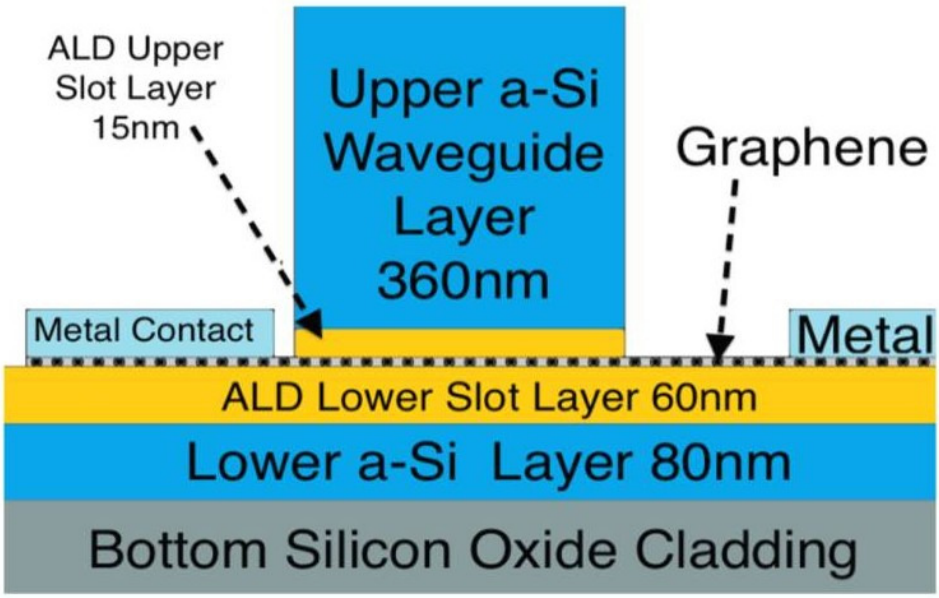

Figure 4.4: The waveguide material stack and the geometrical design. Only the upper amorphous silicon is pattered. The lower amorphous silicon and Al_2O_3 layer were left untouched. Reproduced from paper VI.

Grating Couplers and Waveguides

The grating couplers used for this integrated solution uses the partially etched grating coupler. The slot layer is a good etch stop and the top amorphous silicon layer is etched to make the waveguides and the grating couplers. The waveguide material stack is shown in Fig. 4.4. Fabrication of this device is enabled by thin film deposition equipment to implement the passive devices and to embed the graphene layer.

Benefits of an ALD High-k Slot Layer

Embedding the graphene layer in the ALD Al_2O_3 slot region serves two purposes. The slot region has the highest mode density in the waveguide. Considering the thickness of a graphene layer this can enhance the light-graphene interaction. Another benefit with the ALD Al_2O_3 layer as the embedding material is to protect the graphene layer. Graphene can be easily etched and damaged by any dry etching process. While the upper amorphous silicon layer is being etched the Al_2O_3 layer on top of the graphene protects the graphene. Al_2O_3 is hard to dry etch and it is reliable etch stop.

Chapter 5

Fabrication Process

In this chapter the grating coupler, germanium photodiode, and graphene detector fabrication process will be explained in details.

5.1 Fully Etched Waveguides

The waveguide/coupler stack was deposited using deposition equipment. The thickness of these layers were measured using ellipsometry. The fully etched process ensures the etching of the waveguide/coupler stack to the bottom oxide cladding layer [115]. The fabrication process has two phases. In the first phase the amorphous silicon layers and slot high-k films were deposited. After patterning the second phase starts where the deposited layer are etched. Finally the structures are covered by a top cladding layer.

Waveguide Stack Deposition

The waveguide is deposited on a bulk silicon wafer. The bottom cladding layer is a rather thick dielectric layer to ensure the mode confinement in the waveguide. A high refractive index contrast results in a more compact mode profile, which is favorable. The material with the lowest refractive index known to the CMOS technology is SiO_2. A 1.2 μm thick SiO_2 layer was thermally grown on the bulk silicon wafer. This process was done at 1100 ℃. In the BEOL of the CMOS technology this can be implemented by depositing a micron scale thick SiO_2 layer by means of PECVD [40]. This is also analogous to the traditional passivation technique to isolate the transistors in a chip. In the CMOS framework, a CMP step can provide a planar surface for the photonics devices. With the CMP step any losses in the waveguides due to sharp bends and roughnesses will be avoided.

The waveguide core is deposited through multiple steps. These steps are depicted in Fig. 5.1 for the double slot waveguide structure. The first layer to deposit is a-Si. In this work LPCVD was used. The benefit of this deposition method is

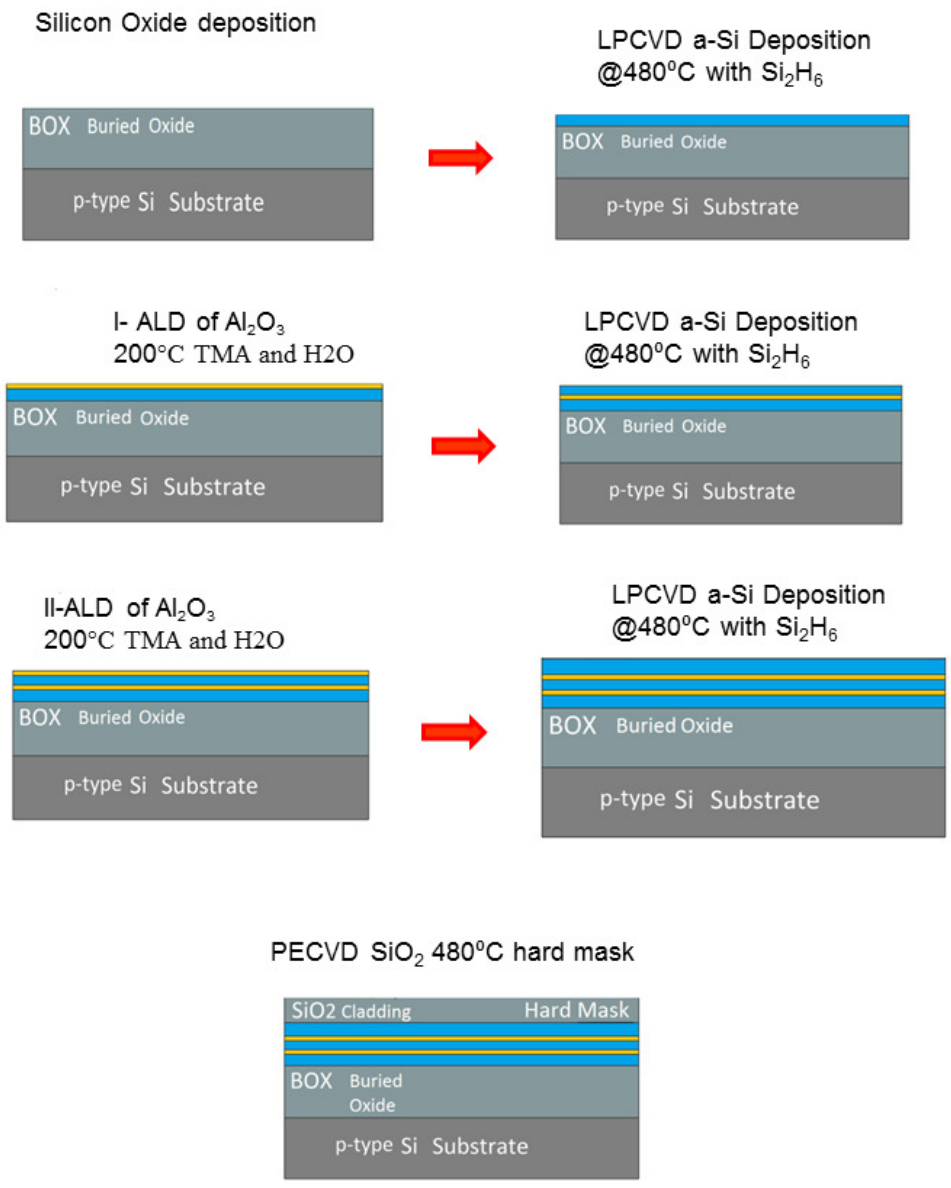

Figure 5.1: Waveguide material stack deposition steps.

a high mechanical stability of the layers. A well known process for deposition of a-Si is to deposit silicon using the silane (SiH_4) gas at 550 ℃. The drawback with this method is formation of random micro-grain islands in the film. These islands are formed due to the thermal budget while depositing silicon. The density and the number of these grains are not as much as polysilicon. Nevertheless, the grains harm the performance of the waveguides by introducing scattering sites. Formation of unwanted scattering sites can be avoided by reducing the deposition temperature. The silane gas is not suitable for the deposition of a-Si below 550 ℃. In an LPCVD furnace the silane molecules will not crack in a temperature below 550 ℃. Instead disilane (Si_2H_6) gas can be used for lower temperature deposition. Formation of mentioned islands was stopped by depositing the silicon layer at 480 ℃.

It is also possible to deposit the a-Si layers with PECVD. The mechanical stability of the layer deposited using PECVD is not as high as LPCVD. But the PECVD a-Si layers have higher hydrogen content. This high hydrogen content in a-Si results in a low optical loss in the waveguides [39]. The performance of the waveguides and the hydrogen content of the films is discussed more in 6.2.

For the presented double slot waveguides the high-k layers were deposited using ALD. The temperature at which the high-k layer is deposited is harmless to the deposited a-Si layer. This ensures that the optical properties of the a-Si layer is intact through out the waveguide deposition step. In a single slot waveguide structure after the deposition of the slot layer a final a-Si layer was deposited to complete the waveguide core stack. In a double slot structure two more deposition steps are required to deposit an extra slot layer and a-Si layer.

After the waveguide core deposition, the waveguide top cladding needs to be deposited. This cladding layer affects the coupler performance as well [101]. This is done by depositing SiO_2 on top of the core stack. This top cladding is also the hardmask for the etching of the waveguide. For the case of the double slot waveguides a 400 nm top SiO_2 layer was deposited.

The deposited material stack is shown in Fig. 5.2. The layers are color coded according to the schematics in Fig. 5.1. The resulted cross section SEM micrograph shows a smooth layer profile for all of the deposited materials. This smooth layer profile ensures a minimal scattering at the slot boundaries. Scattering in a slot waveguide is more sensitive at the slot boundaries. This is due to a high mode confinement in the slot region. Both of the Al_2O_3 layers had a thickness of 25 nm. The bottom and top a-Si layer were 180 nm. The middle a-Si layer was 90 nm.

Patterning

The SiO_2 hardmask was patterned using an XLS i-line stepper. The wafers were spin coated using a positive SPR700 resist. The SiO_2 hardmask was dry etched after the resist patterning and baking. The photoresist was removed after the dry etching of the hardmask. The waveguide and grating structures were etched using the hardmask.

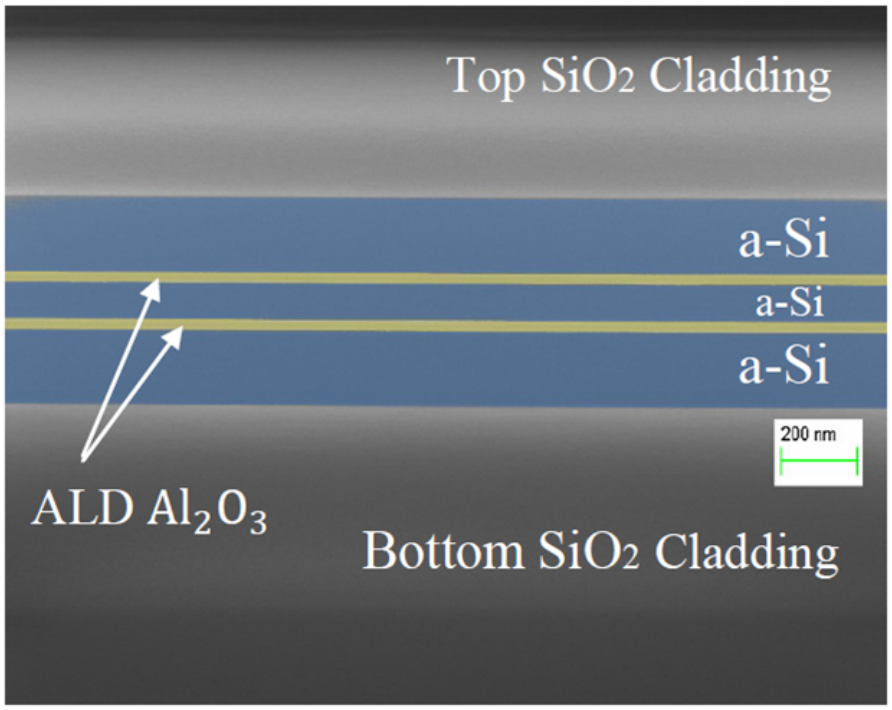

Figure 5.2: The double slot waveguide material stack. A pair of 25 nm Al_2O_3 layers interposed by three a-Si layers. The layer quality shows a suitable quality for photonic applications. Figure reproduced from paper III in this thesis.

The patterned grating coupler is shown in the SEM micro-graph of fig. 5.3. In addition to grating couplers, waveguides and ring resonator patterns where tested for this lithography equipment. A 10 second ashing of the resist can reduce the line edge roughness [116]. Waveguides with a width of 500 nm were resolved. Ring resonators with a waveguide width of 500 nm and a proximity of 450 nm were resolved. The ring resonators had a radius of 20, 30 and 50 μ m. A ring resonator with a radius of 20 μ m in shown in fig. 5.4. This shows a good feature tolerance for bent structures that enables the patterning of structures such as mach-zender interferometers. fig. 5.5 shows a zoomed view of the ring resonator and the bus waveguide. At critical dimensions a wrong exposure dose can lead to deformations in the patterns. As illustrated in fig. 5.5 this is well avoided . Neither the curve of the ring nor the straight bus waveguides are deformed. Targeting proximities below 450 nm will require a sophisticated optimization and difficult to achieve.

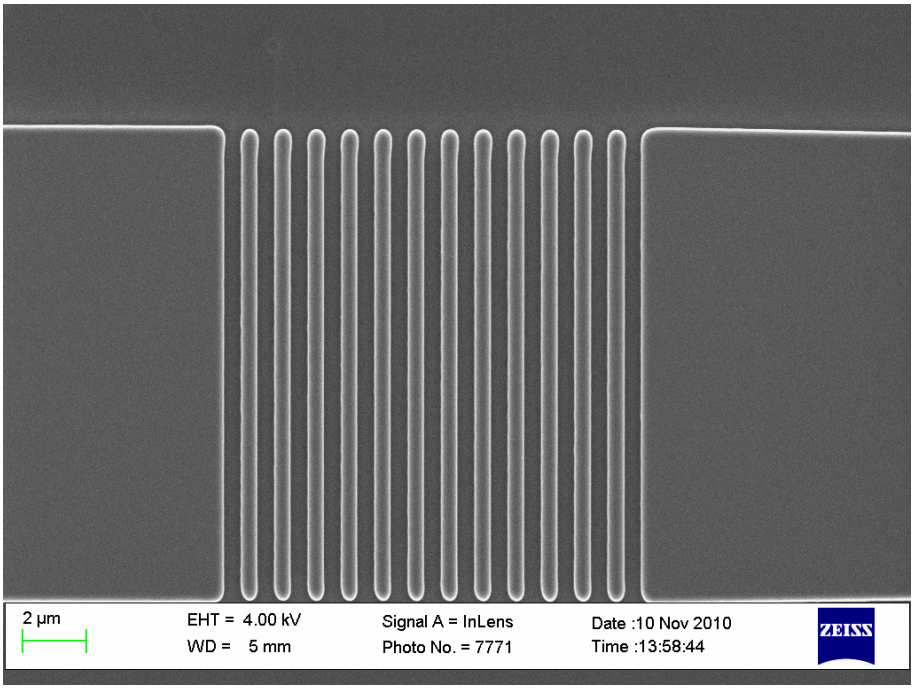

Figure 5.3: Grating coupler structure successfully patterned by the XLS stepper.

Grating and Waveguide Etching

As it was mentioned earlier, the waveguides and the grating couplers were produced with the same mask. This single mask process reduces the complexities of the device fabrication. Rotational and translational mis-alignments are avoided . This ensures a better coupling between the waveguide and the grating. All of the layers in the material stack were dry etched using the SiO_2 hardmask. All of the etching steps where done in an Applied Materials - Precision 5000 chain tool. The etching steps were done in various chambers of the tool. After each etch step the wafer was transfered to another chamber using a robot arm. In this process the wafers stay in the load lock pressure and are not taken out of the equipment during the material stack etching.

For a single slot fully etched structure the material stack was etched in 3 steps. First the top a-Si layer was dry etched using an $HBr/Cl_2/He/O_2$ chemistry. The single slot grating coupler characterized in 6.2 had an SiO_2 slot layer which results in a good end point detection while dry etching of the silicon layer. The slot layer was etched using a $CHF_3/CF_4/Ar$ chemistry [115]. This etching step also results in a suitable endpoint because the underlying layer is an a-Si layer. The final layer to etch is another a-Si which is well stopped at the underlying SiO_2 cladding layer.

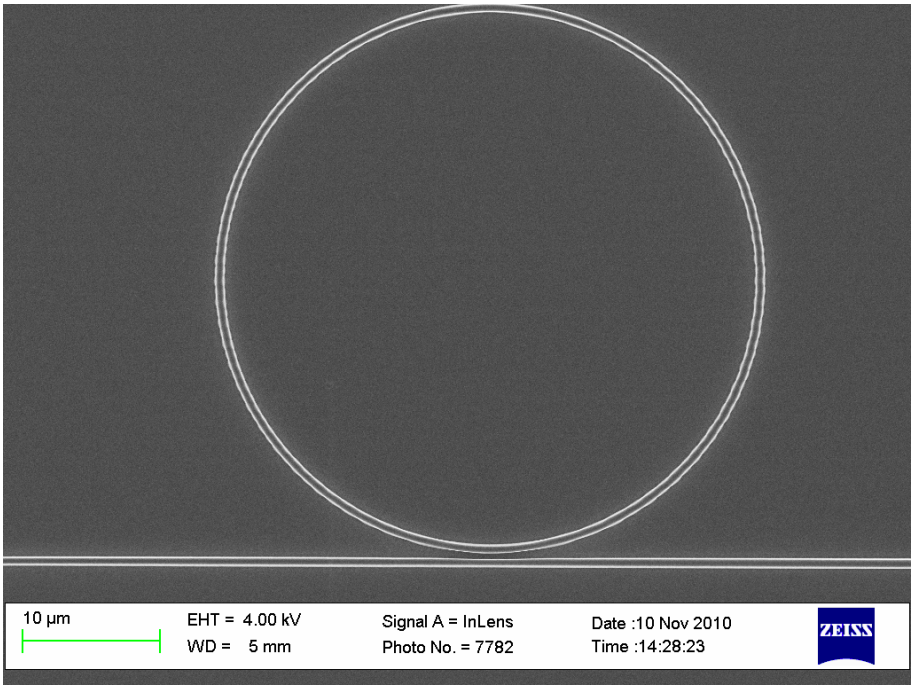

Figure 5.4: Ring resonator structure patterned by the XLS stepper.

Because of a good etch selectivity between SiO_2 and a-Si a little fraction of the top hardmask was consumed. The main consumption of the hardmask was during the etching of the SiO_2 slot layer and the breakthrough step of the a-Si dry etch.

In a double slot fully etched structure the material stack was etched in 5 steps. This process flow is schematically shown in Fig. 5.6. The a-Si layers were dry etched as described above. The slot layers in the grating couplers and waveguides characterized in 6.2 and 6.2 were ALD Al_2O_3. The etching of a-Si layers deposited on Al_2O_3 layers resulted in a reliable endpoint detection. As it will be explained further Al_2O_3 is hard to dry etch using the chemistries and the etching chambers available to this work. This causes a very high selectivity while etching of the a-Si layers.

In order to etch the Al_2O_3 layer a $BCl_3/Cl_2/N_2$ chemistry [117, 118] was used in the metal etch chamber of the tool. This process is similar to the etching of the native oxide in dry etching of aluminum. The ALD Al_2O_3 etch needed optimization to be suitable for photonics applications. A high RF power were required in the chamber to increase the etch rate. But this high power of the etching process were harmful to the waveguide and the grating coupler pattern. After a high power etch line-edge roughnesses were introduced to the waveguides. This roughness lowers

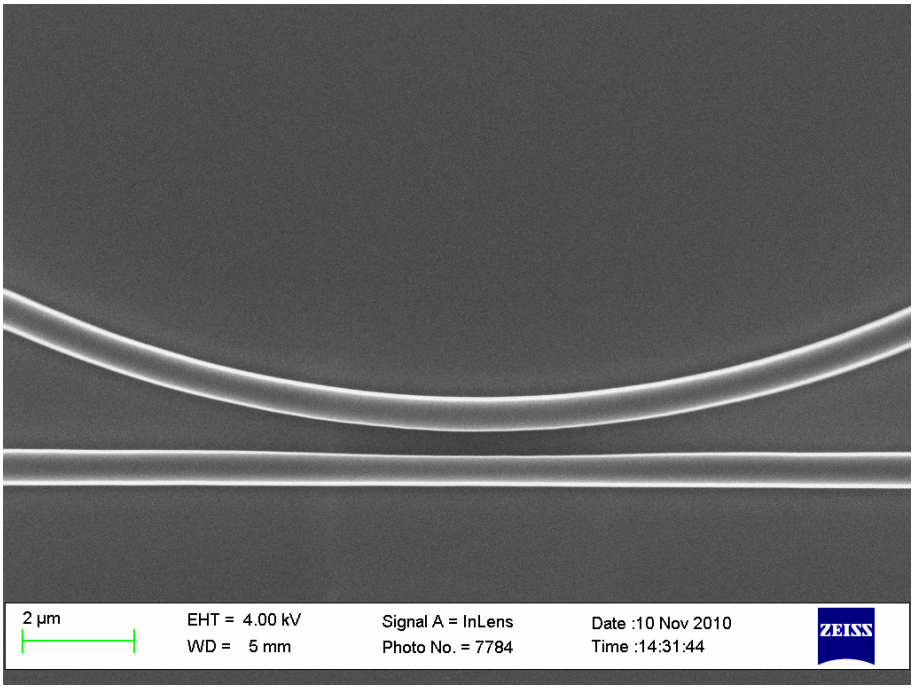

Figure 5.5: Ring resonator at the proximity of the bus waveguide.

the transmission in the waveguide and the coupling in the gratings. In order to avoid this, the RF power was kept at 100 W.

Etching of the Al_2O_3 layers cannot benefit from the endpoint detection [119]. A-Si has a higher etch rate than Al_2O_3 layers. In order to achieve a robust process the slot layers where etched by time. In order to calculate the etch rate of the high-k materials spectral ellipsometry was used. Nevertheless, robustness of the waveguide and grating coupler fabrication is not affected. The last etched layer in the material stack was a silicon layer, and the etching of the silicon was stopped at the bottom SiO_2 cladding layer. For the double slot waveguides a 400 nm hardmask layer was used to ensure that the waveguide structure is protected during all the mentioned etch steps.

Top Cladding Deposition

The hardmask has a double purpose for the waveguides. It is also the top cladding for the waveguides. As mentioned above, this hard mask layer is thinned while the etching of the structures. In addition, the grating coupler groves can be filled with a cladding material. The thickness of this layer effects the coupling efficiency and the peak wavelength. With the right choice of material and thickness this layer

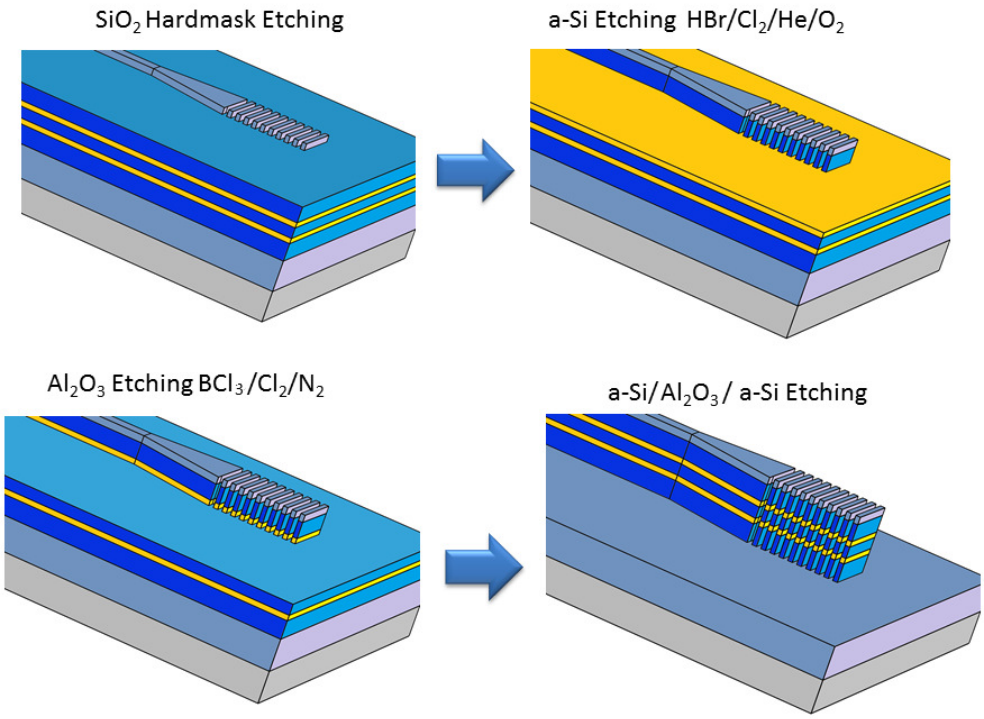

Figure 5.6: Process flow of the high-k double slot waveguides. The diagram shows the etching phase of the process starting from the patterned hardmask and ending to the bottom cladding layer

can be engineered to become an anti-reflective coating [120]. The characterized single slot couplers in 6.2 have a 500 nm SiO_2 cladding layer. The high-k double slot couplers in 6.2 were characterized without a cladding layer and with a 500 nm SiO_2 cladding layer. These layers were deposited using PECVD at 300 ℃.

In a multi-layered optical interconnect architecture this top SiO_2 layer is the bottom cladding layer for the next interconnect level. Due to the patterned features the deposited SiO_2 cladding layer is not planar. In order to make this layer suitable as a bottom cladding a CMP step is required to make a planar profile.

The back reflections are higher in fully etched couplers. Using a dielectric with a higher refractive index can enhance the coupling efficiency by reducing the back reflections. The drawback to using a higher refractive index cladding layer is a larger guided mode size in the waveguides. This will increase the waveguide footprint (width) in the chip.

5.2 Partially Etched Waveguides

In the Partially etched grating couplers the waveguide core is redesigned. The bottom and top a-Si layers have different thicknesses. This tunes the position of the slot layer in the waveguide. The position of the slot layer in this design determines the suitable grating period. The similarity of this design to the SOI waveguide design is that the waveguide is etched to a certain depth. In this design the etch depth is determined by the position of the slot layer. Since the slot layer is very hard to dry etch, it acts as a reliable etch stop. The top a-Si layer is the only layer that is etched and the rest of the layers are left intact. In comparison to SOI waveguide technology this technology benefits from an endpoint detection feature and a single mask design.

In the material stack deposition phase three layers were deposited. The first a-Si layer was deposited using LPCVD at 450 ℃. This layer in the design had a thickness of 80 nm. The thickness of the first a-Si layer determines the position of the slot layer. The grating coupler operation is sensitive to the position of the slot layer. Using the method mentioned in 5.1 the thickness of all the three layers were accurately measured by means of ellipsometry. The Al_2O_3 slot layer was deposited using ALD. This layer had a thickness of 60 nm. The second a-Si layer was deposited using LPCVD and the thickness of the layer was 360 nm.

The etching phase of the process for the grating couplers and the waveguides were started by etching of the SiO_2 hardmask. After this step the photoresist mask was removed and the top a-Si layer was dry etched. The process was stopped and the polysilicon dry etching endpoint algorithm was suitable for the etch-stop detection.

5.3 Germanium Photodetectors

Pre-Growth Etching

After the waveguide etching, the bottom cladding SiO_2 layer was etched to reach the silicon substrate. This SiO_2 layer has a thickness of 1.2 μm. This process was done in two steps. A dry etching was used to etch the SiO_2 layer almost fully. The etch rate of SiO_2 in the P5000 dry etcher is 150 nm/min but this applies to very large openings. In case of openings for the detectors this etch rate is lowered to 90 nm/min. This is due to the pattern dependency of the dry etch process.

About 50 nm of the layer was left in the openings to be wet etched. This final wet etching step is required to maintain the surface quality to the silicon substrate. Dry etching causes roughnesses to the silicon surface. This roughness degrades the growth quality since the silicon surface is the growth seed. The remaining SiO_2 was etched using buffered hydrofluoric acid which is highly selective towards the resist mask. After this step the wafer were ready for selective germanium growth. fig. 5.7 shows the etched opening through the SiO_2 hardmask at the top of the waveguide stack, waveguide stack and the thick bottom SiO_2,

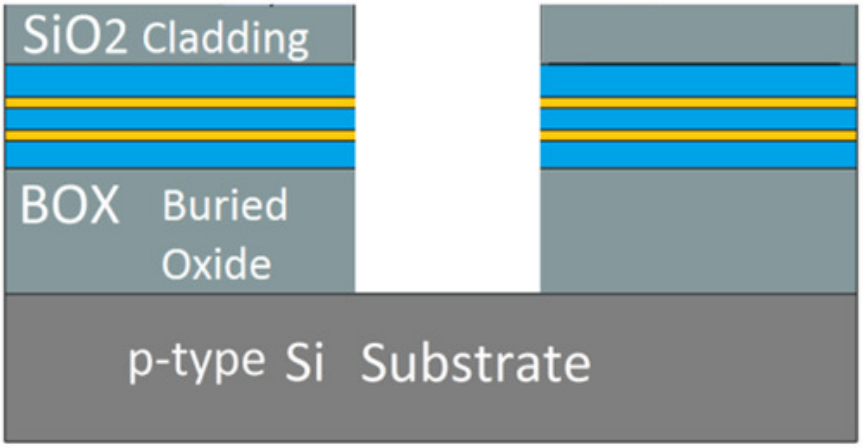

Figure 5.7: Trenched waveguide stack and bottom SiO_2 layer. The SiO_2 layer is deep etched to reach the silicon substrate. The substrate would be used as the growth seed.

Selective Germanium Growth

The selective germanium growth process was developed. Germanium mesas were grown using an RPCVD Epsilon 2000 equipment. Germanium PIN mesas were grown using digermane (Ge_2H_6) gas. The germanium in the n-type region was in-situ doped with the phosphine gas (PH_3). The p-type region was in-situ doped using a diborane precursor (H_6B_2). The selectivity in the growth process was maintained with hydrogen chloride (HCl) gas. This gas is an etchant for germanium. The deposited germanium on the SiO_2 layers were etched and the island formation was prevented on unwanted surfaces. Hydrogen gas was used as the carrier gas for the precursors.

Baking Process and The Effects on Waveguiding Properties

Although that the wafers were cleaned in a hydrofluoric acid bath, at the time of growth, some native SiO_2 might be present that the surface. This layer on the silicon substrate interfere the growth. In order to remove this layer a baking step was used. The baking process was done at 950 ℃. In case of the fabricated chips at the time of baking, the morphology of the amorphous silicon layers will be changed. Due to high thermal budget and temperature the amorphous silicon films will turn

into polysilicon layers.

Polysilicon layers suffer from high optical absorption. This is due to a high concentration of dangling bonds at the grain boundaries [31,32]. In addition to this optical absorption, polysilicon layers are rough. The roughnesses in the waveguide degrade the transmission in the waveguides. This is due to scattering of the light at the waveguide boundaries and in specific at the slot boundaries. Since the mode concentration is very high in the slot region, the attenuation is sensitive to the roughnesses at the slot region of the waveguide.

Waveguides fabricated and integrated using this method experience some degradations in the transmission performance. One solution is to have the waveguide material stack deposited after the fabrication of the diode.

Two Step Growth Process

The germanium growth was done in two steps. First step was the growth of germanium buffer layer. Germanium has a lattice mismatch of 4 % with silicon. The growth of the germanium directly on silicon will create a high density of defects in the germanium. The goal for the growth was to minimize the defect density in the germanium to have a good device performance.

In order to overcome this problem, a germanium buffer layer was grown at 400 ℃. The grown germanium has a high density of defects.The layer was grown for 6 minutes and the thickness of the layer was 40 nm. Due to the low temperature, mobility of adsorbed germanium atoms and the hydrogen surfactant action was limited. This limitation will cause relaxation from the very beginning of the growth. The benefit with this effect is that two-dimensional to three dimensional growth mode can be avoided [121]. Due to this, the germanium buffer had a smooth surface. As a result, The second step germanium grown on this layer had a higher crystalline quality. It is expected that with thicker layers the quality of the layers are further improved.

The second step germanium growth was done at 670 ℃ for 17 minutes. In order to align the intrinsic region of the detector in front of the waveguide the growth time for p-type germanium should be tuned. The growth rate had a pattern dependency. A higher growth rate was seen in the smaller areas. The highest growth rate was measured as 1.9 nm/sec. A grown PIN germanium mesa is shown in fig. 5.8.

As it was mentioned before the trenches were etched using a resist mask. Any remaining resist on the SiO_2 can jeopardize the selectivity of the growth. This is because of a high germanium growth rate at the surface of the mask. The resist mask was removed using a mix of sulfuric acid and hydrogen peroxide. This wet process was done 30 minutes at 120 ℃.

Selective Growth Uniformity Structures

In addition to the openings for the photodetectors other openings are required in the mask set. This is because of the dependency of the selectivity on distribution

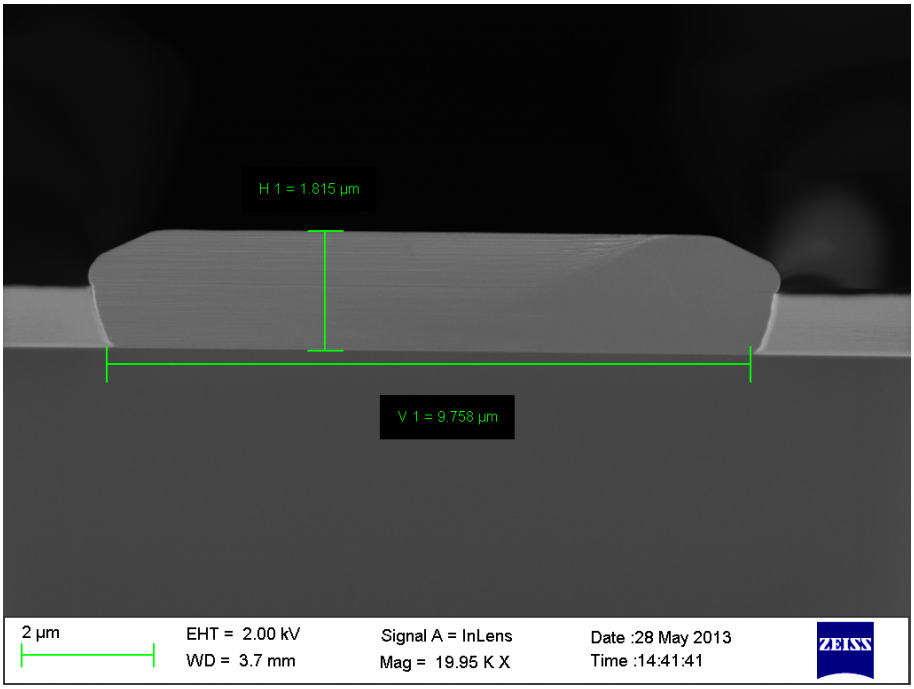

Figure 5.8: Selectively grown germanium PIN mesa in a SiO_2 trench.

of the openings [122]. An area with less openings has a worse growth selectivity. In order to increase the selectivity, some uniformity structures were added to the mask design. This is crucial for the areas that contain the waveguides and the grating couplers. The formed germanium islands introduce roughnesses to the waveguides and degrade the transmission. These islands can also form on top of the grating coupler surface degrading the coupling efficiency. These uniformity structures in a fabricated test chip are shown in fig. 5.9.

Wet Etching of Germanium

Germanium can be wet etched using H_2O_2 or the mixed solution of H_2SO_4 and H_2O_2 (piranha) [123]. If piranha is used the resist mask will be attacked by the solution and therefore, it cannot be used as the etching mask. In case of hydrogen peroxide the resist mask can be used. In order to have a more controlled etch rate the hydrogen peroxide was diluted. Using a 20:1 diluted H_2O_2 the germanium etch rate was 50 nm/min at room temperature. The wet etching process has an isotropic profile. This causes germanium undercut beneath the resist mask. The dry etching has an isotropic profile which makes it more favorable for the photodetector fabrication.

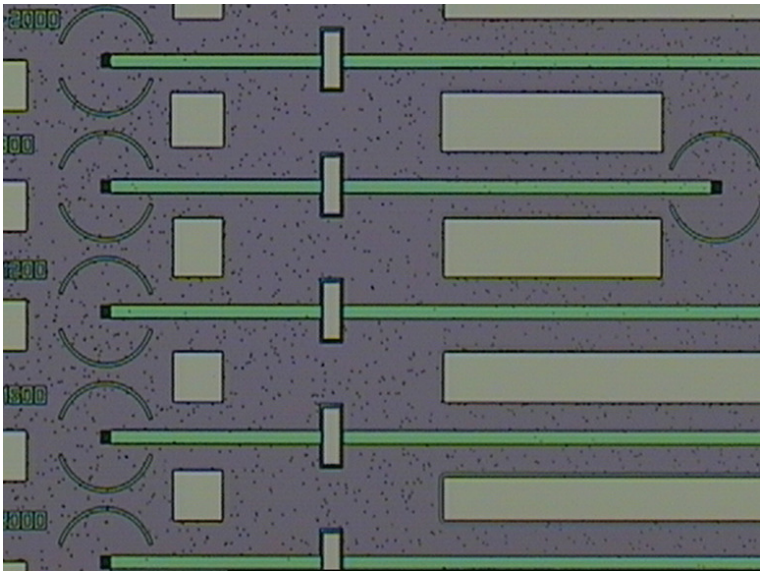

Figure 5.9: The selectively grown PIN germanium mesas and the dummy openings neighboring the high-k double slot waveguides and the grating couplers.

Dry Etching of Germanium

A group IV type of dry etching has a suitable chemistry for the germanium etch process. Silicon dry etching chemistry used in the P5000 equipment is HBr/Cl2/He/O_2. The etch rate for silicon using this chemistry is 150 nm/min. Using the exact same recipe the etch rate for germanium was 650 nm/min. This etch rate was measured for the photodetector openings which in principle should have a much lower etch rate than large openings. This showed that germanium compared to silicon, is easier to etch with this chemistry.

Contact Metalization

A metal stack was sputtered to form the contacts to germanium. The bottom layer in the stack was titanium tungsten (TiW). The benefit with using this metal in contact with germanium is to minimize formation of Schottky barrier between germanium and the metal. The stack was finished with a 500 nm aluminum layer to provide with good conductivity.

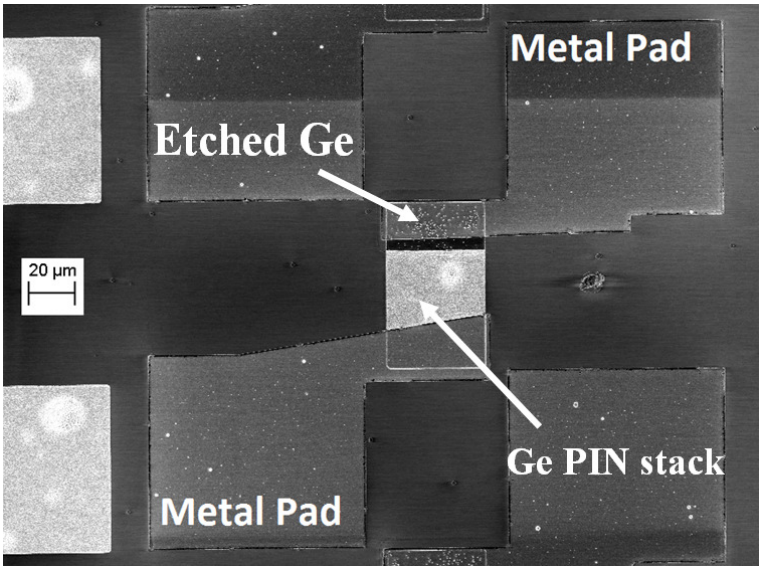

Figure 5.10: Fabricated selective PIN germanium diode. The etched germanium and metalized contact pads are marked.

5.4 Embedded Graphene Photodetectors

Deposition of the Waveguide Stack

The material deposition process is explained in fig. 5.11. The bottom SiO_2 cladding layer was thermally grown on a bulk silicon wafer at 1100 ℃. The first amorphous silicon layer was deposited using LPCVD and disilane gas at 450 ℃. On top of the first amorphous silicon layer a 60 nm Al_2O_3 was deposited using ALD.

CVD Graphene Transfer

Graphene deposited on copper was transferred to the 4 inch wafers. Poly(methyl metacrylate) (PMMA) resist was used to transfer the graphene. The resist was deposited on top of the graphene and the bottom copper layer was wet etched in $FeCl_3$ solution [124]. The graphene with the resist on top was floating on water. By putting the wafer in the water and lifting the graphene layer was placed on the wafer. This method enables a wafer scale fabrication process.

Graphene Etch

The graphene was patterned using the i-line stepper tool and a photo-resist mask. The graphene was then etched with the Al_2O_3 dry etching chemistry. This etch-

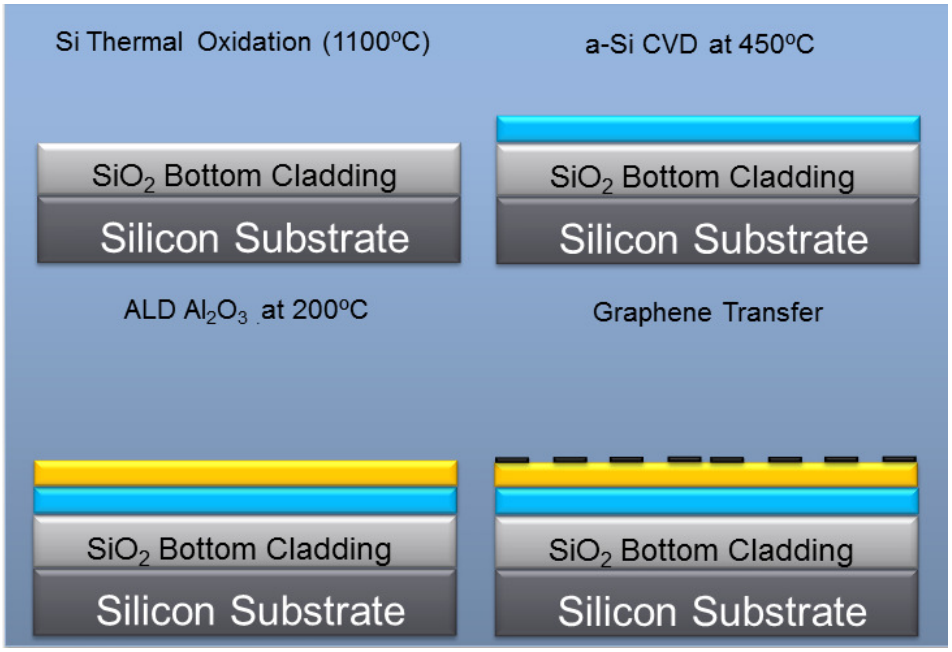

Figure 5.11: Steps of the waveguide deposition process. a) thermal growth of the bottom SiO_2 cladding b) deposition of the bottom a-Si layer c) deposition of the bottom slot layer d) and the graphene transfer

ing chemistry was chosen to make sure that the graphene is etched with minimal residues on the rest of the wafer. In addition to the graphene, the underlying Al_2O_3 was etched. In order to have a total slot layer of 60 nm, the Al_2O_3 was etched for 20 nm. The rest of the fabrication process is illustrated in fig. 5.12.

Metal Contact Liftoff and the Top Al_2O_3 Deposition

Using the liftoff method, the metal contacts were deposited on the graphene layer. A titanium/gold stack was deposited using e-beam evaporation. After the contact formation, a 3 nm layer of aluminum was deposited on the graphene layer. This aluminum layer was oxidized in air to form a thin layer of Al_2O_3. The wafer was then transfered to the ALD to deposit a 20 nm Al_2O_3.

Grating Coupler and Waveguide Layer

A thick layer of a-Si was deposited on top of the stack using LPCVD. This layer had a thickness of 360 nm. After the deposition, the layer was patterned for the grating couplers and the waveguides. The top a-Si layer was dry etched and stopped at the

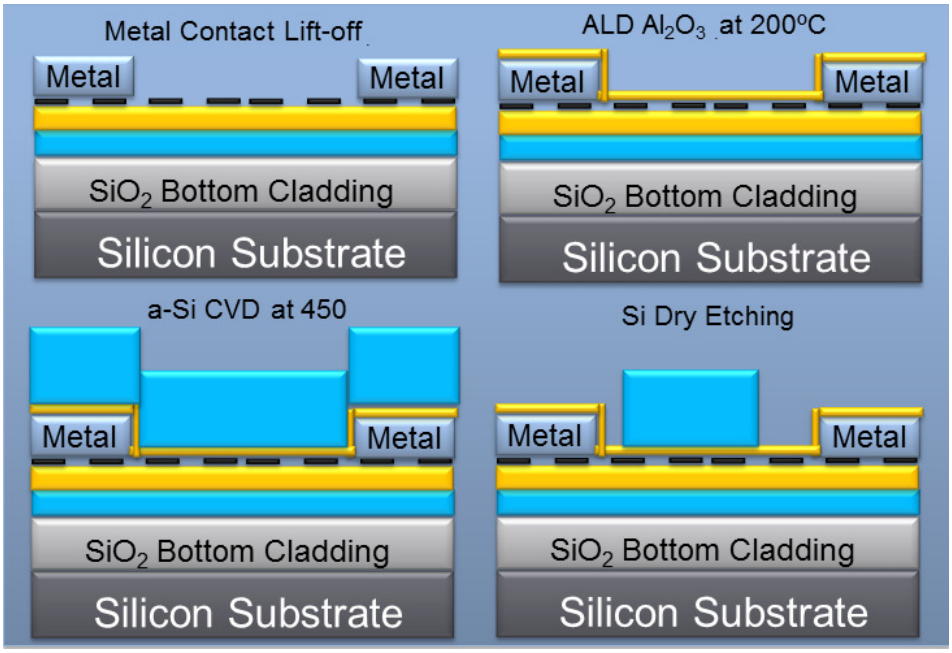

Figure 5.12: The four final steps of the fabrication process for the embedded graphene photodetectors. a) metal contact lift off b) deposition of the top Al_2O_3 layer. c) deposition of the top a-Si layer and d) patterning and dry etching of the grating couplers and the waveguides.

Al_2O_3 layer using the end point detection in the etching chamber. The fabricated integrated photodetector is shown in the fig. 5.13 [103].

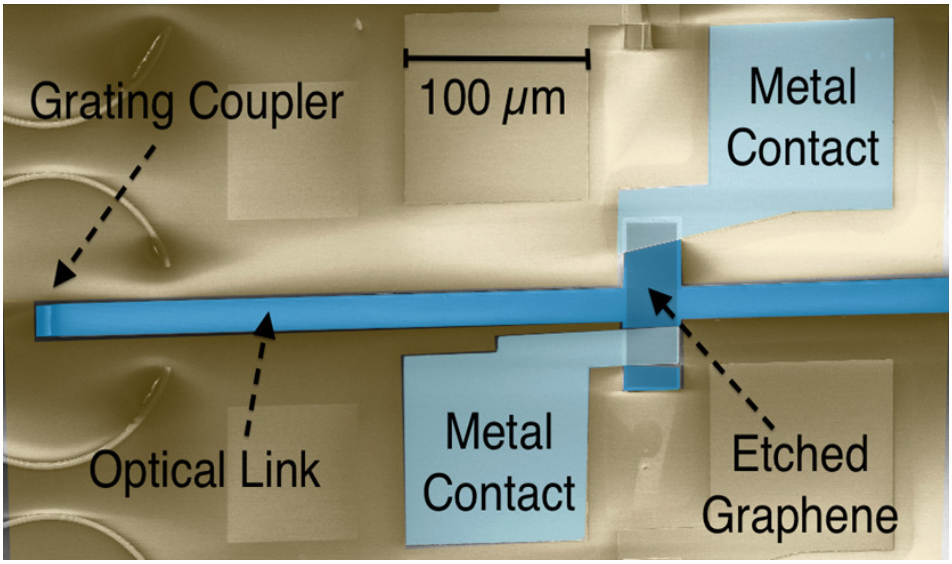

Figure 5.13: SEM micrograph of the fabricated chip including grating couplers, single high-k ALD slot waveguides and graphene photodetectors. Reproduced from paper VI in the thesis.

Chapter 6

Results

This chapter will report the thin film characterizations and the device performance studies. The thin film characterization was done using the spectroscopic ellipsometry to measure the real and the imaginary part of the refractive index of the high-k thin films. The chapter will continue with reporting of the grating coupler efficiency and waveguide transmission. The photodetector characterization results will be presented in the ending section.

6.1 Slot Material Characterization

The refractive index of the high-k films were measured using spectral ellipsometry. This method has a high precision for both the real and the imaginary part of the refractive index. Hafnium oxide films were deposited at 350℃ using Bis (methylcylpentadienyl) methoxymethylhafnium($HfDO_4$) $Hf[C_5H_4(CH_2)]2(OCH_2)(CH_3)$ and DI water precursors. Films were deposited with 300, 600 and 1000 cycles. The thicknesses were measured 18.2 nm, 27.1 nm, and 53.9 nm, respectively. The refractive index at 1.55 μm wavelength was measured 1.95. The 'k' value was zero at this wavelength representing zero absorption in the layer. Fig. 6.1(a) shows the measured n and k for hafnium oxide compared to the values reported in the literature [110]. Grating periods shown in Fig. 3.3 are calculated using the reference refractive index values. Grating coupler simulations were redone using the measured refractive index of hafnium oxide. Since the slot waveguide optical mode is sensitive to the slot material properties, the coupler design was different. Fig. 6.1 (b) shows the grating coupler periods suitable for a coupling peak at 1.55 μm, for the reference and measured refractive index values.

Aluminum oxide layers were deposited at 200℃ using TMA(Trimethylaluminum) and DI water precursors. A Cauchy absorbent dispersion model was used. Fig. 6.2 (a) summarizes the refractive index of Al_2O_3, reported in the literature and the optical numbers calculated using the developed technique. The measured refractive index is lower than the literature values [108]. This is due to a lower film density.

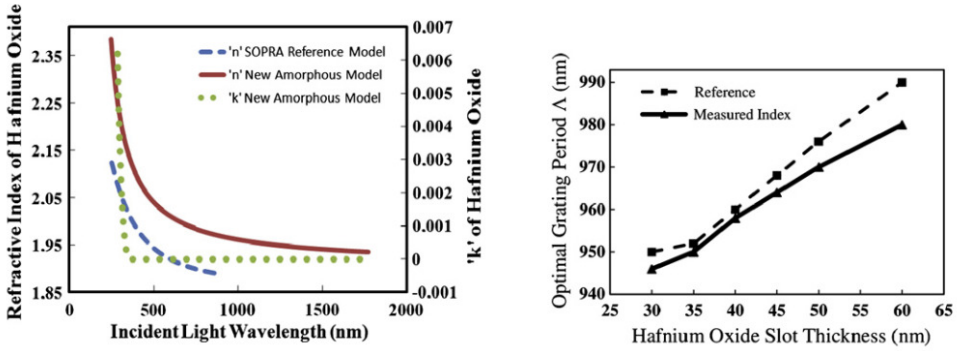

Figure 6.1: (a) The measurement results for n,k of hafnium oxide and the reported refractive index from [110]. (b) Suitable grating coupler periods based on the measured refractive index and the previously reported values. Figures reproduced from [115].

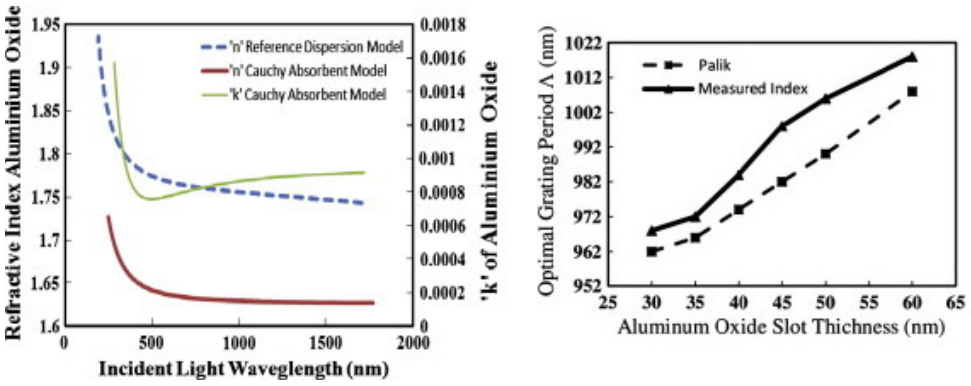

Figure 6.2: (a) Measured n,k of aluminum oxide and the refractive index in the literature [108]. (b) Suitable grating coupler periods based on the measured refractive index and the previously reported refractive index at 1550 nm. Reproduced from paper II.

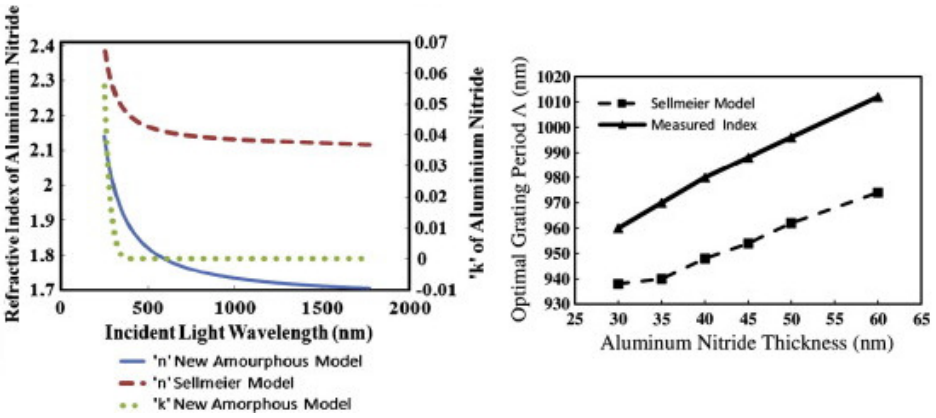

Figure 6.3: (a) The measured n,k of aluminum nitride and the refractive index spectrum from the Sellmeier model [109]. (b) Suitable grating coupler periods based on the measured refractive index and the previously reported values [115].

At 1550 nm the refractive index of Al_2O_3 is reported 1.75. The measured refractive index of ALD Al_2O_3 was 1.62 at 1550 nm. For the same waveguide dimensions the measured numbers promise a larger field enhancement in the slot layer. This lowers the effective refractive index of the slot waveguides. The grating couplers were simulated using the measured refractive index. Fig. 6.2 (b) shows the suitable grating coupler periods for various slot thicknesses. Compared to grating couplers designed with the literature value, smaller grating coupler periods are required to have a peak coupling efficiency at 1550 nm.

Aluminum nitride (AlN) layers were deposited at 350℃ using TMA and ammonia gas (NH_3). Measured and reference [109] values for the refractive index and the 'k' are summarized in Fig. 6.3 (a). A 'new amorphous' dispersion model was used to fit the ellipsometric values. At 1550 nm the literature value for the refractive index is 2.15. The measured refractive index for the ALD AlN layers was dramatically lower. At 1550 nm, the deposited layers had a refractive index of 1.8. This will require larger grating periods to have a peak of coupling efficiency at 1.55 μm. Suitable grating periods simulated for various thicknesses are sown in Fig. 6.3 (b). AlN films had the highest deviation from the literature values. As a result the grating coupler design also had the largest deviation.

In the simulations based on the literature values, the effective refractive index is higher. This also indicates a higher mode confinement for the films developed in this work.

6.2 Couplers and Waveguides

Test chips were fabricated on 100 mm silicon wafers. These chips contained waveguides and grating couplers. Coupling efficiency of single slot and double slot fully etched structures will be presented. Performance of the double slot high-k waveguides will be further discussed. Finally, the performance of the partially etched grating couplers will be discussed.

Single Slot Couplers

The single SiO_2 slot grating couplers were characterized. For this fully etched structure the highest achieved coupling efficiency was 18.5%. The fabricated slot layer was 25 nm thick. With a 17° fiber tilt the peak efficiency was at 1540 nm wavelength. The grating period for this coupler was 980 nm. In Fig 6.4 the efficiency spectrum is shown. The ripples in the spectrum are caused by the back reflections at the grating couplers.

In the literature a practical coupling efficiency of 20% was reported for SOI single slot waveguides [107, 125]. The reported grating couplers where partially etched. In the couplers the slot was a silicon rich SiO_2 layer. This coupling efficiency was not optimized for the bottom SiO_2 cladding layer.

Another method that has been reported in the literature for light coupling into horizontal slot waveguides is the "nano-taper" solution. Coupling efficiencies up to 96% have been reported [126]. In addition to silicon waveguides this solution has been presented for slot waveguides [127]. This technique is similar to the butt coupling [93]. A polymer is used to cover a part of the waveguide. The waveguide is tapered to a very narrow width at both ends (about 80 nm). The optical mode in the waveguide radiates in the polymer. The mode cannot be guided in such a narrow structure and will gradually radiate from the waveguide region without being reflected at the sidewalls [128]. Despite the very high coupling efficiency the nano-tapers have drawbacks. The wafer needs to be diced. In addition to dicing, the polymer face needs polishing. This complicates the integration of the photonic circuits in a chip.

Sensitivity of the grating couplers were tested against the grating coupler period. Grating couplers with grating period of 1010 nm were characterized. In these measurements the fiber tilt angle was kept at 17°. Fig. 6.5 shows the efficiency spectrum for these grating couplers. In comparison with the spectrum fig. 6.4 the coupling peak was red shifted 20 nm. The ruling physics of this shift is explained in [92].

Double Slot High-k Couplers

Double slot ALD high-k waveguides were characterized. The efficiency spectrum of the double slot high-k grating couplers without a top cladding layer is depicted in fig. 6.6. The coupling efficiency spectrum of the grating couplers with an SiO_2

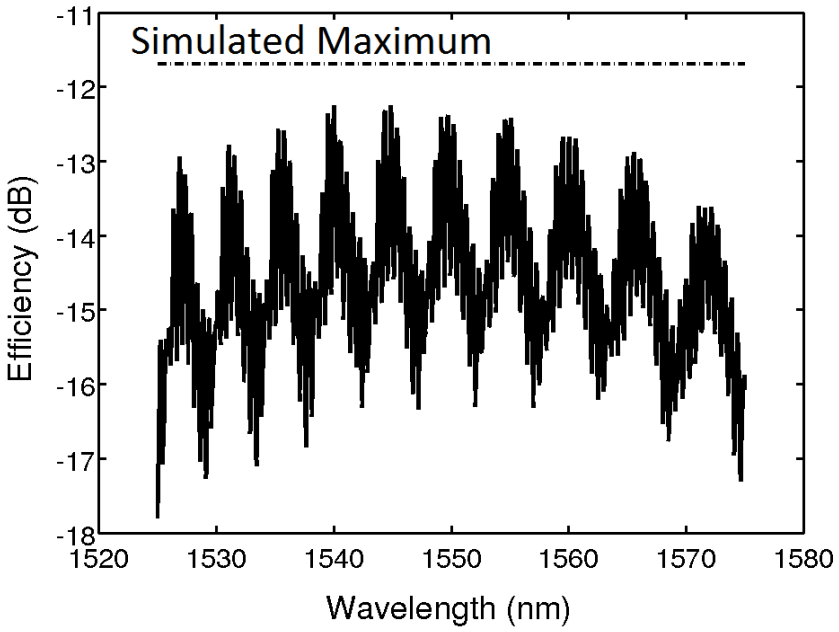

Figure 6.4: Efficiency of the fully etched single SiO_2 slot coupler. The theoretical and measured insertion loss of a single grating coupler is compared for a grating period of 980 nm. In paper II.

cladding layer is shown in fig.6.7. A significant shift to the efficiency spectrum was seen in the measurements. This is due to the change in the effective refractive index of the grating structure. A smaller grating period was required to have a peak coupling at 1.55 μm. The highest efficiency measured for these couplers were 22%. The cladded grating couplers had a 2.5 dB bandwidth of 48 nm and the uncladded couplers had a 2.5 dB bandwidth of 60 nm. Other solutions have been proposed by other works to improve the coupling efficiency of grating couplers. For a fully etched structure by mixing sub-wavelength features [129]. In this design the back reflections are highly suppressed. However, this solution requires a high resolution lithography and the coupler has low variation tolerance. Another technique to increase the coupling is to implement a miror at the bottom of the grating coupler [130]. A metallic layer can be deposited at the back of the grating couplers with a micro-machining technique [131].

Double Slot High-k Waveguides

The light transmission in the double slot waveguides were investigated. The average attenuation in the ALD Al_2O_3 double slot waveguides were 81 dB/cm. .This

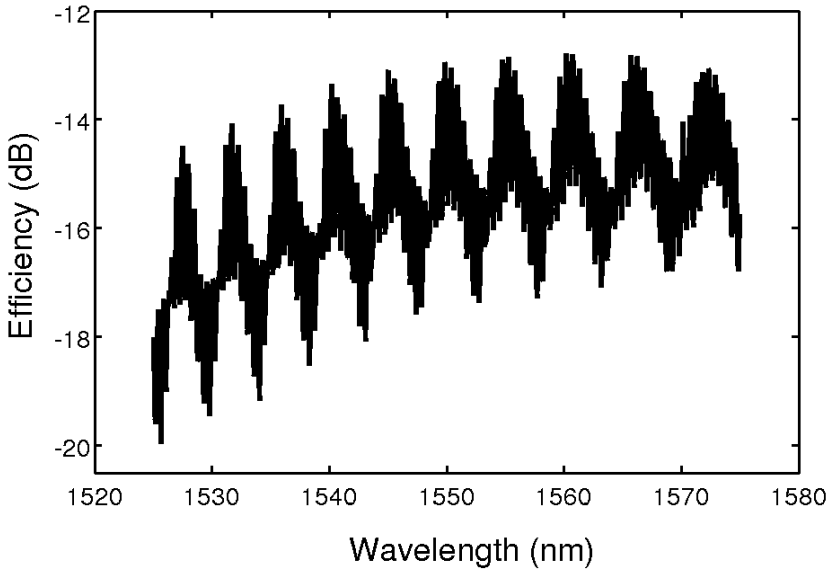

Figure 6.5: Efficiency of the fully etched single SiO_2 slot coupler efficiency with a grating period of 1010 nm (Paper II).

attenuation is mainly caused by the high absorption in the LPCVD a-Si. This high absorption is due to a high density of dangling bonds and deformations. Hydrogen atoms in the a-Si network can terminate the dangling bonds and the deformation. LPCVD a-Si has a very low hydrogen content. The high optical loss in fabricated waveguides is originated from low hydrogen content in the a-Si films. The hydrogen content in a-Si layers can be slightly improved using forming gas anneal (FGA) process. After 30 mins of FGA at 400 ℃ the optical loss was improved to 55 dB/cm. This optical loss is far from satisfactory levels [38].

The benefit with a slot waveguide design is a lower loss compared to an all a-Si waveguide design. The loss in the all a-Si waveguide was calculated using simulations. The complex refractive index of a-Si was measured using the spectral ellipsometry equipment. These measurements were done both for as-deposited and FGA treated a-Si films. A mode analysis solver was used in COMSOL Multiphysics and the waveguide complex effective refractive index was found. The mode analysis was done using the measured complex refractive index of a-Si. The result of this simulation is the complex effective refractive index of the Waveguides. Using the imaginary part of the effective refractive index the waveguide loss was calculated [132].

A loss of 136 dB/cm was calculated for the all a-Si waveguides before the FGA process. The loss calculations showed a reduction down to 70 dB/cm for these

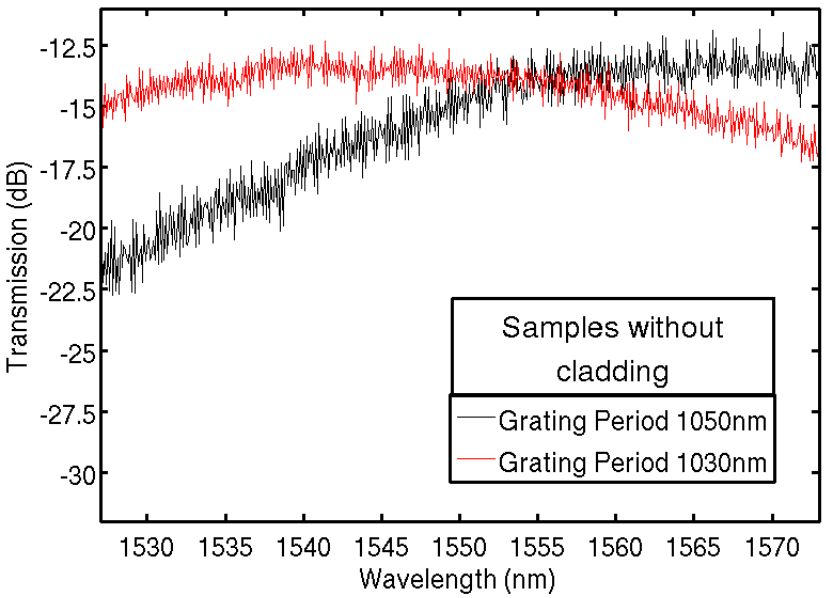

Figure 6.6: Efficiency of the fully etched double slot Al_2O_3 slot couplers with grating periods of 1030 nm and 1050 nm. These couplers are not filled with a top cladding material. Reproduced from paper III in the thesis [100]

waveguides with the FGA treatment. The cross-section schematics of the waveguides is shown in fig. 6.8. Simulations also showed that increasing the total slot thickness enhances the transmission in the slot waveguides. This trend is shown in fig. 6.9. This is due to a higher mode confinement in the slot region. For a larger slot layer a larger fraction of the mode will be distributed in the slot region. The refractive index of the slot layer can also have an effect on the waveguide loss. using the measured refractive indices HfO_2 slot waveguides have the highest loss and AlN slot waveguides the lowest. High-k slot layers in the C-band have a negligible loss. This good optical property is because of the large band gap of these dielectrics.

In order to achieve a low loss slot waveguide, PECVD a-Si can be used [38]. A-Si thin films deposited with PECVD have rich hydrogen content. Low loss all a-Si waveguides have been shown in literature using PECVD [39]. The transmission in these reported waveguides can be further improved using a slot waveguide design [132].

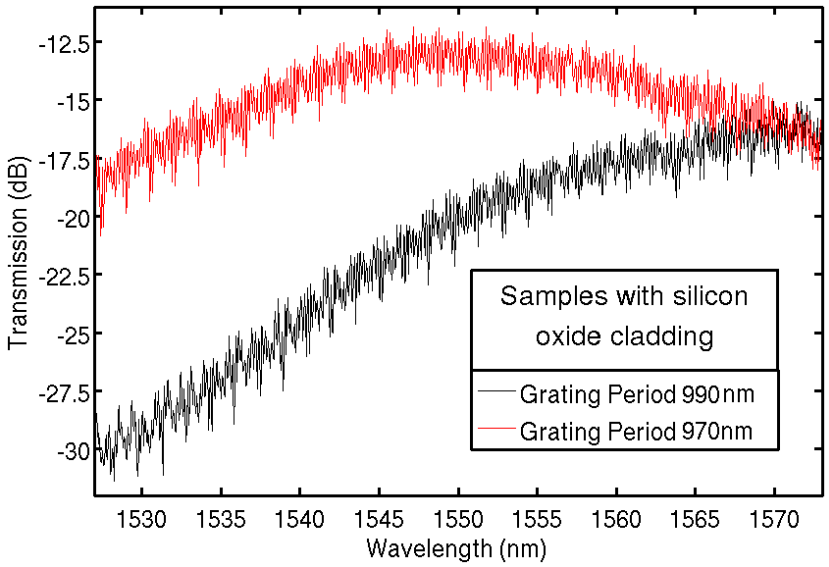

Figure 6.7: Efficiency of the fully etched double Al_2O_3 slot couplers with grating periods of 970 nm and 990 nm. The couplers were filled with SiO_2 cladding layers. Reproduced from paper III.

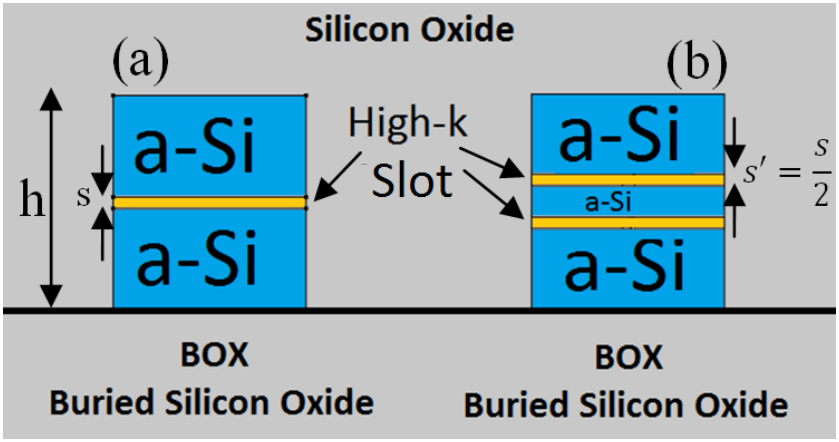

Figure 6.8: Waveguide cross-section schematics for (a) slot waveguide and (b) all a-Si mode analysis [132].

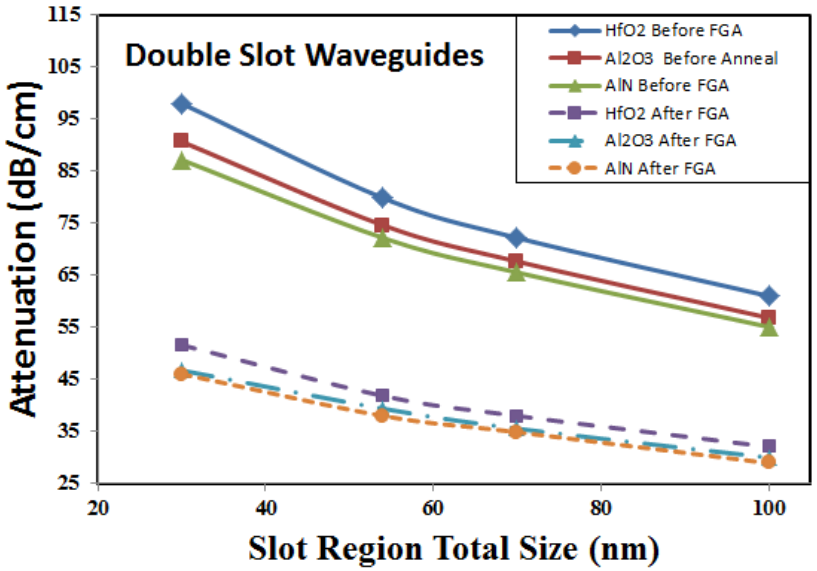

Figure 6.9: Waveguide loss vs. the slot thickness. The loss was calculated from the imaginary part of the effective refractive index of the waveguides. The loss was also simulated for Al_2O_3, HfO_2 and AlN. Reproduced from paper IV in the thesis.

Partially Etched Couplers

High efficiency grating couplers were fabricated and characterized. The third type of characterized grating couplers were single slot ALD high-k grating couplers. The slot layer was positioned lower than the middle of the waveguide to provide with less back reflections and a higher coupling efficiency. This grating coupler and waveguide design is suitable for 2D materials with non-linear optical effects. Using these optical materials detectors and modulators can be fabricated.

The coupling efficiency vs. input wavelength from the optical fiber is shown in fig. 6.10. The characterized grating coupler had a grating period of 1010 nm. The slot layer in the waveguides were 60 nm thick Al_2O_3 films. The peak coupling efficiency of the couplers was 37 % at 1552 nm wavelength. The 3dB bandwidth of the grating couplers were 60∼70 nm.

At the time of writing of this thesis, SOI grating couplers in industry have a coupling efficiency of 35.5 % (-4.5 dB insertion loss) in IHP standard passives [133] and 69 % (-1.6 dB inserion loss) in IMEC standard passives [134]. The latter technology utilizes a silicon overlay to increase the coupling [135] .The efficiency of SOI grating couplers is constrained by the BOX layer thickness. The grating couplers presented in this work can reach higher efficiencies if the bottom and the top cladding thicknesses are optimized. In addition, the grating coupler depth is

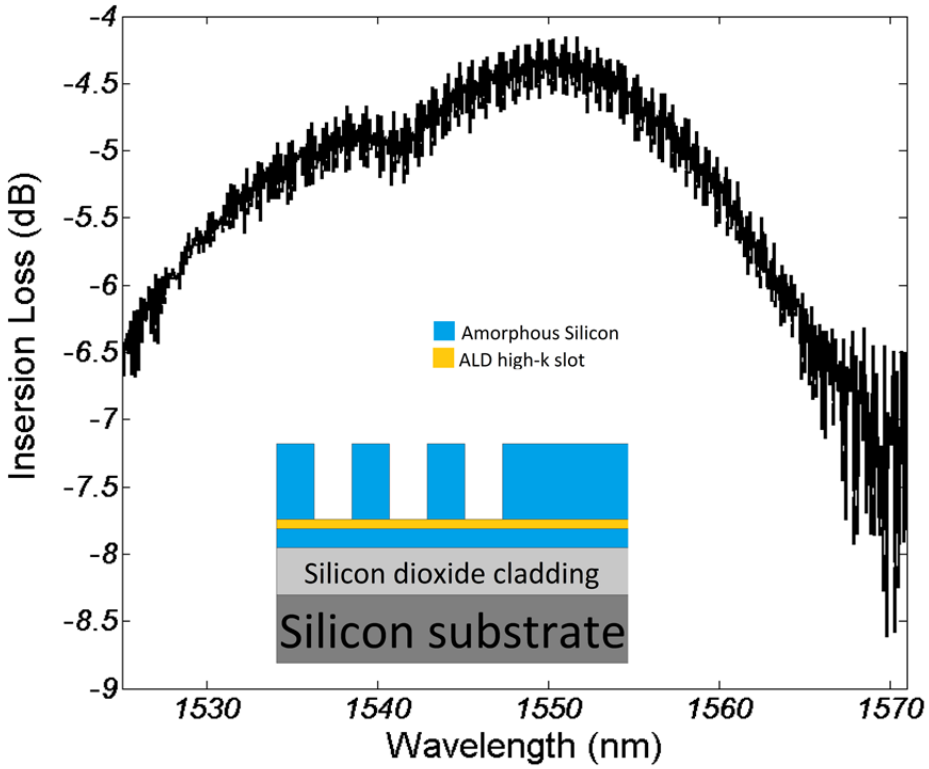

Figure 6.10: Efficienjcy spectrum of the partially etched etched Al_2O_3 coupler.

controlled by the Al_2O_3 etch stop layer. This controlled etch depth increases the uniformity of the grating couplers. Variations in the etch depth causes shifts in the coupling spectrum of the gratings. Grating couplers have a narrow coupling bandwidth. Due to this, the grating couplers are highly sensitive to the etch depth.

6.3 Germanium Photodetector

The photodetectors were characterized for their performance. The main interest with the study was to show that the fabricated diodes are suitable for integration with the waveguides.

Dark Current Density

Current-voltage measurements were done for the photodetectors in a dark ambient. A lower dark current density is favorable for the device performance. The dark

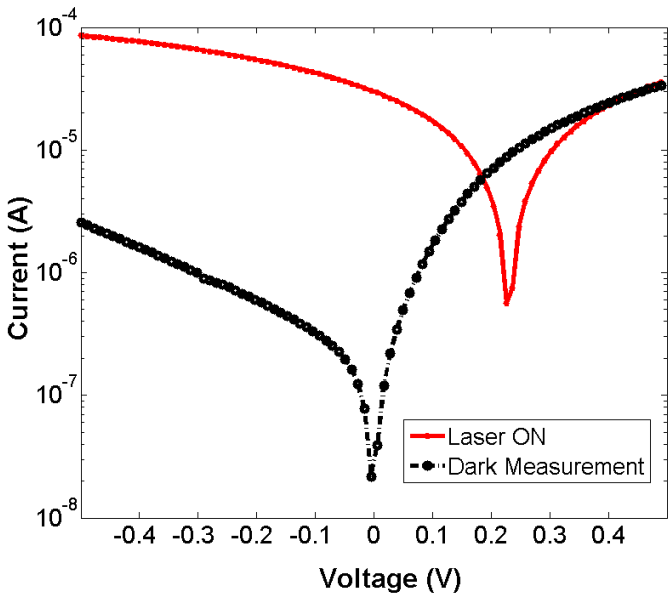

Figure 6.11: I-V measurements for a 40 μm by 50 μm active area photodetector in dark and presence of the laser beam. The laser had a wavelength of 1524 nm. Reproduced from paper V.

current density defines one of the major contributions to the current noise level of the detector at a certain bias voltage. Two device sizes were measured. Rectangular active areas of the devices had the dimensions of: A) Large detector: 40 μm by 50 μm B) Small detector: 25 μm by 50 μm. At 0.5 V reverse bias the dark current density for the large and small detectors were measured 80 mA/cm^2 and 60 mA/cm^2, respectively. A dark current density of 80 mA/cm^2 at 1 V reverse bias has been reported for waveguide integrated germanium photodetectors grown on silicon [136].

The dark current density is mainly dependent on the thickness and the crystal quality of the intrinsic germanium region. A thicker intrinsic layer of germanium will increase the resistance of the diode in reverse bias. In addition, in a higher quality intrinsic germanium less current can pass through the region. This is because of a lower density of defect states in the germanium. The better dark current density measured in the small photodetectors is because of the pattern dependency of the intrinsic layer thickness and the crystal quality. In another work high quality and strained germanium photodetectors grown on silicon had a 25 mA/cm^2 dark current density at 1 V reverse bias [46]. A higher growth rate and a better crystal quality is expected for the smaller openings.

Responsivity

The responsivity of the germanium photodetectors were calculated using the measured photoresponse. A laser beam was vertically delivered to the top of the detectors. The delivered laser beam had an optical power of 3 mW. I-V measurements were done to measure the photoresponse. Fig. 6.11 shows the current measurements in the dark and presence of the laser beam. One feature of the detectors is a photoresponse at zero-bias. Operation at zero-bias benefits from a minimal low dark current. This increases the ON/OFF current ratio.

Since the light was incident vertically, a fraction of the light was reflected at the germanium-air interface. Usually an anti-reflective coating is used on top of the detectors to avoid this reflections. The calculated reflection at this interface was 65 %. In addition to reflections, a large fraction of the optical power is absorbed in the top n-type germanium region. The thickness of the n-type region of the PIN stack was about 200 nm. The absorption of light in this region is 20 %. In an integration scheme the light is directly incident to the edge of the intrinsic region of the detector. Therefore, the 65% reflection and 20 % absorption will not be present. In order to give a more realistic figure of merit for the integrated detectors, the optical power incident at the intrinsic region was calculated. An incident power of 0.88 mW was calculated taking reflection and absorption into account. The effective responsivity was calculated using this optical power. For a 40 μm by 50 μm active area photodetector, a responsivity of 0.1 A/W was calculated for a 0.5 V reverse bias.

6.4 Graphene Photodetectors

The photodetectors were characterized by injecting the light into the grating couplers and measuring the photo-response current. Photodetectors with the length of 40 μm were characterized [103]. Given a 37 % transmission through the grating couplers and 3dB total loss in the waveguide, the responsivity was calculated from the measured photo-current. A responsivity of 3.5 mA/W was measured for the photodetectors at 1.5 V bias. The integration schemes reported in the literature use SOI waveguides [137, 138]. The photodetectors presented in this work can be manufactured on a bulk silicon wafer or the process can be transfered to the BOEL process of the CMOS technology.

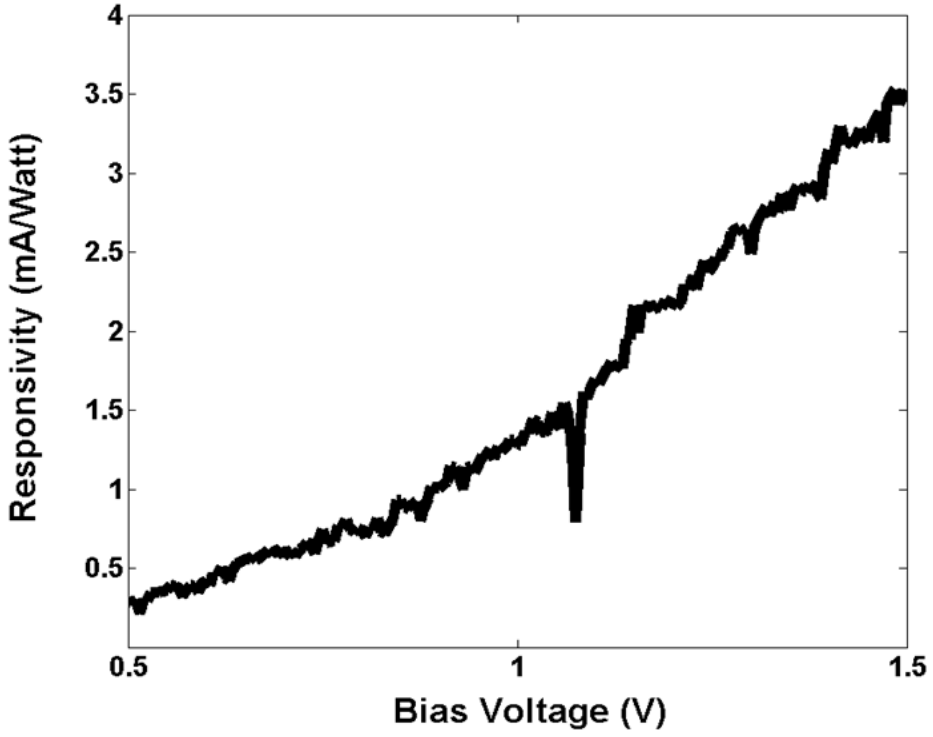

Figure 6.12: Responsivity of the 40 μm long integrated graphene photodetectors. This responsivity was calculated by considering losses in the grating couplers and the attenuation of the waveguide. In paper VI.

Conclusions and Future Outlook

Optical interconnection will be required in the future CMOS technology due to higher demands on data transfer rates. Yet it is not known which approach, and set of devices that will be the ultimate cost effective and feasible solution for CMOS-friendly silicon photonics. Currently, most of the presented active and passive devices available in the literature use the SOI technology. Transferring of the devices to the top layer of a microprocessor is a tedious task. The expected achievable yield with the SOI approach is not clearly known.

This thesis has introduced an original approach to realize devices that eventually can build cost effective photonic integrated circuits. Inspired by the current BEOL process of CMOS technology, this thesis has proposed to use deposited dielectric thin films to form waveguides on top of the active semiconductor layer. In this context horizontal slot waveguides were presented. This type of waveguides enable the use of other optically active materials. In this work high-k dielectrics were exclusively investigated.

Grating couplers were investigated as a building block for integrated waveguides. It was shown that the operation of the grating couplers are sensitive to the material choice and the thickness of the slot layer which originates from change in the effective refractive index of the waveguides with the slot properties.

Fully etched grating couplers were designed for high-k slot waveguides. The fabrication process of these devices were investigated. Dry etching of the high-k layers required special fine tuning to maintain the waveguides line edge roughness. In order to facilitate wafer-scale opto-electrical measurements an instrument was developed. This setup features tunable fiber angles and high precision XYZ positioners for effective coupling through the gratings.

The highest coupling efficiency achieved with the fully etched couplers was 22% with this design. A partially etched grating coupler design would have a better performance because of lower back reflections. A partially etched grating coupler with 37% coupling efficiency was demonstrated. As an extension to the current studies it will be essential to study other high-k materials. Investigation of engineered thin films can broad the horizons for active photonic devices enabled by slot waveguides. Example of these engineered materials are as follows: 1) nano-crystalline silicon embedded in SiO_2 (formation of silicon islands in silicon rich SiO_2). 2) Erbium doped Al_2O_3 horizontal slot waveguides for light amplification at 1.5 μm

3) Thulium doped Al_2O_3 for light generation at 2 μm wavelength range.

Investigation of the transmission in the waveguides showed that there is room for improvements. The required optical quality of the a-Si layer to be engineered for higher hydrogen content. Based on the reported values for all-silicon waveguides the slot waveguides should deliver an acceptable transmission rate as well as to have lowest possible attenuation.

An integration scheme was shown for germanium photodetectors. In this scheme, bulk silicon substrates were used as the growth seed of the photodetectors. Selective growth of germanium was presented and the fabrication of the waveguides and detectors in test chips were presented. Due to high temperature treatments during the fabrication, the waveguide morphology was harmed. The author suggests a process in which the waveguides are fabricated after the germanium growth step. Integration of these waveguides with other active devices is worthwhile. Electro-optical modulators using Ge, GeSi or GeSnSi alloys integrated with these waveguides would be highly interesting. The platform is not only limited to group IV photonics. These waveguides can also be studied for integration with III/V light emitters or modulators.

The fabricated PIN germanium detectors had a low dark-current density of 60 mA/cm^2 and an effective responsivity of 0.1 A/W at 0.5 V reverse bias. Using cyclic annealing steps strained germanium can be achieved in which, the responsivity and the dark current can be improved.

A novel integrated solution was presented for graphene photodetectors. By taking advantage of the field enhancement in the slot region a better light-matter interaction can be achieved. Test chips with integrated graphene photodetectors were fabricatated and characterized. Through the first attempt, a responsivity of 3.5 mA/W was measured. These photodetectors require a more extensive study. The quality of the graphene layer can effect the waveguide performance. During the process some residues were observed on the graphene layer that degraded the guiding. In addition, graphene modulators are of a great interest and can be implemented through the same photonics platform. A second graphene layer is required as the gating metal to alternate the absorption. This device can operate as a detector if the gate is not biased, making it a two-purpose device. If this is achieved, a full off-chip-source integrated photonic circuit can be realized. This platform would not require crystal growth. Also the two-purpose devices enable monolithic fabrication of the circuits.

This thesis has taken an effort to introduce a new viable alternative to the SOI counterpart that is currently used in the research. This method requires improvements and the integrability of this waveguide technology with active devices need to be presented further more. The solutions demonstrated in this work were motivated to simplify the silicon optical interconnects and improve the manufacturability of this technology, with an eye on the cost effectiveness.

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