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Effects of 3-MeV Protons on 4H-SiC Bipolar Devices and Integrated OR-NOR Gates

Sethu Saveda Suvanam, *Student Member, IEEE*, Luigia Lanni, Bengt Gunnar Malm, *Senior Member, IEEE*, Carl-Mikael Zetterling, *Senior Member, IEEE*, and Anders Hallén

Abstract—Radiation effects of 3-MeV protons on 4H-SiC bipolar devices and integrated OR-NOR gates have been investigated. The chips were irradiated from a fluence of $1 \times 10^8 \text{ cm}^{-2}$ until $1 \times 10^{13} \text{ cm}^{-2}$. Up until a fluence of $1 \times 10^{11} \text{ cm}^{-2}$, both the bipolar devices and the logic gates were found to be stable, but for higher fluence, they begin to degrade as a function of irradiation fluence. Using TCAD simulations, degradation of the transistor current gain has been found to be more dominated by surface states than bulk defects generated by the proton irradiation. Simulations of logic circuits using SPICE show that the gain degradation is the key contribution to the unstable performance of the circuits from the fluence of $1 \times 10^{12} \text{ cm}^{-2}$ and above.

Index Terms—4H-SiC, bipolar integrated circuits, emitter couple logic (ECL), OR-NOR gates, proton radiation.

I. INTRODUCTION

INCREASING demands for extreme environment electronics has opened new frontiers for exploring materials beyond conventional silicon (Si). Silicon carbide (SiC) is a wide band-gap semiconductor, which is a strong candidate for high-power, high-temperature, and high-radiation-level applications. Due to the wide band-gap (3.26 eV at room temperature) of 4H-SiC, on the average 8-9 eV is needed to produce an electron-hole pair, which is about 3 times more than for Si. Also, the relatively high atomic displacement energies (20–35 eV) are a contributing factor for SiC to be more radiation-hard [1]. Si devices and circuits have been extensively studied since 30 years, and the radiation standards have been established [2], [3], [4]. For SiC, some investigations have been made on discrete SiC devices so far such as diodes, MISFET, BJT, etc., under proton, heavy ion, and gamma ray exposure [5]–[8], but there exist no such studies on SiC integrated circuits (ICs). Many SiC ICs, utilizing different devices, have been tested for high-temperature operations since the 1990s [9]–[11]. In regards to bipolar-based SiC ICs, Singh *et al.* [10] have demonstrated transistor-transistor logic (TTL) operating at 355 °C with propagation delay of

Fig. 1. NPN transistor. (a) Cross section. (b) Optical image. Dashed line is the cross-section line [18].

~ 10 ns similar to that of Si TTL ICs. Operation of emitter coupled logic (ECL)-based ICs has been reported up to 500 °C [11]. In this paper, an investigation is presented to understand the effects of 3-MeV proton irradiation on the performance of 4H-SiC high temperature OR-NOR gates realized with ECL, and to correlate these results with the degradation of individual transistors.

II. EXPERIMENT

The devices and circuits were fabricated on a six-layer epitaxial structure ($n^{++}/n^{+}/p/n^{+}/n^{++}/p$) grown on an 8° off-axis 4H-SiC 2-in wafer purchased from SiCrystal AG. To minimize the amount of defects, epitaxy was performed in a continuous run. Fig. 1(a) and (b) shows the cross section ($162.5 \times 5.3 \mu\text{m}^2$) and top view ($162.5 \times 105 \mu\text{m}^2$) of the fabricated low-voltage NPN transistors. A p-isolation layer provides isolation between each device in the circuit. The thickness and doping concentration for each of the six layers can be inferred from Fig. 1(a). Mesa etches for emitter, base, and collector were done using plasma etch with HBr and Cl_2 followed by sacrificial oxidation. A 50-nm PECVD deposited SiO_2 , annealed in N_2O at 1250 °C, acts as surface passivation. For n-type emitter and collector contacts, Ni was deposited by e-beam evaporation, whereas for p-base and the p-type isolation-layer contacts, a stack of Ni/Ti/Al was used. A thick SiO_2 is deposited as interdigitated dielectric, and finally Ti/TiW/Al was sputtered and patterned to form interconnects.

The test chip contains isolated NPN transistors that are individually measureable and OR-NOR gates designed using the emitter coupled logic (ECL) technology. As shown in

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The authors are with the KTH Royal Institute of Technology, 16440 Kista, Sweden (e-mail: suvanam@kth.se).

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Fig. 2. Circuit design of OR-NOR logic gate using ECL technology [12].

TABLE I
SUMMARY OF PROTON IRRADIATION PARAMETERS DURING THE TWO ROUNDS OF IRRADIATION FOR THE INTEGRATED CIRCUITS Z1–Z3

Integrated Circuit	Irradiation energy (MeV)	1 st round of irradiation		2 nd round of irradiation	
		Beam Current (nA)	fluence (cm ⁻²)	Beam Current (nA)	fluence (cm ⁻²)
Z1	3.0	0.04	1×10^8	1	1×10^{11}
Z2			1×10^9		1×10^{12}
Z3			1×10^{10}		1×10^{13}

Fig. 2, each OR-NOR circuit consists of 10 NPN transistors and 11 resistors [12].

Three integrated circuits (Z1, Z2, Z3) fabricated on the same wafer are used in this experiment. As shown in Table I, the irradiation was done at room temperature in two rounds with a 3.0-MeV proton beam. In the first round, Z1, Z2, and Z3 were irradiated with the fluence of 1×10^8 , 1×10^9 , and 1×10^{10} cm⁻²; and in the second round with the fluence of 1×10^{11} , 1×10^{12} , and 1×10^{13} cm⁻², respectively, at the Ion Technology Center in Uppsala, Sweden. The beam current during irradiation was in the range of 40 pA for the first three fluences and 1.0 nA for the final three fluences. The beam was scanned across the entire surface of the circuit to achieve a homogeneous coverage. SRIM [13] simulation shows that the protons will reach about 60 μ m, which is deep in the n-substrate. However, a roughly constant level of both lattice displacements (damage) and ionization is produced in the active region of the circuits and devices. All the devices and circuits on the chips were measured before irradiation and again after the first and second rounds of irradiation by direct on-chip probing (no package was used).

Electrical measurements of the OR-NOR gates have been performed at room temperature within about one week of the proton irradiation. Since annealing effects in irradiated SiC devices at

Fig. 3. Output characteristics of low-power NPN transistor (normalized collector current (I_{CE}) versus collector voltage (V_{CE}) for different irradiation fluences (1×10^{10} cm⁻² – 1×10^{13} cm⁻²). For lower fluence, the variation of the saturation current (I_{CS}) is very small.

room temperature after a period of several months have been reported [20], the measurements presented here were done at various occasions during a period of one week. For this time period, no change in data was found. A supply voltage (V_{EE}) of -15 V was used, and the circuit output was measured by sweeping the input voltage from -7 to 0 V at only one of the inputs (A or B). In this way, a low logic level was seen by the other input terminal because of its connection to V_{EE} through the pull-down resistor (R_{i1} or R_{i2}).

III. RESULTS AND DISCUSSION

Fig. 3 shows the normalized collector current (I_{CE}) versus collector voltage (V_{CE}) at a base current (I_B) of 200μ A for the low-voltage NPN transistors measured after different irradiations. It was observed that until a fluence of 1×10^{10} cm⁻², the reduction in the collector saturation current (I_{CS}) is almost negligible ($\sim 4\%$). However, from a fluence of 1×10^{11} cm⁻², I_{CS} decreased strongly as a function of the irradiation, and at the highest fluence, I_{CS} is reduced by 85%. Fig. 4 shows the normalized $\beta(I_C/I_B)$ as a function of proton fluence. The β of each irradiated device was normalized to their respective pre-irradiation values, i.e., β obtained from 1×10^8 cm⁻² and 1×10^{11} cm⁻² irradiations were normalized to the pre-irradiated β obtained from Z1, and similarly for other fluences. About two to three devices per chip were measured, and β spread was found to be negligible.

Fig. 4 shows a strong decrease in β with fluence for fluence above 1×10^{11} cm⁻². For lower fluences, a relatively small linear decrease of β is seen. Similar dependencies of gain degradation versus fluence have been reported in Si-based bipolar devices under the same irradiation energy [21]. Generally, gain degradation due to proton irradiation can be classified by bulk defects created by displacement damage, and by band-gap states in the oxide and at the oxide/SiC interface due to ionization [4].

Sentaurus TCAD device simulations software [15] has been utilized in order to investigate the degradation. The Shockley–Read–Hall (SRH) lifetime (τ), associated with deep band-gap states in the bulk arising from the displacements, and a concentration of surface states due to ionization have been

Fig. 4. Normalized β as a function of proton fluence, showing a rapid degradation in β after $1 \times 10^{11} \text{ cm}^{-2}$.

Fig. 5. Six TCAD-simulated β versus collector current (I_{CE}). The black lines show β for various values of bulk lifetime (τ) and surface states pinned at $6 \times 10^{12} \text{ cm}^{-2}$. Red lines show β for various interface states densities for a bulk lifetime pinned at 100 ns .

used to fit the simulations. In Fig. 5, the black curves show the simulated β versus collector current (I_{CE}) for various values of bulk lifetime (τ), while the surface states are pinned at a value of $6 \times 10^{12} \text{ cm}^{-2}$. It can be observed that a decrease of the bulk lifetime from 100 to 25 ns (75% reduction) results in a reduction of β from 26 to 20 , i.e., only 23% reduction.

A similar trend as a function of τ has been observed also for different fixed densities of surface states. In order to understand this phenomenon, the approximate number of vacancies introduced into the active region of device was calculated using SRIM simulation. It was found that for the highest proton fluence, about $2 \times 10^{16} \text{ cm}^{-3}$ vacancies are produced in the base area of the BJT. At room temperature, about 10% of these created vacancies from low mass ion irradiation will produce stable, electrically active defects. The remainder of the primary defects will recombine or form electrically inactive defects [16]. Since these NPN devices have a relatively high doping ($5 \times 10^{17} \text{ cm}^{-3}$) in the base region, introducing defects that are two orders of magnitude less will not contribute to doping compensation, as reported in [7] for power transistors with much lower base doping. On the other hand, the red curves in Fig. 5 show

Fig. 6. Interface states and bulk lifetime normalized to the unirradiated samples as a function of dose, extracted from TCAD simulation by fitting the simulated results to match the peak β of the measured devices. τ_0 and D_{it0} are the bulk lifetime and interface states of unirradiated samples w.r.t. which the normalization is done.

the simulated β versus I_C for various interface state concentrations, with the bulk lifetime pinned at 100 ns . It can be clearly seen that, in this regime, the surface states have a greater influence on the β degradation than the bulk lifetime.

Thus, the degradation of β for these devices could be explained by two simultaneous processes due to the irradiation: 1) introduction of bulk point defects in the material, which act as recombination centers, thus reducing the minority carrier lifetime; 2) creation of surface states at the emitter-base mesa passivation, increasing the recombination currents. Due to the high base doping of the tested BJTs, which will give a relatively low lifetime of about 100 ns in the p-base, process 2) is expected to be dominant for the β degradation in this fluence regime. This also highlights the importance of developing new dielectrics for SiC that are more stable under radiation environment, for instance Al_2O_3 [17], [18].

The measured device characteristics have then been fitted with simulated results to match the peak β value. Extracted interface states and bulk lifetime at various doses normalized to the unirradiated sample is shown in Fig. 6. A crude estimate of the bulk lifetime in the p-type base region can be made from the following equation:

$$\tau = 1/(\sigma_e v_{th} N_T). \quad (1)$$

A value of 10% of the vacancies extracted from the SRIM simulation is used as the concentration of electrically active traps, $N_T = 1 \times 10^{15} \text{ cm}^{-3}$, and for the electron capture cross section σ_e to the dominating lifetime controlling defect in 4H-SiC, the carbon vacancy, a reported measured value of $1 \times 10^{-15} \text{ cm}^2$ [19] is employed. The thermal velocity, v_{th} , is estimated to be about 10^7 cm/s . Thus, from (1), τ was found to be 100 ns for fluence $1 \times 10^{13} \text{ cm}^{-2}$. It can be noted that the bulk lifetime extracted from the TCAD simulation for the same fluence was 45 ns , which is of the same order of magnitude as the estimation by (1). In conclusion, any change in bulk lifetime due to the highest fluence used in this study barely causes any change in gain, and therefore the most likely cause for the degradation is surface recombination due to surface states.

Fig. 7. Voltage transfer characteristics of the OR output of the OR-NOR logic gate. Up to fluences of the order of the $1 \times 10^{11} \text{ cm}^{-2}$ the circuits appear unaffected. Dashed and solid arrows show the degradation in logic threshold and logic high, respectively.

Fig. 7 shows the voltage transfer characteristics (VTCs) for the OR output of an OR-NOR gate after irradiations at different fluences. No significant change can be observed in the output logic levels and logic thresholds, defined as the central intersection point in the voltage transfer characteristic, of the gates irradiated with fluences up to $1 \times 10^{11} \text{ cm}^{-2}$, which results in stable noise margins of about 1 V.

When higher fluences are used, the gate VTC shows evident changes. Specifically, from the fluence of $1 \times 10^{12} \text{ cm}^{-2}$, a shift toward negative voltage of the threshold voltage can be seen, which replicates the voltage at node V_{REF} in Fig. 2. The logic levels are also reduced, mainly due to the reduced current gain of the BJTs in the gate. Output logic swing and noise margins show no significant changes at this fluence. Fluence as high as $1 \times 10^{13} \text{ cm}^{-2}$ cause an even larger shift of the threshold voltage toward negative voltage and a strong reduction of the output logic swing, which translate to a significant lowering of the low noise margin. For the reported gate, the logic threshold follows the potential at the node V_{REF} , the reference voltage, in Fig. 2. This determines the voltage around which the input voltage changes from logic high to low for a given output voltage, or vice versa. For this reason, changes in transistors and/or resistors in the net that controls the reference voltage can affect the circuit behavior. Thus, degradation of the OR-NOR gate with increasing irradiation fluence can be attributed to the reduced BJT performance as previously described.

SPICE simulations are able to predict the gate VTCs after irradiation if adequate BJT SPICE models are used. As shown in Fig. 8(a) and (b), a satisfactory agreement is achieved between measured and SPICE simulated OR and NOR VTCs, respectively, for both fluence $1 \times 10^{11} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$. It is worth noticing that, for each fluence, an adequate BJT SPICE model was extracted based on forward and reverse device characteristics measured on a BJT irradiated with that fluence, while the emitter layer sheet resistance was measured at $170 \Omega/\text{square}$ for both fluences.

Finally, it should be noted that it is difficult to assess the relative radiation hardness of SiC bipolar devices compared to existing Si technology. Radiation effects on any device depend

Fig. 8. SPICE simulated and measured voltage transfer characteristics for fluence of the order of the $1 \times 10^{11} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$. (a) OR output. (b) NOR output. For the simulations estimated value of $170 \Omega/\text{square}$ was used for the emitter sheet resistance.

strongly on the nature and design of devices. Thus, an absolute comparison cannot be made unless the devices have the same design but are made of different materials. For instance, by comparing to a recent article on Si BJT irradiated with 3-MeV protons [21], it seems that the degradation occurs at roughly the same fluence. However, the devices in [21] were power BJTs, and these have typically much lower base doping. It is therefore likely that reduction of the bulk lifetime will be the cause for degradation, while in our investigation, the surface states are pointed out as the main cause for degradation. This again indicates the importance of improving the quality of dielectrics for SiC to improve the radiation hardness of SiC devices in comparison to Si devices.

IV. CONCLUSION

A result of the degradation of 4H-SiC logic circuits as a result of 3-MeV proton exposures is reported in this paper. Up to a fluence of $1 \times 10^{11} \text{ cm}^{-2}$, the performance of both the devices and circuits appear unaffected, but for higher fluence, the devices and circuits degrade rapidly. TCAD simulations of the

prototype device showed that the gain degradation is a combined process of both displacement and ionization. It is shown that the ionization is most influential in the degradation process by introducing interface states that lower the current gain, β . SPICE circuit simulations showed a good match with measured OR-NOR logic gates for various fluence. Due to the gain reduction of the BJTs, the voltage reference of the logic circuit has been affected and this, in turn, degrades the VTC of the OR-NOR gates.

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