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Fault Analysis on Distribution Feeders Employing Solid State Transformers

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Abstract— This paper focuses on fault analysis of a distribution feeder which employs Solid State Transformers (SSTs) rather than magnetic transformers in order to facilitate large scale integration of Distributed Energy Resources (DERs) into the system. To estimate the fault current profile on such a feeder, the paper proposes a new method which extends the capability of conventional short-circuit analysis method. Performance of the proposed method has been assessed by simulations on a sample distribution feeder.

Index Terms-- solid state transformer (SST), fault analysis, distribution system, PSCAD/EMTDC.

I. INTRODUCTION

Recently, there has been considerable effort towards infusion of new technologies into distribution systems in order to facilitate the integration of Distributed Energy Resources (DERs) into a distribution system [1-4]. Microgrids have emerged as one of the approaches [5], and an extended version of this approach employs power electronics based Solid State Transformer (SST) to replace the magnetic distribution transformer at every node to facilitate DER integration [6]. SST offers very desirable features such as regulated voltage at the secondary side, reactive power compensation at the primary side, voltage sag ride-through, and fault isolation between the primary and the secondary sides [7-9]. These features coupled with a communication capability facilitate the management of generation, storage, and loads at distribution level [10].

SSTs impact the protection system as they will contribute to the fault current during a fault. As the penetration of SSTs on a feeder gets higher, the fault current profiles on such a system will be considerably different than that of the feeder with no SST. These fault current variations will in turn impact the operation and coordination of protection devices on such a feeder considerably [11]. Since conventional short-circuit analysis methods provide only one snapshot of the fault current [12], they become inadequate to analyze the fault current variations on such SST-dominated feeders and estimate their impact on protection relays and devices.

The impact of power electronics based devices, typically

converters interfacing Distributed Generation (DG), on fault current profile of distribution systems has been investigated in literature [13,14]. However, SST has different impact on the fault current profile as it is designed to serve mixture of load and generation; hence, it acts as an active prosumer² in the system. Also, the special self-protection scheme employed for the SST makes the current contribution from a SST different than that of a regular converter.

This paper proposes a method which can provide an estimate of fault current variation on a SST-dominated distribution feeder during the first few seconds of the fault occurrence. This enhanced fault analysis method will enable the protection engineers to design and coordinate protection schemes on such feeder [15]. In the next section, the paper shows that both the current injection from a SST, as well as the protection scheme employed for the SST need to be considered in order to capture the SST's response to a fault. In section III, the proposed fault analysis method has been introduced. Conclusions are drawn in section IV.

II. SOLID STATE TRANSFORMER (SST)

A. Basic Configuration

The solid state transformer is a power electronic device that replaces the traditional magnetic power transformer by means of high power converters, as shown in Fig. 1. The SST consists of three main components: a high voltage AC/DC rectifier that regulates a high voltage DC bus, an isolated high frequency operated DC/DC converter to regulate the secondary DC bus, and a DC/AC inverter to regulate the output terminal AC voltage which serves the local loads and DGs (alternatively called prosumer cluster in this paper) [6,16].

Considering that SST power loss is relatively negligible, the active power that flows through the SST is equal to the net active power that the prosumer cluster on the SST secondary side either demands from or supplies to the SST, i.e. $P_H \approx P_L$. SST can provide the reactive power on the prosumer side (Q_L) while it operates under unity power factor at the primary side. Moreover, if needed, SST can provide reactive power compensation (Q_H) to the grid [17].

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² **prosumer** = **producer** + **consumer**

Fig. 1. Basic configuration of SST.

SST has also self-protection for which it usually employs an under/over voltage scheme that monitors the high voltage DC bus, as shown in Fig. 1. The protection scheme immediately shuts down the SST if it detects any abnormal voltages on the high voltage DC bus. This will be more discussed in the next section.

B. Behavior under Fault

When a fault occurs on the feeder, the SST feeds current to the fault. The current to be injected depends on the SST rectifier design. SST is designed to transfer the active power demanded/generated by the prosumer from/to the system and also to provide reactive power compensation to the system. So the SST rectifier tries to transfer this power even under low voltage conditions which occur during a fault, i.e., it will try to act like a constant power source. Hence, the current injection from a SST to the system can be approximated as $\vec{I} = (P_H + jQ_H)^* / \vec{V}$ where P_H is the transferred active power, Q_H is the SST reactive power compensation to the system, and $\vec{V}$ is the AC terminal voltage at the SST primary side. However, if this current gets to be higher than the maximum current rating of the SST rectifier, the rectifier limits the current at its maximum level which is typically 1 to 2 times the rated current [16]. Hence, for fault studies, we will assume the limiting current to be 2 times the rated current, for worst case scenario. Thus, from the system point of view, the SST will have the V-I characteristics shown in Fig. 2. This V-I characteristics has been verified by using a detailed SST model simulated on PSCAD, and will be introduced in the next section. We propose to use the V-I characteristics on Fig. 2 in the fault analysis in order to estimate the fault current contribution from a SST. This can be achieved by modeling the SST as a controlled current source whose properties depend on its terminal voltage and reactive power compensation, and also the transferred active power. Fig. 3 illustrates this model.

Another important factor which affects the current contribution from a SST during a fault is the protection scheme employed for the SST. Table I summarizes a possible scheme to be employed for the protection of SSTs. As the table indicates, the protection module shuts down the SST when it detects abnormal voltage on the HVDC bus. Note that when a fault occurs on the feeder, the time it will take for the protection scheme to shut down the SST depends on the variation of the HVDC bus voltage. This variation, in turn, depends on the active power demanded/generated by the prosumer (P_L), the reactive power compensation (Q_H), and

Fig. 2. V-I characteristics of a SST.

Fig. 3. SST model for fault analysis.

TABLE I. PROTECTION SCHEME FOR A SST

HVDC bus voltage	trip time
$V < 0.7\text{pu}$	immediately
$0.7\text{pu} \leq V < 1.2\text{pu}$	normal operation
$1.2\text{pu} \leq V$	immediately

the post-fault terminal voltage at the SST primary side ($\vec{V}$). These dependencies have been illustrated in Figs. 4 to 6 by means of PSCAD simulations. In this study, an average model of SST reported by [6] has been adopted for simulation.

Fig. 4 depicts the HVDC voltage variation for different values of P_L when a fault occurs on the feeder. For all of these cases, $\vec{V}$ and Q_H are 0.3 p.u. and zero, respectively. Subsequent to the fault occurrence, the SST tries to increase its primary current to transfer the active power demanded/generated by the prosumer (P_L). However, as the primary current gets limited to 2 p.u., the demanded/generated P_L cannot be fully transferred (i.e. $P_H < P_L$) and will be partially drawn/sunk from/to the HVDC capacitor, making it discharge/overcharge. As the figure shows, the higher the P_L is (either demanded or generated), the faster the bus voltage hits the limits and the protection scheme shuts down the SST. Note that for low values of P_L (0.1 p.u.), the HVDC voltage remains regulated as the SST can still transfer the P_L by increasing the primary current before it hits the 2-p.u. limit (i.e. $P_H = P_L$).

Fig. 5 shows simulation results from the same test except that P_L is kept constant at 0.65 p.u. and the HVDC voltage variation is observed for different values of Q_H . Since $|\vec{I}| = |(P_H + jQ_H)^* / \vec{V}|$ is limited to 2 p.u., the presence of Q_H reduces the amount of P_H that can be transferred, leading to a higher mismatch between P_H and P_L . As shown in the figure, the higher the Q_H is, the faster the bus voltage hits the limits and the protection scheme shuts down the SST.

Fig. 4. Variation of SST HVDC bus voltage and primary current for different values of P_L when a fault occurs on the feeder.

Fig. 5. Variation of SST HVDC bus voltage and primary current for different values of Q_H when a fault occurs on the feeder.

Fig. 6 depicts the HVDC voltage variation from the same test but, this time, P_L and Q_H are kept constant at 0.65 p.u. and zero, respectively, and $|\vec{V}|$ is varied by changing the fault resistance. As shown in the figure, the lower the $|\vec{V}|$ is, the faster the bus voltage hits the limits and the protection scheme shuts down the SST. Note that when the $|\vec{V}|$ is high enough

(0.5 p.u.), the HVDC voltage remains regulated as the SST can still transfer the P_L by increasing the primary current before it hits the 2-p.u. limit (i.e. $P_H = P_L$).

In order to consider the effect of such protection scheme on SST current contribution during a fault, the voltage of the HVDC bus has to be estimated as shown in Fig. 7. In this figure, C is the HVDC capacitor and W is the capacitor stored energy. As $W = \frac{1}{2} C V_{HVDC}^2$, V_{HVDC} variations due to mismatches between P_H and P_L can be obtained as:

$$V_{HVDC(t-t_0)} = V_0 + \Delta V_{HVDC(t-t_0)} = V_0 \pm \sqrt{\frac{2|\Delta W_{(t-t_0)}|}{C}} \quad (1)$$

where V_0 is the HVDC regulated voltage and t_0 is the instant of fault occurrence. As $\Delta W_{(t-t_0)} = (P_L - P_H)(t - t_0)$, we can rewrite (1) as:

$$V_{HVDC(t-t_0)} = V_0 \pm \sqrt{\frac{2|P_L - \text{Re}(\vec{V} \vec{I}^*)|(t - t_0)}{C}} \quad (2)$$

As illustrated in Figs. 4 to 6, (2) shows that V_{HVDC} variation depends on P_L , Q_H (through $\vec{I}$), and $\vec{V}$.

Fig. 6. Variation of SST HVDC bus voltage and primary current for different values of $|\vec{V}|$ when a fault occurs on the feeder.

Fig. 7. Power flow through SST HVDC capacitor.

Since the protection scheme shuts down the SST when V_{HVDC} drops to $0.7V_0$ (for demanded P_L) or rises to $1.2V_0$ (for generated P_L), we can obtain the SST disconnection time by replacing V_{HVDC} in (2) with those values:

$$t_{disc.} = t_0 + \frac{C(C_P V_0 - V_0)^2}{2|P_L - \text{Re}(\vec{V} \vec{I}^*)|} \quad (3)$$

where C_P is 0.7 (for demanded P_L) and 1.2 (for generated P_L). Note that for faults where SST can still transfer P_L from/to the grid, $P_L \approx \text{Re}(\vec{V} \vec{I}^*)$ which results $t_{disc.}$ to be infinity.

Also note that an important implication of such a voltage dependent protection scheme is that on a feeder with many SSTs connected along its length, the SSTs will be disconnected from the feeder at different times during a fault. As a result, the fault current will be varying. Hence, in order to be able to determine such a fault current profile on a feeder, we need to extend conventional fault analysis method by incorporating both the V-I characteristics and protection schemes of SSTs. Next section introduces the proposed scheme for this purpose.

III. FAULT ANALYSIS METHOD

A. Algorithm for Fault Analysis

Fig. 8 shows the proposed algorithm for the fault analysis method for a SST-dominated feeder. As the figure shows, the fault is assumed to occur at $t=0$ and then the algorithm first calculates the node voltages ($\vec{V}$) and branch currents ($\vec{I}_{branch}$) during the first period after the fault where all SSTs respond to the fault and contribute to the fault current. Since, SST current injection ($\vec{I}_{SST}$) depends on its terminal voltage, an iterative procedure is needed to obtain the solution, as the figure illustrates. The SST model indicated in the figure is the controlled current model developed in the previous section (Fig. 3). In the next step, response of the SST protection is emulated in order to determine the SSTs that will shut down by their protection system, and how long it will take for the protection scheme to disconnect them ($t_{disc.}$ in (3)). Once this time, Δt , is identified, the algorithm increments simulation time by Δt and disconnects the SSTs identified. The algorithm then updates the node voltages and branch currents by repeating the calculations done at the first step. This loop is repeated until the SST protection does not disconnect any more SST.

B. Test Results

To evaluate the performance of the proposed method, an actual distribution system serving mostly residential loads in a suburb of Raleigh NC is considered as the test case in this study. The feeder has three-phase primary with several single-phase underground cables tapped off from the main circuit to feed the customers within the same neighborhood. For this study, this system is simulated using PSCAD in order to get

Fig. 8. Proposed fault analysis algorithm for a SST-dominated feeder.

detailed time domain simulations and to use them for comparison with the proposed method. Since it was not practical to include all loads individually in the simulation, the loads on the single-phase laterals served off the main line sections have been aggregated as one lumped load as shown in Fig. 9. Also, a Photovoltaic system (PV) has been added to each node as DG and the distribution conventional transformers have been replaced by SSTs. The SST is simulated by adopting the model, introduced in [6], which uses average models for the converters, and includes the previously discussed protection scheme. Fig. 10 shows the I-V curve of the adopted SST model obtained from the simulation results. As shown in the figure, the SST operates under two modes of operation: constant power and constant current.

Performance of the proposed method has been assessed by comparing the results obtained from the method with the results obtained from PSCAD simulations under different scenarios. Figs. 11 and 12 compare the results for a number of selected scenarios (due to paper space limit). The fault currents given are the fault currents through the feeder circuit breaker under three-phase faults when all SSTs on branch 1 are operating with 1 p.u. generated P_L and all SSTs on branch 2 are operating with 1 p.u. demanded P_L .

As the figures show, the method calculates the current levels and the time instants at which the current level changes. Fault currents are shown for faults at two different nodes (1,2) and with varying fault resistance (1Ω,3Ω). These results show that the proposed method estimates are very close to the ones from simulations. The maximum difference between the current magnitudes calculated by the proposed method and obtained from the simulations is 5.58%.

IV. CONCLUSIONS

This paper shows that the fault current profile on a SST dominated distribution feeder is considerably different than that of a conventional feeder. Both, the fault current contribution from SSTs and the voltage based protection schemes they employ, contribute to the variation of fault current. The paper proposes a new method that extends the conventional short-circuit analysis method and provides an estimate of the fault current profile. The simulation based test results indicate that the method provides quite accurate estimates.

Fig. 9. Test feeder - a sample SST-dominated feeder (circles indicate the node numbers).

Fig. 10. I-V curve of the simulated SST.

Fig. 11. Breaker current for three phase faults at node 2 on the sample distribution feeder.

Fig. 12. Breaker current for three phase faults at node 1 on the sample distribution feeder.

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