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This is the accepted version of a paper published in *IEEE Electron Device Letters*. This paper has been peer-reviewed but does not include the final publisher proof-corrections or journal pagination.

Citation for the original published paper (version of record):

Lanni, L., Malm, B., Östling, M., Zetterling, C. (2015)
Influence of Passivation Oxide Thickness and Device Layout on the Current Gain of SiC BJTs.
IEEE Electron Device Letters, 36(1): 11-13
<http://dx.doi.org/10.1109/LED.2014.2372036>

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N.B. When citing this work, cite the original published paper.

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Influence of passivation oxide thickness and device layout on the current gain of SiC BJTs

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Abstract—The effect of passivation oxide thickness and layout on the current gain of SiC bipolar junction transistors (BJTs) is reported. Different thicknesses of PECVD silicon dioxide in the range 50 to 150 nm were deposited prior to the same annealing process in N_2O , and their effect on the transistor gain was investigated for different device layouts. For a fixed device layout, approximately 60% higher gains were observed for oxide thicknesses ranging between 100 and 150 nm with current gains of approximately 200 at room temperature and larger than 100 at 300 °C. For each tested thickness of deposited oxide, device layout providing lower collector resistance achieved slightly higher gains.

Index Terms—Bipolar junction transistor (BJT), silicon carbide (SiC), current gain, deposited oxide, nitridation, surface passivation.

I. INTRODUCTION

Silicon carbide (SiC) bipolar junction transistors (BJTs) provide significant advantages for high-voltage and high-temperature applications due to their low on-resistance and to the absence of a sensitive gate oxide. Both applications benefit from high current gains (β). For high-voltage applications high gain BJTs provide reduced power losses in the base drive circuits. For high-temperature applications, instead, high gains could prevent performance degradation of analog and digital circuits in the range 27 to 300 °C where β exhibits a negative temperature coefficient [1]. Additionally, the possibility of improving the gain that can be achieved for a given epitaxial design could allow developing complementary technologies capable of high gain NPN and PNP transistors. As discussed in [1], a high base doping yields high gain lateral PNP transistors but at the same time limits the gain of NPN transistors.

Several studies have demonstrated a strong influence of surface passivation on the gain of SiC BJTs [2], and various passivation processes have been reported based on thermally grown or on deposited oxides and high-temperature treatments [3], [4]. Ghandi et al. [3] have compared passivation processes consisting in thermally grown oxides and in high-temperature annealing of deposited SiO_2 . The highest gain (~ 40) was reported for post-deposition annealing in N_2O (at 1100 °C for 3 hours) of 50 nm of PECVD SiO_2 . Whereas Miyake et al. [4] have demonstrated the impact on BJT current gain of

continuous growth of base and emitter epitaxial layer and of various post-deposition annealing processes of a fixed deposited oxide thickness. With 80 nm of PECVD SiO_2 annealed for 30 min in NO current gains of ~ 102 and 256 were reported for discontinuous and continuous epitaxial growth, respectively. In both cases the high gain was also attributed to a deep-level-reduction process performed prior to the passivation and consisting of two 5 hour-long oxidation processes at 1150 °C with an activation anneal process at 1800 °C in-between. However, in [4] only nominal values of base doping and thickness are reported, with no estimation of the actual intrinsic base sheet resistance.

In this letter the effect of device layout and thickness of the PECVD silicon dioxide deposited before the same N_2O annealing process on the gain of low-voltage SiC BJTs is investigated. In agreement with what has been reported for the mobility of 4H-SiC MOSFETs [5], the important role played by oxide thickness is proven.

II. DEVICE FABRICATION

Three different thicknesses of PECVD silicon dioxide were tested on one 100 mm 4H-SiC wafer, whose epitaxial structure is shown in Fig. 1. It consists of a 300 nm thick Al doped ($\sim 5 \times 10^{17} \text{ cm}^{-3}$) base layer and 4 other layers that allow designing NPN transistors suitable for low-voltage integrated circuits (i.e. -15 V supply voltage).

The emitter mesa was defined by means of inductively coupled plasma etching (ICP), while base and collector mesas were defined by means of reactive ion etching (RIE) [6]. After a dry sacrificial oxidation process (3 hours at 1100 °C), the wafer was cut into quarters and on three of them different thicknesses of silicon dioxide were first deposited by PECVD and then annealed at 1250 °C for 1 hour in N_2O . After the passivation process all quarters were processed in the same way up to the second metal layer. More process details can be found in [1] and [6].

III. RESULTS AND DISCUSSION

For each quarter wafer the current gain of minimum 30 transistors from various dies and with different emitter sizes was measured at 27 °C versus the collector base voltage (V_{CB}). In addition, the intrinsic base sheet resistance $R_{sh,IB}$ was extracted by means of transfer length method (TLM) measurements performed with a 4-point probe technique on at least 3 dies per quarter wafer.

Statistical comparisons of measured peak current gain (at 27 °C and $V_{CB} = 0V$) and intrinsic base sheet resistance are

shown in Fig. 2. Although the three quarters exhibit similar values of $R_{sh,iB}$ (see Fig. 2 (a)), devices with 100 and 150 nm of PECVD SiO_2 exhibit much higher gains, ~ 200 , than the devices passivated with 50 nm of oxide, for which measured gains are ~ 125 (see Fig. 2 (b)). The fact that the tested oxide thicknesses result in significantly different transistor gains suggests that the oxide thickness plays an important role in the passivation of SiC BJTs. In order to compare the performance of the tested devices independently of variations in doping and/or thickness of the base layer the ratio between peak current gain and intrinsic base sheet resistance ($\beta_{max}/R_{sh,iB}$) was used instead of the absolute gain [6]. As shown in Fig. 2 (c), devices with thicker deposited oxides exhibit almost 60% higher values of $\beta_{max}/R_{sh,iB}$ compared to devices with 50 nm of deposited oxide. The higher gains observed for deposited oxides in the range 100 to 150 nm can be attributed to lower surface recombination at the SiC/ SiO_2 interface as suggested by the Gummel plots shown in Fig. 2 (d). Although the collector currents of the three BJTs are similar, smaller base currents can be observed for thicker deposited oxides. In addition, the current gain plots of 3 sets of BJTs collected in Fig. 3, which correspond to three different layouts each one tested with 50, 100 and 150 nm of deposited oxide, show a similar impact of the oxide thickness on the transistor gain independently of device layout and size. For each set not only different peak current gains can be observed but also different gains in the low current region. As discussed in [7] and [8], this can be related to different surface recombination at the SiC/ SiO_2 interface and/or different interface recombination at the base-emitter junction. Since the devices were fabricated on the same wafer the different gains can likely be related to different surface recombination and, hence, to the different thicknesses of the passivation oxide. Furthermore, in agreement with what has been reported in [5] and [9] depositing thicker oxides could provide a better balance between nitridation and oxidation process during the N_2O annealing due to a lower oxidation rate. According to the model proposed in [9], during the N_2O annealing of deposited SiO_2 oxidation and nitridation take place simultaneously. The oxidation releases carbon, while the nitridation passivates dangling Si bonds and removes excess carbon due to the oxidation; and the balance between these two mechanisms can affect the quality of the SiC/ SiO_2 interface. In particular in [5] it has been shown that the channel mobility of 4H-SiC MOSFETs passivated with deposited SiO_2 annealed in N_2O is maximized when a certain increase in oxide thickness is obtained after the annealing, and that for a fixed annealing temperature this optimum increase depends not only on the annealing time but also on the thickness of the deposited SiO_2 .

Measurement results displayed in Fig. 3 also show that for each tested oxide thickness and for the same collector-base voltage (V_{CB}) transistors with triple-sided collector contact achieve higher gains due to their smaller collector resistance. Such an impact of the collector resistance on the transistor gain is confirmed by the slightly different peak gains observed for the same device when different collector-base voltages were applied. As shown in Fig. 4, increasing V_{CB} delays the

gain drop at high collector currents (observed for $V_{CB} = 0V$) and increases the peak gain by delaying the internal forward biasing of the base collector junction and by reducing the electrical base width of the transistor. It has to be noted that the BJTs in Fig. 3 not only differ in collector resistance value but also in base resistance value, R_B . In particular, the highest and the lowest value are achieved by the devices in Fig. 3 (a) and (c), respectively. Since all the three layouts use double- or triple-sided base contact and the same distance between base contact and emitter mesa edge the different R_B values are expected to have a negligible impact on the current gain and to mainly affect the collector current at the peak gain. Specifically, for the devices passivated with 50 nm of oxide higher R_B values shift the peak gain towards lower collector currents, whereas almost no difference is observed for the transistors passivated with 100 or 150 nm of oxide because of their higher gains, which result in lower base currents.

The transistor current gain was also investigated up to 300 °C. As shown in Fig. 5 BJTs with different thicknesses of deposited oxide exhibit similar temperature dependences of the current gain with a negative temperature coefficient, which can be related to the increasing amount of ionized acceptor dopants in the base layer. Nevertheless, thanks to the high room-temperature gain, oxide thickness in the range 100 – 150 nm allows current gain larger than 100 at 300 °C, which could significantly improve the performance of high-temperature SiC bipolar integrated circuits, especially for analog applications [10].

IV. CONCLUSION

The impact of passivation oxide thickness on the current gain of 4H-SiC BJTs has been investigated by varying the thickness of the PECVD silicon dioxide between 50 and 150 nm before performing a 1 hour annealing in N_2O at 1250 °C. Furthermore, the effect of device layout on the current gain has been evaluated by testing transistor layouts resulting in different collector resistances. Independently of device area and layout, oxide thicknesses ranging between 100 and 150 nm provided approximately 60% higher peak gains than those obtained by depositing 50 nm of oxide. While for the same oxide thickness, devices with lower collector resistances achieved slightly higher gains.

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Figure 1 Cross-sectional view of the fabricated BJTs.

Figure 2 Statistical comparisons of measured intrinsic base sheet resistance (a) and peak current gain (27 °C and $V_{CB} = 0$ V) of single-sided collector contact BJTs with different emitter sizes (b). Average ratio between peak gain and intrinsic base sheet resistance (c). Gummel plot of 3 BJTs with the same layout passivated with different SiO₂ thicknesses (d).

Figure 4 Current gain plots at 27 °C and different V_{CB} measured on a transistor with emitter size $24 \mu\text{m} \times 70 \mu\text{m}$ and single-sided collector contact passivated with 100 nm of deposited SiO₂.

Figure 3 Current gain plots (at 27 °C and $V_{CB} = 5$ V) of 3 sets of BJTs with different layouts passivated with different thicknesses of deposited SiO₂. Provided collector resistance values (extracted from measured output characteristics) refer to the BJTs passivated with 100 nm of deposited oxide.

Figure 5 Current gain temperature dependence of 3 BJTs (with emitter size $24 \mu\text{m} \times 70 \mu\text{m}$ and single-sided collector contact) passivated with different thicknesses of deposited SiO₂: 50, 100 and 150 nm.