Paper IV

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Fabrication of Relaxed Germanium on Insulator via Room Temperature Wafer Bonding

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We report on the fabrication of, high quality, monocrystalline relaxed Germanium with ultra-low roughness on insulator (GeOI) using low-temperature direct wafer bonding. We observe that a two-step epitaxially grown germanium film fabricated on silicon by reduced pressure chemical vapor deposition can be directly bonded to a SiO_2 layer using a thin Al_2O_3 as bonding mediator. After removing the donor substrate silicon the germanium layer exhibits a complete relaxation without degradation in crystalline quality and no stress in the film. . The results suggest that the fabricated high quality GeOI substrate is a suitable platform for high performance device applications.

Introduction

Traditionally an increase of the CMOS technology node performance and computing power has been strongly connected with the reduction of the CMOS field effect transistor dimensions. However, further scaling down the feature sizes of CMOS transistors coincides with a degradation of silicon carrier mobility. In recent years several interesting approaches have been investigated to address this challenge. A direct approach is the enhancement of the carrier mobility by means of introducing strain into the Si channel (1, 2). This idea has resulted in significant improvement and, hence, is now adopted into the CMOS process. A second approach is the usage of silicon on insulator (SOI) substrates which is considered extensively to improve the short channel effects and, thus, the device performance (3). Even further performance improvement can be achieved by entirely replacing the Si channel with high carrier mobility materials such as III-V semiconductors or germanium (Ge), the latter being considered as CMOS compatible. In particular Ge is of major interest as both electron and hole mobilities are considerably larger compared to Si (5). This has been recently verified in strained Ge-pFETs (4, 5). However, due to the lower band gap and higher dielectric constant of Ge, bulk Ge devices suffer from high leakage currents and short channel effects. Similar to the idea of using SOI substrates those could be suppressed by employing germanium on insulator (GeOI) substrates (6). Such GeOI substrates are fabricated similar to SOI structures using separation by oxide implantation (SIMOX) (7), Ge condensation, or wafer bonding.

The SIMOX technique is an implantation of oxygen ions below the surface of a substrate, followed by a high temperature annealing. This annealing heals the implantation-damaged top-layer and forms a buried oxide layer using the implanted oxide ions. However, this technique is limited to manufacture GeOI substrates with Ge

fractions up to 30% due to thermal instability during the high temperature annealing (8). The Ge condensation consists of SiGe epitaxy using SOI substrates. Here the Ge layer forms during an oxidation at high temperature whereby Ge atoms are repelled from the SiGe layer. As the Ge atoms cannot diffuse through the SiO_2 they condense at the remaining SiGeOI layer. The Ge layer will be relaxed due to the high temperature oxidation. Furthermore, the process generates high defect densities (9). More promising in this respect is wafer bonding due to its simplicity and potential for achieving high quality crystalline Ge layers (10). In addition the flexibility of this approach is beneficial as the different structures like SiOI, SiGeOI or GeOI can be generated. Commonly used methods in wafer bonding include: (i) grind and etchback, and (ii) SmartCut. In the first approach after the bonding the backside of the donor wafer is grinded and subsequently etched in a solution of KOH or tetramethylammonium hydroxide (TMAH). The SmartCut process starts with hydrogen implantation at a desired depth into the donor substrate. After the bonding process a high temperature annealing causes the donor wafer to separate at the hydrogen interface. Given that all layers are grown epitaxially and by utilizing etch stop layers the thickness of the transfer layers can be controlled precisely, allowing the fabrication of thin layers on insulators with both techniques (11). Nevertheless, these wafer bonding techniques require high temperature post-bond annealing undesired in the CMOS process. In addition, process requirements such as grinding, CMP and implantation complicate the bonding process (1, 10, 12).

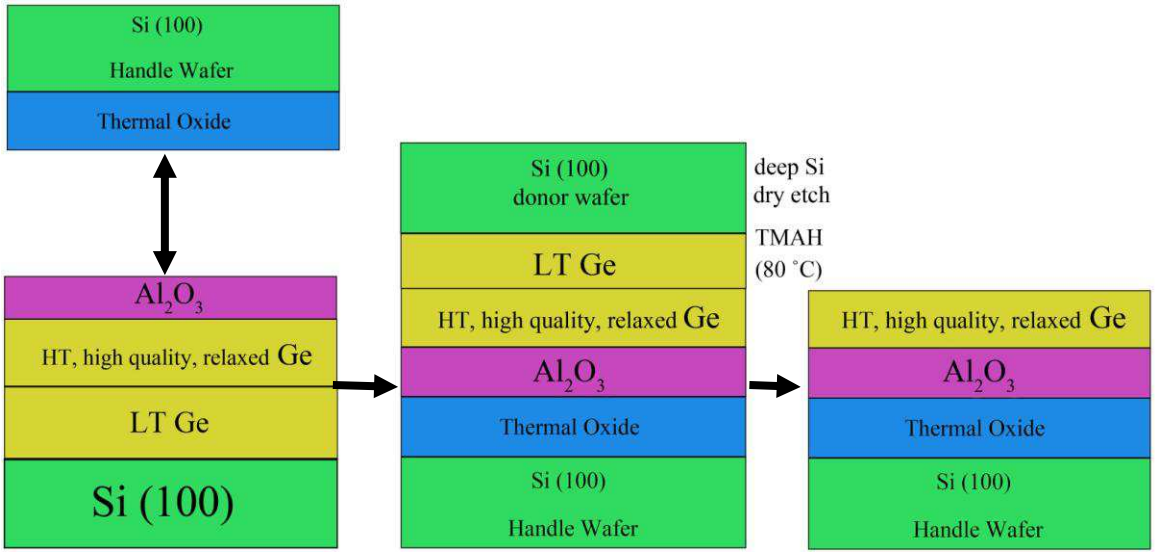
In this work we present a novel GeOIwafer bonding technique based on heteroepitaxy and layer transfer. We designed and fabricated GeOI substrates via wafer bonding and etch back process without intermediary chemical mechanical polishing (CMP) step. Low temperature bonding avoids strain relaxation, Ge diffusion and detaching due to thermal expansion coefficient differences.

Process flows and experiment

High quality relaxed Ge growth

The donor layer is epitaxially fabricated using reduced pressure chemical vapor deposition (RPCVD) Epsilon 2000 ASM reactor. Digermane Ge_2H_6 was used as Ge gas source. A standard n-type Si (100) wafer was used as a substrate. The substrate is pre-cleaned using a a mixture of sulphuric acid and hydrogen peroxide (H_2SO_4: H_2O_2 = 3: 1) followed by an 5% hydrofluoric acid dip.

The epitaxial process is illustrated in figure 1(a). Epitaxy is initialized with an in-situ anneal 1100 °C in H_2 atmosphere. Subsequently, around 100 nm of Ge is deposited at 400°C (LT-Ge). The low temperature results in the formation of a high amount of point defects effectively trapping misfit dislocations and threading dislocations which are caused by the lattice mismatch of 4.2% between Ge and Si. This layer is plastically relaxed inhibiting three-dimensional (3D) island nucleation due to a reduced surface diffusion of Ge atoms. Finally, a second Ge layer with a thickness of 530 nm, is grown at 720 ° (HT-Ge). This HT-Ge layer confines the dislocation formed in LT-Ge layer (13, 14). After the epitaxial growth we deposit 10 nm of Al_2O_3 by means of atomic layer deposition (ALD).



(a) (b)

Figure 1. Schematic image of the bond and etch-back process, (a) epitaxial growth, ALD deposition and bonding and (b) Dry and wet etches are used to remove Si substrate, exposing the relaxed high quality GeOI.

Wafer bonding

Figure 1(b) illustrates the bonding process where a Si (100) handle wafer with a 100 nm thick thermal oxide on top was utilized for bonding. Prior to bonding both samples were cleaned and prepared for low temperature direct bonding. The cleaning process consists of an etch in H_2SO_4 : H_2O_2 = 3: 1 followed by deionized water rinse for the handle wafer and acetone, isopropanol cleaning followed by deionized-water rinse for the donor wafer. The cleaning process yields a hydrophilic surface. This is crucial as stronger bonds can be obtained using hydrophilic surfaces during low temperature bonding (15). During the bonding Al_2O_3 and SiO_2 form a strong bond which can withstand polishing processes even without a post-bonding anneal (12). The strong bond of Al_2O_3/SiO_2 at the interface proceeds the following reaction (12):

$$Al\text{-}OH + Si\text{-}OH \rightarrow Al\text{-}O\text{-}Si + H_2O$$

Compared to other wafer bonding processes this direct approach offers the advantage that no adhesive or additional material is used between the surfaces. In addition, direct bonding is compatible with CMOS standard process and any stacked structure can be manufactured using this approach. Furthermore, the bonding interface is reported to withstand high temperature processes (12).

Back-side thinning

Finally, the HT-Ge layer is exposed using back-side etching. Using Applied Materials Centura II deep trench Si the Si substrate of the Ge donor wafer was etched reducing the thickness of the donor wafer own to a value of about 200 µm. The remaining Si on the backside of the donor wafer was then selectively removed by employing a 5% TMAH

solution at 90°C. This highly selective etch removes Si and the LT-Ge. We would like to highlight that the HT-Ge acts as an efficient etch stop simplifying the process significantly. The final structure is depicted in figure 1(c) and consists of the HT-Ge layer on top of the Al_2O_3-SiO_2 bonding interface.

Results and discussion

The Ge sample roughness was characterized using atomic force microscopy (AFM) in tapping mode. The thickness of the Ge layer was measured by cross-sectional scanning electron microscopy and the result was compared with spectroscopic ellipsometry and AFM step height measurements. Raman spectroscopy in back-scattering technique was employed using the 514.5 nm line of an Ar-Ion laser. The back scattered light is spectrally dispersed using a double monochromator and detected using an InGaAs CCD line array. Hall measurements are determined at room temperature using a 4 T magnet.
Figure 2 shows a 3D AFM image of the HT-Ge surface prior to bonding. We obtain a root mean square (RMS) surface roughness of approximately 0.3 nm. This is of particular importance as the direct bonding process requires a very high surface quality with an RMS value lower than 1 nm [15].

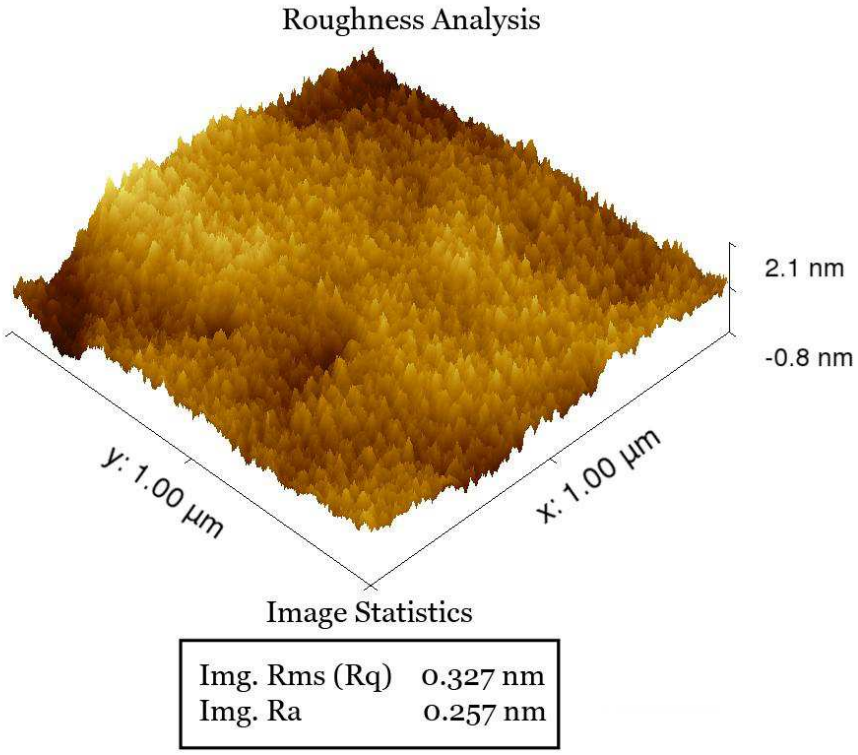


Figure 2. AFM image of the epitaxial Ge layer on Si substrate.

The surface morphology of the GeOI surface after etch-back is shown in Fig 3. An RMS value of approximately 0.3 nm has been extracted which is slightly higher than for the unetched surface. However, the wet chemical etch-back does not significantly decrease the surface quality allowing the usage of the here presented GeOI manufacturing process for high performance devices.

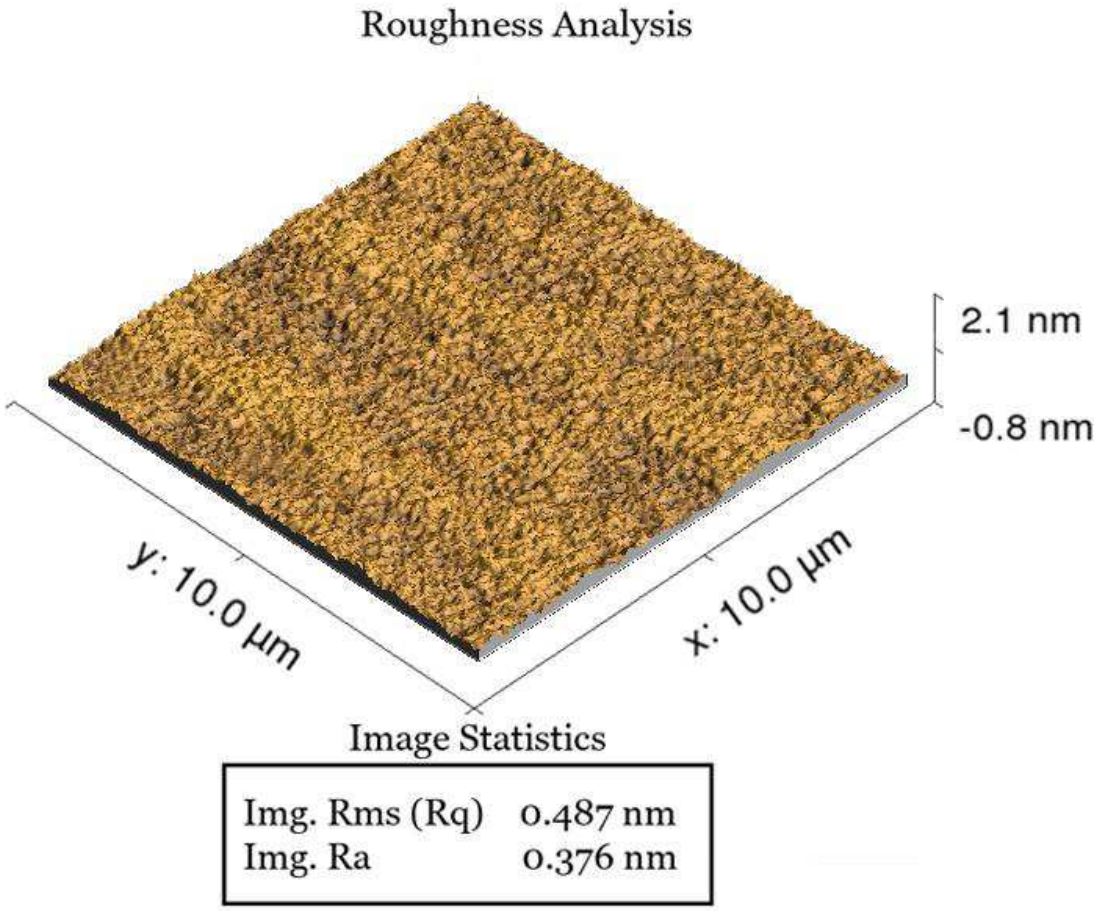


Figure 3. AFM image of the GeOI sample after etch-back process.

Figure 4 shows a cross sectional SEM image of the GeOI top layer. The images yield a layer thickness of approximately 650 nm which is in nice agreement with our ellipsometry measurements (not shown here). The layer thickness we determine here is the sum of the LT-Ge and HT-Ge. Hereby the LT-Ge has a larger thickness of approximately 110nm. The HT-Ge is approximately 530nm thick. The HT-Ge layer is not subject to any limitations and could be altered to meet device requirements. In addition we would like to highlight that not undulations or bulging is visible at the top surface.

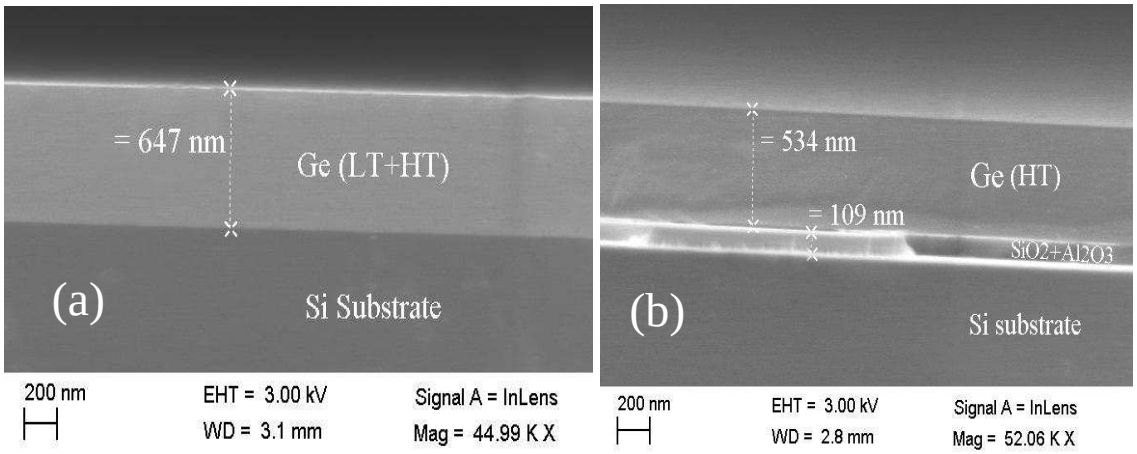


Figure 4. SEM images of (a) the Ge layer thickness after epitaxy consisting LT and HT Ge on Si substrate, and (b) Ge on insulator after etch-back process which only consists of HT Ge layer.

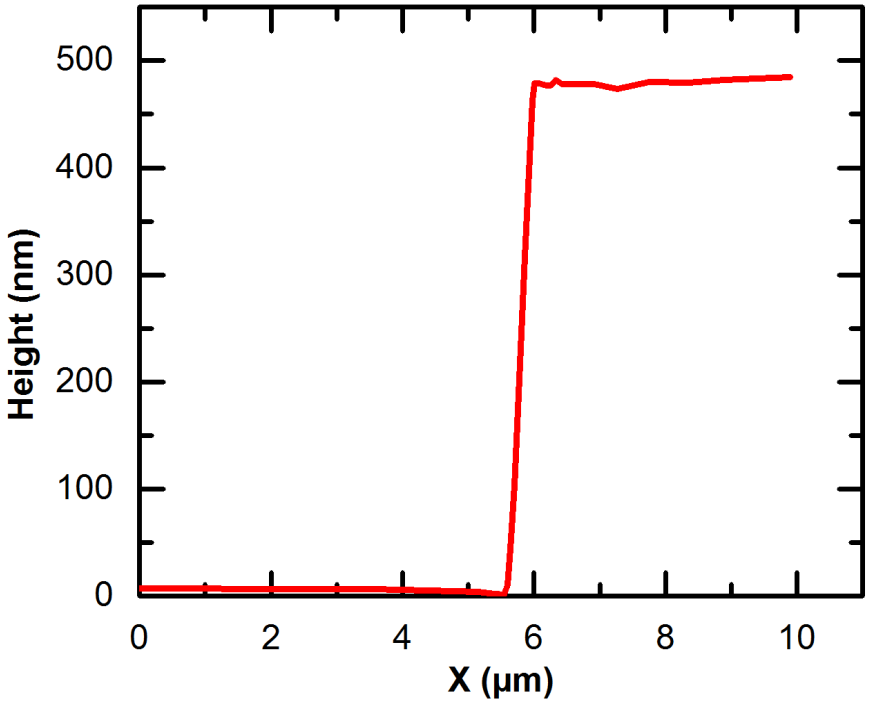


Figure 5. AFM step height measurement of the GeOI layer

The thickness of our HT-Ge layer after etch back has been precisely measured using AFM (Figure 5). We obtain at thickness of 500 nm which is in very good agreement with previous measurements from SEM. Considering the GeOI thickness we conclude that the LT-Ge buffer has been removed by TMAH solution during etch-back. Moreover, we find that the HT-Ge buffer acts as an efficient etch-stop strongly simplifying the fabrication process.

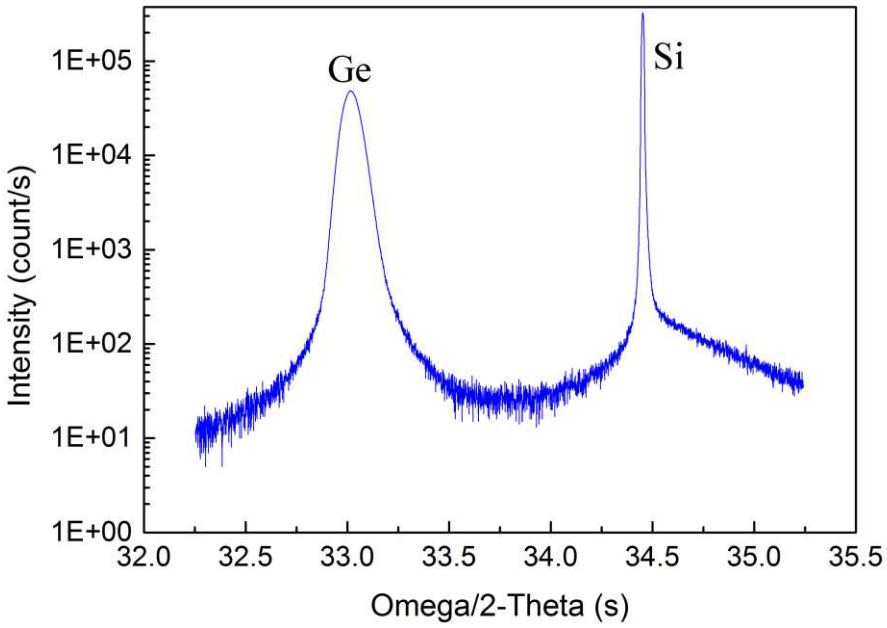


Figure 6. XRD Ω-2θ scan around (004) of Ge on insulator

Fig.6 shows the high resolution x-ray diffraction (0 0 4) rocking curve of a GeOI substrate. We find two peaks at approximately 33 sec stemming from the Ge and at 34.5 sec stemming from the Si substrate. The Ge peak nicely coincides with the expected Ge (004) position indicating a very high degree of relaxation and purity. Moreover, no asymmetry is visible indicating that Si atoms have not interdiffused into the Ge layer.

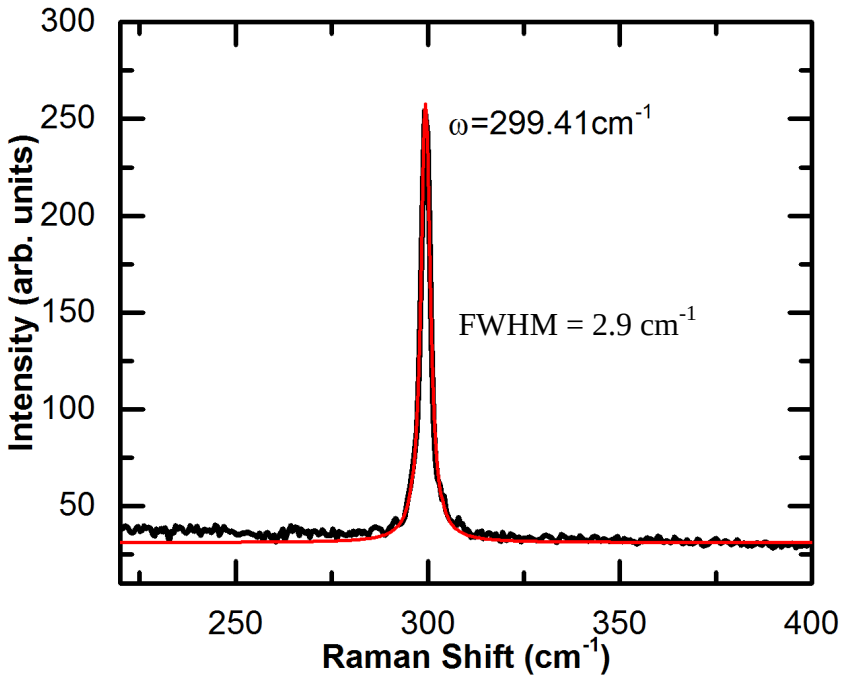


Figure 7. Raman spectrum of the final GeOI sample.

In order to examine the stress and crystalline quality of the final Ge film, a Raman spectroscopy was performed on GeOI sample. Figure 7 shows the Raman spectroscopy spectrum with a narrow longitudinal Ge optical phonon peak at approximately 300 cm^{-1} with a full width of half maximum (FWHM) of 2.9 cm^{-1}.The Raman shift was compared to bulk Ge (16) and exhibits no frequency shift and, therefore, no strain. In addition, the full width half maximum of our peak is similar to the reference value of 5.3cm^{-1} indicating a high crystal quality.

For any device applications the electrical properties of the Ge film are crucial and have been assessed using hall measurements. The intrinsic hall mobility on the GeOI sample $\mu = 580$ (cm^2/Vs) and the background doping is p-type. This is still about a factor of 4 lower than literature values (17) but we expect that further improvements of the growth conditions and the bonding process can improve this value.

Conclusions

In summary, we have shown a novel process scheme for the development of ultra-low surface roughness, monocrystalline, relaxed GeOI substrate using direct low temperature wafer bonding. The bonding process is performed at an Al_2O_3-SiO_2 interface. The two-step Ge epitaxial growth yields a high quality Ge film with a surface roughness less than 0.5 nm which is maintained even after exposure. The GeOI film exhibits neither stress nor any degradation in crystalline quality. Further development of the epitaxial process and the bonding is expected to result in an improved Hall mobility making this substrate an interesting platform for the future scaled technology nodes.

Acknowledgments

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