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Improved Low-frequency Noise for 0.3nm EOT Thulium Silicate Interfacial Layer

Maryam Olyaei, B. Gunnar Malm, Eugenio D. Litta, Per-Erik Hellström, and Mikael Östling

KTH – Royal Institute of Technology, Integrated Devices and Circuits,

School of Information and Communication Technology P.O. Box 229, SE-16440 Kista, Sweden, olyaei@kth.se

Abstract—Low-frequency noise (LFN) of gate stacks with Tm_2O_3 high-k dielectric and thulium silicate (TmSiO) interfacial layer (IL) is investigated. The measured $1/f$ noise is compared to $\text{SiO}_x/\text{HfO}_2$ stacks with comparable IL thickness. Integration of a high-k thulium silicate IL provides a scaled EOT of 0.3nm with good mobility and interface quality and hence excellent LFN is obtained. The LFN noise for devices with $\text{TmSiO}/\text{Tm}_2\text{O}_3$ gate dielectric is reduced for nMOSFETs and comparable for pMOSFETs compared to $\text{SiO}_x/\text{HfO}_2$ devices.

Keywords— Low-frequency noise; high-k dielectric; interfacial layer; Thulium silicate; MOSFET

I. INTRODUCTION

High-k dielectrics have enabled downscaling required in complementary metal-oxide-semiconductor (CMOS) technology by offering high capacitance density while keeping the gate leakage low. Implementing the high-k dielectric directly on the silicon layer provides aggressively scaled equivalent oxide thickness (EOT), but it is challenging not to degrade mobility and reliability due to poor interface with silicon. Therefore, dual layer dielectric stacks have been introduced containing a high-k layer and an interfacial layer (IL) providing both low EOT and good interface quality with silicon [1][2][3]. The most commonly used materials as ILs are SiO_x , SiON and HfSiON among which SiO_x offers great interface with silicon and together with HfO_2 as high-k dielectric ($k = 17\text{-}30$) creates a suitable dual layer dielectric stack [4][5]. Scaling SiO_x IL thickness below 0.4nm is challenging to achieve as thinner IL leads to mobility and reliability issues. Further scaling of IL EOT can potentially be achieved by the introduction of ILs with higher dielectric constants such as silicates [6][7][8]. We have previously demonstrated that thulium silicate (TmSiO) can be integrated in $\text{TmSiO}/\text{HfO}_2$ gate stacks achieving low $D_{it} \sim 2 \cdot 10^{-11} \text{ cm}^{-2} \text{ eV}^{-1}$, sub-threshold slopes $< 80 \text{ mV/dec}$ and 15-20 % enhanced mobility for p and nMOSFETs compared to $\text{SiO}_x/\text{HfO}_2$ at sub 1 nm EOT [9].

Previous studies have shown that the thickness of the IL layer has a high impact on the level of LFN [1] [4] [10]. In this paper we evaluate the low-frequency noise (LFN) in devices with TmSiO IL EOT of 0.3 nm and compare to state-of-the art LFN in published $\text{SiO}_x/\text{HfO}_2$ devices. This work is different from benchmark studies where HfO , ZrO and ALO and layered combination of these have been used as gate materials [11]

[12]. Few studies have been reported on intergration of Tm_2O_3 as high-k dielectrics in MOS devices [7] and as capping layer for La_2O_3 gate stacks [13]. No studies have been published on $1/f$ noise of Tm_2O_3 yet, to the best of the author's knowledge.

In section II the device fabrication steps are described. In section III, experimental details are explained. The results are reported and discussed in section IV. Finally, the work is concluded in section V.

II. FABRICATION

The nMOS and pMOS devices were fabricated on 100 mm p-type (100) Si wafers. The fabrication was performed in a gate last process. A dummy gate was deposited, after isolation and well formation ($N_{\text{well}} = 10^{17} \text{ cm}^{-3}$). Then, source and drain were implanted and active areas were patterned. The process was continued after dummy gate removal by deposition of Tm_2O_3 at 250°C in ALD. TmCp_3 and H_2O were used as precursors and Ar as carrier gas in Beneq TFS 200 system. The deposition was followed by rapid thermal annealing (RTA) at 550°C in N_2 resulting in formation of TmSiO . The unreacted Tm_2O_3 was kept as top dielectric.

Fig. 1. Gate stack schematic of the investigated devices. The TmSiO is grown as an IL layer with 0.9 nm physical thickness (EOT=0.3 nm). Tm_2O_3 is the bulk high-k layer with 3.5 nm physical thickness (EOT=0.9 nm). Total EOT of $\text{TmSiO}/\text{Tm}_2\text{O}_3$ is 1.2 nm.

PVD TiN gate metal was deposited in the next step followed by passivation and contact hole patterning. The extra TmSiO was etched away in HF 1%. Finally PVD Ti/TiW/Al (10/100/100 nm) stack was deposited and patterned as contacts followed by FGA (10% H₂ in N₂) at 400°C for 30 min [9]. The gate stack composition of these devices is depicted in Fig. 1. TmSiO is the interfacial layer with 0.3 nm EOT (0.9nm physical thickness) and Tm₂O₃ on top is the bulk high-k with 0.9 nm EOT (3.5 nm physical thickness).

III. EXPERIMENTAL

Low-frequency noise measurements were performed on nMOSFETs and pMOSFETs with $W=10\mu\text{m}$ $L=3$ and $L=10\mu\text{m}$ at $|V_{DS}|=100\text{ mV}$ and $|V_{GS}-V_t|$ ranging from 0V to 0.3V using a spectrum analyzer and a Programmable Biasing Amplifier (PBA) with an external low noise power supply. Long channel devices were selected for noise measurement as they have channel resistance larger than S/D resistances. During noise measurements V_G was limited so that the drain current was always at least one decade larger than the gate current.

The DC properties of these devices such as gate leakage, transconductance g_m and threshold voltage V_t were extracted with a Keithly 4200-SCS parameter analyzer. The devices show well behaved I_D-V_G with an average threshold voltage of 0.4V for nMOSFETs and -0.8V for PMOSFETs.

Fig. 2 shows I_D-V_G of an nMOSFET and pMOSFET with $W=10\mu\text{m}$ and $L=3\mu\text{m}$ with $V_{tn}=0.37\text{V}$ and $V_{tp}=-0.68\text{V}$ in the linear region. The subthreshold slope is $\sim 70\text{ mV/dec}$ which is close to the ideal subthreshold for well doping density of 10^{17} cm^{-3} and CET of 1.6 nm.

Fig. 2. I_D-V_G on nMOSFET and pMOSFETs with $W \times L=10 \times 3\mu\text{m}^2$, $V_{DS}=50\text{ mV}$.

IV. RESULTS AND DISCUSSION

The typical noise spectrum of an nMOSFET and a pMOSFET are shown for a frequency range between 1-10⁴ Hz in Fig. 3. The spectrum is shown for gate voltage overdrive of 0.2V at fixed drain voltage of 100 mV for nMOSFETs and -100mV for pMOSFETs. The noise spectra of all measured devices show $1/f^\gamma$ behavior which γ varies between 0.8 and 1.1.

The normalized drain noise data at $f=10\text{Hz}$ over drain current is shown in Fig. 4 for 3 different nMOSFETs. On the second y-axis, $(g_m/I_d)^2$ is depicted in solid line where g_m is the transconductance. It is shown that the normalized noise follows the same trend as $(g_m/I_d)^2$ for nMOSFETs (Fig. 4. (a)). This verifies that the carrier number fluctuations are the major source of noise in these devices [14].

Fig. 3. LFN versus frequency for nMOSFET with $W \times L=10 \times 10\mu\text{m}^2$ and $V_{DS}=100\text{ mV}$, amplifier gain= 10^{-6} (A/V) (a), pMOSFETs with $W \times L=10 \times 3\mu\text{m}^2$ and $V_{DS}=-100\text{ mV}$, amplifier gain= 10^{-5} (A/V) (b).

However, in Fig. 4. (b) for pMOSFETs, the S_{ID}/I_D^2 curve does not seem to follow $(g_m/I_D)^2$ closely. This implies that the source of noise might be different in these devices. To clarify this, the normalized drain current noise is plotted over gate voltage overdrive and shown in Fig. 5. It is observed that S_{ID}/I_D^2 curve shows a slope of $1/(V_{GS}-V_t)$ which confirms that the dominant noise mechanism the unified correlated number and fluctuation model [15].

Fig. 4. Normalized drain current spectral density (marked as blue circles) and $(g_m/I_d)^2$ (marked solid line) over drain current for n-MOSFET with $W \times L = 10 \times 10 \mu m^2$, $V_{DS} = 100$ mV and $f = 10$ Hz (a) and p-MOSFET with $W \times L = 10 \times 3 \mu m^2$, $V_{DS} = -100$ mV and $f = 10$ Hz (b). nMOSFETs follow $(g_m/I_d)^2$ closely.

In Fig. 6. the normalized drain current spectral density is shown versus gate voltage overdrive for nMOSFETs (a) and pMOSFETs (b). The low frequency noise has been measured for several devices all over the wafer with TmSiO/Tm₂O₃ gate stack. These data is shown with different symbols for three devices in the figure.

Fig. 5. Normalized drain current spectral density (marked as blue circles) at $f = 10$ Hz and $V_{DS} = -100$ mV over gate voltage overdrive for pMOSFETs with $W \times L = 10 \times 3 \mu m^2$.

Fig. 6. Normalized drain current spectral density (marked as blue circles) versus gate voltage overdrive at $f = 10$ Hz for TmSiO/Tm₂O₃ nMOSFETs with $W \times L = 10 \times 10 \mu m^2$ (a) and pMOSFETs with $W \times L = 10 \times 3 \mu m^2$ (b) and reference SiO_x/HfO_2 with $W \times L = 10 \times 1 \mu m^2$ [4].

A variation is observed in the measured $1/f$ noise but overall, the level of noise is reduced comparing the results of nMOSFETs to a reference $\text{SiO}_x/\text{HfO}_2$ gate stacks with a comparable EOT IL (0.4nm). PMOSFETs generally show slightly higher noise level comparing to nMOSFETs with $\text{TmSiO}/\text{Tm}_2\text{O}_3$ gate stack, but the $1/f$ noise is comparable to reference $\text{SiO}_x/\text{HfO}_2$ with IL EOT=0.4nm.

In Fig. 7. The normalized drain current spectral density versus interfacial layer EOT is depicted. Benchmark data from different $\text{SiO}_x/\text{HfO}_2$ studies are included in the graph. A trend versus IL EOT can be illustrated with the fitting line shown in the plot. It is observed that S_{I_D}/I_D^2 increases with decreasing interfacial layer thickness. The $\text{TmSiO}/\text{Tm}_2\text{O}_3$ nMOSFETs with 0.3nm EOT of IL show a level of noise which is lower than a SiO_x interfacial layer with the same thickness. In fact, the level of noise of these devices is comparable to SiO_x IL with thickness of 1nm.

Fig. 7. Normalized drain current spectral density versus IL EOT for reference nMOSFET $\text{SiO}_x/\text{HfO}_2$ samples [1] [4] and for $\text{TmSiO}/\text{Tm}_2\text{O}_3$ nMOSFET at $f=10\text{Hz}$.

V. CONCLUSION

Low frequency noise of nMOSFETs and pMOSFETs with 0.3nm thulium silicate interfacial layer and thulium oxide high-k has been investigated experimentally. This is the lowest IL EOT that has been reported in low-frequency noise characterization. The results suggest that applying the high-k thulium silicate interlayer can provide low EOT while preserving good electrical interface quality with Si. The comparison of measured LFN noise of these devices with comparable EOT SiO_x IL shows improved level of $1/f$ noise for nMOSFET and comparable $1/f$ noise for pMOSFETs.

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