Development of Through Glass Vias (TGVs) for Interposer Applications

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Master’s Degree Project

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Abstract

In this thesis work the manufacturing of through glass vias (TGVs) is presented. The TGVs were manufactured by adapting technique based on magnetic assembly developed at KTH for creating through silicon vias (TSVs). TGVs were fabricated by introducing nickel wires in via-holes that were pre-made on a glass substrate and applying a spin-on polymer to isolate the nickel wires from the walls of the via-holes.

Another focus of this work was improving the TGV and TSV manufacturing process. This was done by investigating the influence of the assembly speeds on the yield of the assembly process. Two methods for removing the excess wires left on the surface of the wafer after the magnetic assembly of the nickel wires were tested. Also the influence the pitch between the via-holes has on the yield of the process was investigated.
## Contents

1 Introduction ................................................. 4  
  1.1 Problem Statement and Goals ............................. 5

2 Background .................................................. 7  
  2.1 Through-Via Fabrication ................................. 7
  2.2 Magnetic Assembly of Through-Vias ..................... 9
  2.3 Through Glass Vias (TGVs) ............................. 10

3 TGV Fabrication ............................................ 12  
  3.1 Nickel Wire Stud Fabrication ............................ 13
  3.2 Magnetic Assembly of the Nickel Wires in the Via-Holes 15
  3.3 The 400F Spin-on Glass ................................. 17  
    3.3.1 Spin-on Glass Deposition and Baking .............. 18
  3.4 TGV Fabrication Results ............................... 19  
    3.4.1 Silicon Wafer Tests ............................... 20
    3.4.2 Glass Wafer Tests .................................. 21

4 Assembly Tests and Improvements .......................... 24  
  4.1 Array Density ........................................... 24
  4.2 Excess Wires ........................................... 26
  4.3 Wires with and without Burrs ........................... 28

5 Conclusion .................................................. 32  
  5.1 Improvements ............................................ 33

6 Appendix A - 400F Spin-on Glass Properties .............. 36
Chapter 1

Introduction

Today’s trend in the field of electronics is to decrease the size while increasing the performance of integrated circuits (ICs) and systems. A method to achieve this is by building 3D ICs. This is done by stacking two or more levels of electronic components vertically in order to reduce the footprint. In Figure 1.1, the principle behind 3D ICs and the considerable reduction in the dimensions of the footprint can be seen. Besides a reduction of the IC volume, 3D integration comes with the advantage of shorter signal paths, leading to smaller parasitic capacitances, faster signal speeds and a reduction of power consumption [1].

![Different methods of packaging ICs](image)

*Figure 1.1: Different methods of packaging ICs, ranging from the flipchip and wire-bond (left) to the 2.5D side-by-side integration with TSVs and silicon interposer (center) and the 3D vertical stacking (right).*

An interposer represents an electrical interface that connects multiple electrical connections. They are used in order to minimize the footprint of a device. Active
dies are placed on the interposer and the connections are made with the help of the through-vias present in the interposers. The use of interposers is referred to as 2.5D-IC. An advantage of using interposers is that wirebonds are eliminated, thus minimizing the volume of the device and also because they are not driving wirebonds to on-board (PCB) connections, transistor may be smaller. Another advantage is that heat buildup experienced in full 3D-IC designs may be minimized [2].

Although silicon is the most common material used for manufacturing interposers, glass represents a good alternative for interposer fabrication. Glass is a composite of different substances with properties depending on its specific composition. Because of this, glass can be created with tailored electrical and mechanical properties for a specific application [3]. The most obvious advantage that glass has over silicon is that it is transparent, making it an ideal material for optical applications such as concentrated solar photovoltaics [4] or LED modules. Other advantages are very good dielectric characteristics such as having a smaller dielectric constant, between 3.7 and 10 in comparison with silicon which has a dielectric constant between 11 and 12 and being a very good insulator [5].

The work in this master thesis is performed with focus on developing a novel method for manufacturing functional TGVs. The work is based on the method that was previously developed at KTH [6] for manufacturing TSVs. The main feature of this technique is to use an assembly robot to fill a chip, containing via-holes, with nickel wires providing very good control and repeatability characteristics. The second step represents the filling of the assembled via-holes with an organic dielectric called bisbenzocyclobutene (BCB)[7].

Another focus of this master thesis is to improve the through-via fabrication process by enhancing the assembly speed of the conductive cores of the vias as well as investigating the effects the pitch between the via-holes and the excess wires left onto of the sample have on the yield of the process.

1.1 Problem Statement and Goals

The aim of the project is, first, to successfully fabricate reliable TGVs, by adapting the technique for nickel TSV fabrication developed at KTH [6], and second, to analyze and improve this method of creating both TGVs and TSVs.

This work is based on the magnetic assembly of nickel wires developed previously at KTH. TSVs are manufactured by introducing a conductive nickel wire in a pre-made via-hole by exploiting the ferromagnetic properties of nickel. A robot arm is used to hold and move a magnet in a specific predetermined trajectory [6] in order to assemble nickel wires in the via-holes. After the nickel wires are assembled, an insulator is deposited between the nickel wires and the walls of the via-holes through capillary filling. A drawback of this technique is the slow speeds of creating TSVs along with the limited research done on the influence of the pitch of the holes on the yield of the process.

The main goal of the project is to successfully fabricate TGVs on a glass sub-
strate with arrays of 20x20 via-holes with a diameter of 50 µm, using the same nickel wires but a different insulator, namely 400F spin-on glass (SoG) (Filmtronics Inc., USA). Spin-on glass was chosen as a replacement for BCB because it has very similar attributes as the glass substrate, such as transparency, mechanical properties and dielectric characteristics. The project also investigates the differences of assembling the nickel wires on dense and on spread 10x10 arrays of via-holes, of different diameters starting from 40 µm up to 55 µm and the excess wires left on top of the arrays after the assembly. Another goal is to further improve the magnetic assembly process by reaching 100% of via-holes assembled in a shorter amount of time in comparison with previous work.
Chapter 2

Background

In this chapter, relevant information is provided to the reader regarding TSVs and, more importantly, TGVs. Finally, a characterization of the magnetic assembly process is also included.

2.1 Through-Via Fabrication

The function of a through-via at any level or through any material, be it glass or silicon, is to establish an electrical connection between 2 different electrical layers. In this report through-vias at wafer level will be discussed. A basic through-via has a simple design; it is composed of a hole through the substrate, a conductive material used as a core and an insulator used to separate the core from the substrate. The fabrication process of the through-via and its design vary on the target application.

Figure 2.1: Typical process flow for creating TSVs or TGVs. Each block represents the steps and the most common methods used.
The process of manufacturing both TGVs and TSVs is very similar. In Figure 2.1 the typical method as used by the industry is presented.

This method starts by manufacturing the via-holes through the substrate. This can be done in many ways but the most common ones are dry etching, namely Deep Reactive Ion Etching (DRIE) [8, 9], wet etching [8], mechanical through drilling or powder blasting [3]. The next step commonly consists of applying an insulating layer to effectively separate the conductive core from the substrate. The two main concepts of achieving this are by Chemical Vapour Deposition (CVD) of the desired inorganic material [10, 11] or organic dielectrics [12]. Next, the conductive core of the via is introduced. This process is problematic because it is the primary restrictive factor of the via dimensions. The main material used to create these conductive cores is copper [8, 9] although other materials such as tungsten [11], polysilicon [11] and low-resistivity silicon are also used. Copper is usually deposited through electroplating techniques. Electroplating possesses problems in achieving reliable through-vias because it is difficult to fill high-aspect ratio TSVs with void-free cores. The final stage consists of additional processing such as surface grinding and polishing.

![Figure 2.2: Process developed at KTH for manufacturing TSVs. The Core deposition stage is switched with the insulator deposition stage in comparison with the typical process used in industry.](image)

The process flow for manufacturing through-vias developed at KTH is presented in Figure 2.2. The first step is to fabricate the via-holes through the silicon substrate. This is realized through a DRIE process. The second step consists of magnetically assembling nickel wires inside the via-holes. Next, the insulation stage is performed. BCB was used as the organic dielectric for this step. The difference between the typical method used in industry and the process developed at KTH is that the depositing insulator and core deposition stages are switched. This is due to the fact that in the KTH method nickel wires are used as the conductive core of the via instead of electroplating copper.
2.2 Magnetic Assembly of Through-Vias

In this thesis work, the process of assembling a via through contactless magnetic assembly is used. This process has been developed in previous work at the department of Micro and Nanosystems at KTH. The process is based on the ferromagnetic properties of nickel. 470 µm long nickel wire with a diameter of 35 µm are used as the conductive cores of the vias. The use of nickel wires is to ensure a void-free conductive core of the via.

The nickel wires are assembled in the via-holes by applying a magnetic field on the back-side of the wafer using a magnet. This causes the nickel wires to align themselves to the magnetic field lines of the magnet, effectively aligning themselves...
normal to the wafer surface. By moving the magnet in a predetermined pattern over the etched via-holes the wires fall inside.

This method has proven itself to be efficient in manufacturing TSVs, both as a reliable and effective fabrication process. The resulting TGVs also present good via characteristics [1].

2.3 Through Glass Vias (TGVs)

Although silicon is the most common material used as a substrate for electronics, the advantages of glass make it a very good material for through-via fabrication. Glass transparency makes it an ideal material for optical applications such as LED modules. Glass also has a smaller RF dielectric constant than silicon and it is a very good insulator [5].

Because glass is composed of different materials, it can be tailored for a specific application. Also, its properties can be manipulated, including the electrical resistance, thermal expansion [3] and chemical durability [3, 13].

One method of forming TGVs is by using a silicon mould, etched with a DRIE process and glass re-flow. After the mould is filled by the re-flow glass in a furnace at 1025°C, a process of polishing the surface is performed in order to expose the silicon pillars and ensure flatness. This polishing is performed chemically and mechanically. After this, the silicon is removed. Through seedless electroplating, copper is deposited in the newly formed holes in order to form the void-free core. Next, another chemical and mechanical polarization process is performed. The final step is to pattern the contact pads [13].

In the above case, copper is used as the conductive core of the via. In the industry, highly doped silicon is also used for the via core as an alternative to plated metal. In Figure 2.4, three combinations of silicon and glass for manufacturing through-vias are presented: Through-vias in a silicon wafer that are insulated by glass bushings or by a glass area and through-vias that are made in glass wafers using highly doped silicon as the conductive cores.
Glass interposers have a wide range of applications such as optical MEMS, solar photovoltaics, LED modules, opto components or CMOS image sensors. Glass interposers are used in analog and RF ICs due to the good RF inner properties of glass. Glass substrates are also used in microfluidics, e.g., for manufacturing micro-insulin pumps [5].
Chapter 3

TGV Fabrication

The fabrication process of TGVs in this work has followed the same steps as in the one developed previously at KTH [6, 1, 15]. The difference was the replacement of the silicon substrate with a glass substrate and a different spin-on polymer was used: 400F spin-on glass. Because of these material changes the process had to be changed to suit the new material characteristics. The nickel wires used were 470 µm long and had a diameter of 35 µm.

![Distribution of the arrays on the glass wafer](image)

**Figure 3.1:** Distribution of the arrays on the glass wafer with arrays 1 to 4 and 6 to 9 containing 20 by 20 via-holes while array 5 contains 14 by 20 via-holes.

In Figure 3.1 the via-hole pattern in the glass wafer is presented. The glass wafer thickness was 300 µm. The via-holes were distributed in nine arrays. These arrays contained 20x20 via-holes and were positioned around a central 14x20 array. The via-holes were 55 µm in diameter on the top side of the wafer but because the walls are tapered, at the bottom end the via-hole diameters were reduced to 35 µm.
3.1 Nickel Wire Stud Fabrication

Because filling high aspect ratio TGVs with void-free cores is difficult using copper electroplating, nickel wire studs were fabricated to serve as the conductive cores of the TGVs. By using these nickel wire studs, void-free via cores were ensured. The fabrication method of the nickel wire studs was developed in previous work at the Micro and Nanosystems department at KTH. The impact on the yield of the assembly process was investigated within this thesis work and presented in section "4.3 Wires with and without Burr".

The process started by winding the 35 µm nickel thread on two square silicon substrates with an edge length of 140 mm that were taped together. The distance between each wined strip of wire dictates the number of nickel wires that resulted. The square wafers were mounted on a machine developed by Andreas Fischer from the Micro and Nanosystems department at KTH. This machine turned the wafers around. The machine had two speeds: slow and fast which were alternated between when winding the nickel thread. This made the nickel core fabrication process faster in comparison to alternative approaches. The entire setup can be seen in Figure 3.2.

![Figure 3.2: Nickel wire winding setup. The two taped wafers are mounted onto the setup and spun counter clockwise by the use of a motor. The switch is used to alternate between the two speeds of the motor (fast and slow). The nickel wire is wound from the wire roll onto the cleaved wafers.](image-url)
The next step consisted of dicing the long nickel wires into shorter, well-defined 470 µm long studs, but before this could be achieved the nickel wires were fixed in place. This was done by spin coating at 1000 rpm a layer of photoresist on the surface of the wafers and afterwards soft baking it at 50°C. This step was taken to ensure that the dicing machine, which was used to dice the nickel wires, did not bend or distort the nickel wire studs in any way. The wires were diced using a high precision dicing tool at a well-defined length of 470 µm and a feed speed of 20 mm/s. After the dicing was finished, the result was a set of straight 470 µm wires that were still held in place, on the wafer, by the photoresist. At the end of each nickel wire a burr resulted from the movement of the dicing blade perpendicular to the nickel wires. This burr can be seen in Figure 3.3.

![Figure 3.3: The ends of two nickel wires that have burrs resulted from the dicing step. Courtesy of A. Fischer, KTH Stockholm.](image)

The next step was to remove the burrs. While still embedded in the photoresist, the burrs of the nickel wires were etched in an aluminium etch at a temperature of 50°C for 6 minutes. The aluminium etch gave good etch rates for nickel as well. As can be seen in Figure 3.4, the aluminium etch removed the burrs of the nickel wires. The final step was to collect the wires from the wafers. This was done by dissolving the photoresist in acetone and catching the wires in a container.
3.2 Magnetic Assembly of the Nickel Wires in the Via-Holes

The nickel wires were assembled inside the via-holes with the use of a robot arm. An assembly arm was used in order to ensure a controllable and repeatable process. The entire assembly, consisting of the robot in the middle, a station for a 200 mm wafer cassette, and the assembly stage, can be seen in Figure 3.5. Within this master thesis the wafer handling function of the robot was not utilized instead the wafers were placed manually on the assembly stage.

After the glass wafer was placed on the setup’s mount, a command was given to move the assembly arm under the glass wafer. The arm was fitted with a magnet and positioned in the starting point, just outside the targeted array. The nickel wires were placed on the surface of the glass wafer. Once on top of the glass wafer, the nickel wires aligned themselves to the magnetic field lines of the magnet due to nickel’s ferromagnetic properties. With the nickel wires in place and all the controls set up, as shown in Table 3.1, the assembly could be started. The parameters that were used are speed, acceleration and jerk to control the movements of the assembly arm in a precise manner. The values for theta (T), radial (R) and vertical (Z) movement, in Table 3.1 are expressed in mils.

Figure 3.4: Ends of two nickel wires that were etched using the aluminium etch. The aluminium etch removed the burrs that resulted form the dicing step. Courtesy of A. Fischer, KTH Stockholm.
Figure 3.5: The entire assembly setup consisting of the assembly robot, the wafer cassette and the assembly stage. The assembly robot is placed in the middle of the table while the wafer cassette and the assembly stage are positioned to the assembly robot’s right side. Courtesy of S. Bleiker, KTH Stockholm.

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Spline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>T=40 R=400 Z=450</td>
</tr>
<tr>
<td>Acceleration</td>
<td>T=1400 R=2000 Z=2000</td>
</tr>
<tr>
<td>Jerk</td>
<td>T=25 R=25 Z=25</td>
</tr>
</tbody>
</table>

Table 3.1: The control parameters and their appropriate values used in the LabView program for the assembly of the conductive cores in the via-holes. The Speed, Acceleration and Jerk parameters correspond to the setting realySlow of the program. T represents theta, R radial and Z vertical movement.

The result of the assembly process can be seen in Figure 3.6 as the top three arrays were 100% filled with the nickel wires. Kapton tape was applied to the backside of the glass wafers in order to stop the nickel wires from falling out after the magnetic assembly. This tape can also be seen in Figure 3.6, giving the wafer a greenish hue. A second strip of kapton tape was applied on the top side of the wafer in order to effectively isolate the rest of the arrays from being contaminated during the first TGV fabrication run.
3.3 The 400F Spin-on Glass

Spin-on glass was chosen as the spin-on polymer instead of BCB because it has very similar attributes as the glass substrate, such as transparency, mechanical properties and dielectric characteristics. Furthermore, spin-on glass has the ability to fill submicron gaps.

The 400F spin-on glass is a methylsilsesquioxane polymer that is widely used in industry. A silsesquioxane is an organosilicon compound that can be combined with hydrogen or an organic functional group like alkyl and has the formula $\text{RSiO}_{3/2}$ where $\text{Si}$ is the element silicon, $\text{O}$ is oxygen and $\text{R}$ is either hydrogen or the organic group [16]. Methylsilsesquioxane is composed of cage and/or partial cage structures due to which the dielectric constant is greatly reduced while still providing very good mechanical integrity. Typical curing temperatures for this type of polymer are 400 - 425$^\circ$C [17].

The 400F spin-on glass is available both in solution form and in film form. In this thesis only the liquid solution form was used. In table 6.1 of Appendix A the properties of the 400F solution are presented. It appears as a clear liquid and has as the primary solvent n-Butyl alcohol with the formula $\text{C}_4\text{H}_9\text{OH}$. The 400F spin-on glass is intended for applications ranging from low-k dielectric, interlayer dielectric, pre-metal dielectric to polarization, gap-fill, final passivisation, etchback and non-etchback processes and wafer bonding [17].
3.3.1 Spin-on Glass Deposition and Baking

After the nickel wire assembly followed the application of the 400F spin-on glass as the TGVs insulating layer. Because the spin-on glass was kept cool in the refrigerator, it was left approximately 30 minutes at room temperature. In this time an enclosure made from multiple layers of kapton tape stacked one on top of each other was fixed on the glass wafer in order to enclose the filled arrays. Before filling the enclosure with the insulator, the spin-on glass was placed on a hotplate and heated at 80°C for 1 minute.

Next, the enclosure was filled with the spin-on glass and placed in a soft vacuum of 500 mbar for 4 minutes. This was done in order to softly drive the solvents out of the insulator. As previous attempts showed, the spin-on glass, if placed in a stronger vacuum underwent violent degassing, effectively pushing out the insulator from the assembled via-holes. The same effect occurred if the spin-on glass was baked without priorly driving out the solvents. The soft degassing is crucial for a void-free filling of the insulation layer.

After the degassing, the vacuum was released and the baking process was performed. First, the wafer was placed on a preheated hot plate at 80°C for 2 minutes. For the next step, the temperature was ramped up to 150°C and held there for another 2 minutes. Then, the temperature was ramped up once more to 250°C and held for 2 minutes. The baking process is recommended to be performed with three separate hotplates, each preheated to 80°C, 150°C and 250°C respectively, with a time on each hot plate of 1 minute after which it is cured in a N₂ furnace at 425°C for 1 hour. Due to the lack of necessary equipment at the Micro and Nanosystems Department, where the tests were performed, this curing procedure was not exactly followed in this work. After the baking process was finished the wafer is left to cool before handling.

In Figure 3.7 the temperature and pressure characteristics of the baking stage are presented for BCB and spin-on glass. As can be seen, in both cases the temperature reaches 250°C but the entire procedure is much faster in the spin-on glass case, 26 minutes, in comparison with the BCB, 180 minutes. This was because the 80°C, 150°C and 250°C soaking stages were held for only 2 minutes in the case of the spin-on glass, while for the BCB the 100°C, 150°C were held for 15 minutes and the 250°C was for 60 minutes. The ramping time was also much shorter in the case of the spin-on glass with ramping times of approximately 5 minutes for each temperature step, while for BCB these were 15 minutes for the 100°C and 150°C and 60 minutes for 250°C. Another difference was the pressure at which the baking was performed. To the spin-on glass a soft vacuum of 500 mbar was applied for only 4 minutes and the baking was performed with no vacuum at all while the BCB was backed in a vacuum of 0.02 mbar.
3.4 TGV Fabrication Results

The assembly process described previously was used to fabricate TGVs. It proved challenging to successfully obtain a void-free filling of the via-holes. The issues resided with the filling and baking of the spin-on glass. When applying the spin-on glass on the assembled arrays, air bubbles formed inside the via-holes, thereby stopping the spin-on glass from filling the via-holes. A vacuum was applied to drive out the air bubbles from the via-holes, thus enabling the spin-on glass to fill the through-vias. Another issue was the violent degassing that occurred if the vacuum was too strong. This violent degassing pushed out the spin-on glass from the assembled via-holes, leaving only partially filled through-vias. If the vacuum was not strong enough or not held for a long enough time, these air bubbles would remain and prevent a void-free filling of the insulator. After repeated tests, a vacuum of 500 mbar held for 4 minutes proved efficient in driving out the air bubbles, while not causing a violent degassing of the spin-on glass.

Violent degassing also occurred if the spin-on glass was baked without priorly driving out the solvents. To ensure that this violent degassing did not happen, the spin-on glass was kept at room temperature for 30 minutes after which it was heated for one minute on a hotplate at 80°C to start driving out the solvents. The 500 mbar vacuum held for 4 minutes was also used for the purpose of driving out the solvent and effectively ensuring that the degassing during the baking stage would not push the spin-on glass out of the via-holes.
3.4.1 Silicon Wafer Tests

All tests regarding the fabrication process of the TGVs were first conducted on cheaper silicon wafers in order to ensure a working process for manufacturing void-free TGVs. To make the tests as realistic as possible, while using silicon wafers, the etched via wafers were first thermally oxidized.

Figure 3.8: Cross-section of a TSV. Void-free filling of the assembled via-hole was achieved using spin-on glass as an insulator.
3.4 TGV Fabrication Results

Figure 3.9: Magnified view of the middle and bottom parts of the TSV in Figure 3.8. As can be seen, the nickel core is insulated from the walls of the silicon substrate all around. The silicon wafer was not etched all the way through in order to stop the spin-on glass from flowing out of the via-holes.

In Figure 3.8 and 3.9 a void-free TSV is presented. The insulator is the 400F spin-on glass. It can be clearly seen that a void-free filling was obtained. Because it is an insulating material, the spin-on glass charges in the scanning electron microscope (SEM), thus enabling us to distinguish it from the other materials. With the process ready, the next step was to implement it on the glass substrate.

3.4.2 Glass Wafer Tests

After achieving a void-free filling of the TSVs, using spin-on glass, the same via fabrication process was repeated on glass wafers. In order to see if the TGVs were successfully fabricated, the glass wafer was diced and after, grinded in order to have a clear cross-section of the vias. Using the SEM, cross-sections of the TGVs were obtained. Using the processes described above, void-free filling was achieved.
Figure 3.10: Cross-section of the bottom part of the same TGV. Two different SEM detectors were used in order to better observe the void-free filling of the spin-on glass.

Figure 3.11: Cross-section of the middle of a TGV. Void-free filling of the spin-on glass was achieved.

As can be seen in Figures 3.10 and 3.11 over the entire length of the via-hole a void-free filling of the 400F spin-on glass was achieved. Because the glass substrate is an insulating material it also, charges in the SEM similar to the spin-on glass, impeding the correct assessment of the result. In this case the power of the electron
3.4 TGV Fabrication Results

stream must be carefully managed.
Chapter 4

Assembly Tests and Improvements

In this chapter the improvements of the via assembly process are presented and discussed. The three tasks that were undertaken within part of the project were a comparison between dense and spread arrays, the difference in assembling speeds when using wires that have burrs and wires that do not have burrs, and the excess wires.

4.1 Array Density

One of the secondary objectives of this thesis work was to investigate the influence of the pitch of the holes on the yield of the assembly process. The arrays on the silicon wafers used had 100 via-holes with diameters of 40, 42, 45, 47, 50 and 55 µm. These arrays were of two types, spread and dense. In the case of the spread arrays the via pitch was 350 µm. In the case of the dense arrays the via pitch was 75 µm.

The same assembly robot was used with the speed, acceleration and jerk as shown in Table 3.1. Figure 4.1 shows the spline patter which was used for the tests. The controls were set in order for the nickel wires to go over the desired array only two times, first covering the lower half of the array and afterwards the upper half. In the case of the spread arrays, the magnet traveled a distance of 8.85 mm until fully crossing over the array, followed by a return movement. The movement over the array and back again to the initial position represented one sweep. After completing the first sweep the magnet moved up a distance of 3.05 mm so that the wires would now assemble the second half of the via-holes. This distance represented one step. In the case of the dense arrays, the distance over the array was 3.34 mm and the step was 1.524 mm.
4.1 Array Density

Figure 4.1: Spline pattern where \( D \) is the distance the magnet travels in one sweep and \( d \) is the step the magnet moves after completing the sweep. In the case of the spread arrays \( D = 8.85 \text{ mm} \) and \( d = 3.048 \text{ mm} \). In the case of the dense arrays \( D = 3.34 \text{ mm} \) and \( d = 1.524 \text{ mm} \).

The results of the tests showed that the spread arrays were assembled faster than the dense arrays. As can be seen in Figure 4.2, the spread arrays that had via-holes of 55\( \mu \text{m} \), 50\( \mu \text{m} \), 47\( \mu \text{m} \) and 45\( \mu \text{m} \) in diameter were 100% filled after 2 seconds. The yield of the arrays with via-holes of 42\( \mu \text{m} \) and 40\( \mu \text{m} \) in diameter was over 90% after 2 seconds and reached 100% after 4 seconds. Letting the assembly process run up to 3 minutes did not affect the yield of the process.

Figure 4.2: Yield versus time of the spread arrays with via-holes of 55\( \mu \text{m} \), 50\( \mu \text{m} \), 47\( \mu \text{m} \), 45\( \mu \text{m} \), 42\( \mu \text{m} \) and 40\( \mu \text{m} \) in diameter. The spread arrays with via-holes of 42\( \mu \text{m} \) and 40\( \mu \text{m} \) in diameter, reached 100% yield 2 seconds later than the others, which reached 100% yield after 4 seconds.

It was harder to achieve 100% yield in the case of the dense arrays. The smaller the diameter of the via-holes, the longer it took to fill all of the via-holes, as shown in Figure 4.3. The dense arrays with via-holes of 55\( \mu \text{m} \) in diameter were completely...
filled the fastest, after approximately 8 seconds. The dense arrays with via-holes of 50 \( \mu \text{m} \) in diameter achieved 100% yield after 14 seconds while the dense arrays with via-holes of 47 \( \mu \text{m} \) and 45 \( \mu \text{m} \) in diameter achieved 100% yield after 30 seconds. The arrays with via-holes of 40 \( \mu \text{m} \) and 42 \( \mu \text{m} \) in diameter could not be filled 100% even after a longer time. In the case of the arrays with via-holes of 42 \( \mu \text{m} \) and 40 \( \mu \text{m} \) in diameter, the yield constantly remained at around 99%.

![Figure 4.3: Yield versus time of the dense arrays with via-holes of 55 \( \mu \text{m} \), 50 \( \mu \text{m} \), 47 \( \mu \text{m} \), 45 \( \mu \text{m} \), 42 \( \mu \text{m} \) and 40 \( \mu \text{m} \) in diameter. The fastest a dense arrays reached 100% yield was the arrays with via-holes of 55 \( \mu \text{m} \) in diameter after 8 seconds. The dense arrays with 40 \( \mu \text{m} \) and 42 \( \mu \text{m} \) in diameter via-holes did not reach 100% yield even after 10 seconds.](image)

As can be seen from Figure 4.2 and 4.3 the dense arrays took a longer time to achieve 100% yield depending on the diameter of the via-holes.

As a result the pitch between via-holes or the density of the arrays had a significant impact on the assembly times.

### 4.2 Excess Wires

After each assembly, a big number of excess wires, approximately 150, remained on top of the array as shown in Figure 4.4. These wires clinged to the ones inside the via-holes. One reason for this was that they got stuck to each other mechanically because of the grooves on the tips of the wires that resulted from the etching of the burrs. Another reason was that the wires got magnetized when assembled by the magnet. These surface wires needed to be gathered because they affected the quality of the TGV and they could be reused for future TGVs.

The first attempt to clean the excess wires off was with the use of a vibration motor. The motor was fixed to the wafer and a supply voltage was applied. In addition the wafer was tilted with approximately 15\(^\circ\) to one side. The setup can be seen in Figure 4.5. The intention was to calibrate the supply voltage in order
to get the correct vibrations from the motor to vibrate only the wires on top, off from the wafer and catch them with the help of a magnet.

Figure 4.4: An assembled spread array with 47 µm wide via-holes having approximately 150 excess wires on top of the array.

Figure 4.5: The setup used to vibrate the excess wires on top, off from the assembled arrays. The wafer is tilted 15° and a vibration motor is fixed on one side of the wafer.
This method had proven not to work because at low voltage amplitudes the top wires would not be vibrated off from the wafer. When increasing the voltage amplitude, the wires inside the via-holes were pulled out and vibrated off from the wafer along with the excess wires.

The second attempt to get rid of the excess wires was to use pressurized air to blow off the wires. A small jet of pressurized air set at 1.0 bar was applied from a distance of approximately 15 cm. The air nozzle was positioned perpendicular to the surface of the wafer, only slightly tilted to one side. The tilt served to push the excess wires in a desired direction in order to collect them with the help of a magnet.

In Figure 4.6A an array is presented right after the wire assembly process was performed. The array has via-holes with a diameter of 47 µm. There were a lot of excess wires on the surface of the array, approximately 150 wires. As can be seen in Figure 4.6B, after applying the air jet on the surface of the wafer only a small number of nickel wires remained. A small number of five wires were blown or pulled out of the via-holes at the end of the process.

![Figure 4.6: A. An array with via-holes having a diameter of 47 µm after the nickel wire assembly process. The number of excess wires left on top of the arrays is approximately 150. B. The same array after the cleaning of excess wires with the jet of air. A very small number of wires are left on the surface of the array and very few wires were pulled out of the via-holes (five wires).](image)

### 4.3 Wires with and without Burrs

A key feature of the improvements brought within this thesis work was the etching of the burrs of the nickel wires. These burrs caused problems when assembling
4.3 Wires with and without Burrs

the wires into the via-holes. Because these burrs were etched, the assembly speed of the wires could be increased, taking a shorter time to achieve 100% yield. In this section the improvement of the assembly speed compared to previous work is presented [1].

When assembling the nickel wires an array was placed in a chip holder as can be seen in Figure 4.7. This method has the benefit of not filling parts the via-holes of the arrays nearby together with the array under test. The disadvantage is that a gap is present between the walls of the array chip and the walls of the carrier and a lot of the wires fall inside these gaps as can be seen in Figure 4.8. In this case an array with via holes of 45 µm in diameter was assembled with nickel wires. A large number of wires were used in order to compensate for the ones lost in the gaps. With this number of wires 100% yield was achieved after 2 seconds.

![Figure 4.7: A diced via-hole array fitted in a holder on a carrier. This configuration was used in order to not fill adjacent arrays with wires.](image-url)
Figure 4.8: The result after assembling the nickel wires on an array with via holes of 45 µm in diameter. 100% yield was achieved but a large number of wires got stuck in the gaps between the chip and the carrier.

In Figure 4.9 four filling rates can be seen for which 100% yield was achieved. The Slow Spline and Slow Spline 2 filling rates are the fastest for which 100% yield was achieved in previous work [1], in 81 seconds and 66 seconds, respectively. For Slow Spline and Slow Spline 2 wires that have burrs were used. The spread arrays with via holes of 50 µm and 45 µm in diameter were diced into chips and placed on the holder as shown in Figure 4.8. With the new improvements: etching the burrs and going over the arrays only 2 times, 100% yield was achieved after 6 seconds in the case of the spread array with via holes of 50 µm in diameter and 2 seconds in the case of the spread array with via-holes of 45 µm in diameter. The spread array with via-holes of 45 µm in diameter achieved 100% yield after 2 seconds because more nickel wires were used, approximately 3000 nickel wires, while for the spread array with via-holes of 50 µm in diameter only 1000 nickel wires were used.
4.3 Wires with and without Burrs

Figure 4.9: The filling rates Slow Spline and Slow Spline 2 are the fastest until 100% yield was achieved in previous work [1]. The filling rates of the spread chip arrays with via-holes of 50 µm and 45 µm in diameter were obtained with the new improvements and process.

An alternative is not to dice the chip at all. The disadvantage of this is that adjacent arrays are filled with wires when assembling the array under test. The advantage is that less nickel wires are needed to achieve 100% yield in a very fast time. In this configuration, approximately 1000 nickel wires were used of which more than two thirds were recovered. The filling rates for this configuration can be seen in Figures 4.2 and 4.3 in the section ”4.2 Array Density”. The spread arrays with via-holes of 55 µm, 50 µm, 47 µm and 45 µm in diameter achieved 100% yield after 2 seconds while the spread arrays with via-holes of 42 µm and 40 µm in diameter achieved 100% yield after 4 seconds. In the case of the dense arrays the fastest was the arrays with via-holes of 55 µm in diameter which achieved 100% yield after 8 seconds. The dense arrays with via-holes of 42 µm and 40 µm in diameter could not achieve 100% yield even after 30 seconds of nickel wire assembly.
Chapter 5

Conclusion

The goal of this project was to apply a technique for fabricating TSVs developed at KTH [15, 6] to successfully manufacture TGVs for glass interposers. Instead of BCB, a different spin-on polymer was used, the 400F spin-on glass. A new process was developed, based on the one developed previously at KTH, to suit the manufacturing of TGVs. After performing filling tests on thermally oxidized silicon wafers, regarding the viability of using spin-on glass as a replacement for BCB and observing its behavior when undergoing the filling and curing phases of the process, positive results were achieved. These results encouraged the transition to the glass wafers.

The results obtained, both when using silicon and glass substrates show that TGVs with a solid conductive core and a void-free insulating layer can be achieved with the process developed within this thesis work. This shows that glass interposers with functional TGVs represent a possibility for manufacturing 2.5D devices.

Another goal of the thesis work was to investigate and improve the assembly process. Three aspects were investigated, the influence of the pitch of the via-holes, the cleaning of excess wires left on top of the array after assembly and the influence of the burrs on the assembly process.

The results of the comparison between the dense and spread arrays show clearly that the spread arrays are assembled faster. The dense arrays took longer to achieve a 100% yield than the spread ones, meaning that if the pitch of the via-holes is smaller the assembly process takes longer. In the case of the dense arrays with via-holes of 40 µm and 42 µm in diameter only 99% yield was achieved even after a longer time.

In the case of the excess wires two methods have been investigated. The first method used a vibration motor to vibrate the excess wires off from the assembled arrays. This proved inefficient in removing the excess wires without removing the nickel wires assembled in the via-holes. The second method applied used a pressurized jet of air at 1.0 bar. This method shows that it is possible to clean the majority of excess wires from the surface of the assembled array in a very short time. The number of excess wires left on the surface of the assembled arrays could
be reduced to 20. The downside is that up to 7% of the nickel wires were pulled out from the via-holes.

Finally, a comparison was performed with previous work, showing that the improvements brought in this thesis work had a significant impact on the assembly speed of the process. By etching the burrs and performing only two sweeps over the targeted array the assembly speed was reduced significantly in comparison with the best speed from previous work. 100% yield was achieved after 6 seconds, approximately 10 times faster when comparing to the fastest achieved assembly in previous work, which was after 66 seconds.

5.1 Improvements

Even though the project had been successful and the goals were achieved, further research can be performed. An immediate continuation of this thesis work is an electrical evaluation of the TGVs. Regarding the TGV manufacturing process, tests can be performed to see if the spin-on glass can achieve a void-free filling of the assembled via-holes without the need of an enclosure. Grinding of both the top and the bottom sides of the glass substrate can be performed in order to smoothen the sides of the glass wafer after the fabrication of the vias.

Furthermore, an alternative method for cleaning the excess wires on top of the assembled array can be tested. This could be achieved by implementing a pattern in the control software of the robot that moves the magnet around the edges of the array, at a certain distance and for a specified time. By moving the magnet around the assembled array, the top wires align themselves to the magnet field lines, thus clearing the array surface. A test could be performed in order to see if the assembled wires would be pulled out of the via-holes with this method.

Another improvement that was specified in previous work could be the implementation of a visual inspection protocol. The robot is already equipped with a camera that is used to monitor the assembly process. This can lead to the ability to inspect the yield of the array without additional handling that could damage the assembly process and eliminate chances of misalignment. Furthermore a protocol could be implemented to adaptively control the assembly process by recognizing both filled and unfilled via-holes.
Bibliography


Chapter 6

Appendix A - 400F Spin-on Glass Properties

In Table 6.1 properties of the 400F spin-on glass are presented.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Water Content (wt/wt%)</td>
<td>0.0</td>
</tr>
<tr>
<td>Viscosity (cP) at 25°C</td>
<td>1.70</td>
</tr>
<tr>
<td>Non-volatile Content (wt/wt%)</td>
<td>12.5</td>
</tr>
<tr>
<td>Specific Gravity (water=1.0)</td>
<td>0.81 at 20°C</td>
</tr>
<tr>
<td>Solubility in water (weight %)</td>
<td>Slightly</td>
</tr>
<tr>
<td>Boiling point</td>
<td>117.8°C at 760 mmHg</td>
</tr>
<tr>
<td>Melting point</td>
<td>-53.3°C</td>
</tr>
<tr>
<td>Evaporation rate (ether=1)</td>
<td>0.46</td>
</tr>
<tr>
<td>Vapour density (air=1)</td>
<td>2.55 kg/m³</td>
</tr>
<tr>
<td>Vapour pressure</td>
<td>4.2 mmHg at 20°C</td>
</tr>
</tbody>
</table>

*Table 6.1: 400F spin-on glass solution properties in the left column and the corresponding values in the right column*

The values were obtained from the manufacturer [17].