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Optimization on Guard time and Synchronization Cycle for TDMA-based Deterministic RFID System

Abstract—This paper presents optimizations on guard time and synchronization cycle for Time Division Multiple Access (TDMA) based deterministic Radio Frequency Identification (RFID) system. The TDMA scheme can provide guaranteed latency and high throughput for RFID system that includes fixed number of users (tags) and requests long-message transmission. However, collisions due to accumulated clock drifts of the active RFID tags equipped with independent self-clocked micro-controllers are the major challenge. In this work, we model relations between guard time and synchronization cycle used to tolerate the accumulated clock drift and reduce the probability of collisions for an extended-star RFID system. Constraints of safe guard time and synchronization cycle are proposed to consider energy efficiency and time efficiency. Moreover, optimization on guard time and synchronization cycle are explored in terms of transmission time, tag number, energy efficiency and time efficiency. The simulation results indicate that system with long transmission time (around 1 ms) enjoys higher time and energy efficiency under optimal configuration of guard time and synchronization cycle.

I. INTRODUCTION

Radio Frequency Identification (RFID) systems consisting of a large number of active tags with sensing and locating capabilities are growing in large-scale energy-constraint applications such as environmental monitoring [1], healthcare [2] and industrial automation [3]. Unlike the common used passive tags using centralized clock broadcasted from the reader, each active tag is equipped with a self-clocked micro-controller and distributed in a large area for sensing and monitoring [4], [5]. The active RFID tags provided longer operation distance, greater memory capabilities, and richer additional functions like real-time locating capabilities are hence more desired in wireless sensing networks beyond identifying.

In the applications that have fixed amount of tags and long sensory data packet, the deterministic access protocols which feature guaranteed latency and high channel throughput are expected compared to the stochastic access schemes such ALOHA [6]. Among the deterministic access methods, unlike technologies such as Code Division Multiple Access (CDMA) scheme which suffers from complicated hardware implementation and decreasing overall quality of service in large number of tags, the Time Division Multiple Access (TDMA) scheme separated tags in time is easy to realize and quality of service promised. By scheduling users into different time slots, the TDMA is the most cost-effective and energy-effective technology which enables long battery life and easy deployment. Moreover, the TDMA allows service compatibility, for example, it can work at dual-mode with Frequency Division Multiple Access (FDMA) to provide higher channel throughput [7].

However, the internal clock on the active tag created by

Fig. 1. A frame cycle of TDMA scheme with double-side guard time in each time slot.

build-in crystal oscillator experiences frequency variation due to vary of temperature and other factors of craft, resulting in clock of one tag drifts apart from others. The TDMA-based system hence suffers from synchronization problem due to accumulated clock drift. A double-side guard time as shown in Fig.1 is commonly used to tolerate the accumulated clock drift of tags allocated in neighboring slots for reducing collisions caused by clock skew. Moreover, a certain synchronization mechanism is applied to minimize the probability of message collision [8]. Although longer guard time can promise better collision avoidance performance and longer synchronization cycle, it leads to low time efficiency and low throughput as trade-off.

In this work we explore the relations in terms of guard time, synchronization cycle, transmission time, tag number, clock drift rate, and time and energy efficiency in an extended-star topology RFID system. The Timing-sync Protocol for Sensor Networks (TPSN) algorithm [9] is taken as basis, where we assume that each RFID tag is synchronized by its reader, and a public reference clock is provided by back-end server. Under the worst case assumption, three groups of relations between guard time, transmission time and time efficiency, synchronization cycle factor (energy efficiency), and tag number are proposed, respectively. Accordingly, optimal guard time (minimum) and synchronization cycle (maximum) can be achieved on demand of different requirements.

The remainder of the paper is organized as follows. In Section II, the system model is described, and the corresponded clock drifts scenarios in TDMA are shown. Optimization on guard time and synchronization cycle are provided based on two proposed constraints of synchronization cycle. In Section III, optimal configurations on guard time and synchronization cycle are proposed by exploring their relations with transmission time, tag number, time efficiency and energy efficiency under the worst case assumption. Finally, conclusions are given in Section IV.

Fig. 2. Model of the architecture of a RFID system.

II. GUARD TIME AND SYNCHRONIZATION CYCLE

A. System Model

For a RFID system, as the number of tag increases, multiple readers are requested for handling the tags in a larger area. A back-end server is then employed for gathering and processing data received by the readers. The system can be modeled by a 2-level extended-star topology as shown in Fig. 2:

Letting $S(V)$ to denote the graph of the topology network, and $v_p \in V$ is one of the vertex (reader or server). A tag node n in the topology that coordinated by v_p with order q can then be denoted by $n(v_p|q) \in S(v_p)$, where $S(v_p)$ is a subgraph coordinated by v_p . In this model, v_0 represents the back-end server, and p is the order of reader. A subgraph $S(v_p)$ is the sub-system that controlled by reader v_p . When TDMA is used, all communications between reader and tag are scheduled in time slots. Tags belong to different subgraph can be scheduled in neighboring slots while receiving synchronization message from different readers.

B. Clock Drift and Synchronization

The local clock time of tag n at time t is defined as

$$C_n(t) = \int_{t_0}^t \Delta c_n(\tau) d\tau + C_n(t_0) \quad (1)$$

where $\Delta c_n(\tau)$ is the local clock drift of tag n at time τ , $C_n(t_0)$ is its clock offset at initial time t_0 . The maximum deviation of local clock is defined as *drift rate* ϵ . Then the clock drift is random distributed in the region bounded by the drift rate, i.e. $\Delta c(\tau) \in [1 - \epsilon, 1 + \epsilon]$.

Based on the extended-star topology, we consider the clock value of the back-end server as reference clock for the whole system. Hence, the synchronization message is sent by the back-end server v_0 and passed by the readers to each tag. The clock drift of $n(v_p|q)$ at time t can then be defined as the difference of clock values between $n(v_p|q)$ and v_0 ,

$$\Delta C_n(t) = C_n(t) - C_{ref}(t) \quad (2)$$

where $C_{ref}(t)$ is the clock value of the server at time t .

Accordingly, the clock drift of tag $n(v_p|q)$ at time t can be either forward (positive) or backward (negative) comparing to the reference clock. For a TDMA frame consisting of

Fig. 3. The four possible time overlap scenarios of the neighboring slots.

w time slots, if slot i is assigned to tag $n(v_p|q)$, we can use $\Delta C_n^R(t; i) > 0$ and $\Delta C_n^L(t; i) < 0$ to represent the positive and negative offset of the tag's clock, respectively. Two neighboring time slots that assigned to different tags are then suffering from time shift either in the opposite direction or in the same direction. Therefore, when there exists a time overlap between the neighboring slots, collision of tags may occur. In other words, for slot i and $i+1$ assigned to tag n and $\hat{n}$, collision occurs if their slots shift in the opposite direction to meet each other or in the same direction with different shifts value at time t ,

$$\sigma_t \langle i, i+1 \rangle = \begin{cases} \Delta C_n^R(t; i) - \Delta C_{\hat{n}}(t; i+1) \\ \Delta C_n^L(t; i) - \Delta C_{\hat{n}}(t; i+1) \end{cases} \quad (3)$$

where pair $\sigma_t \langle i, i+1 \rangle$ represents the time overlap of slots i and $i+1$ at time t . $\Delta C_{\hat{n}}(t; i+1)$ is the clock drift of tag $\hat{n}$. The value of σ_t can be positive or negative depending on the accumulated drift status of n and $\hat{n}$. For simplicity, we assume that the initial clocks of the tags are 0, i.e. $C_n(t_0) = 0, n \in S(V)$. When $\sigma_t \langle i, i+1 \rangle \geq 0$, collision due to time overlap exists.

Therefore, guard time is employed to tolerate this time overlap. As shown in Fig. 1, a double-side *guard time* with length φ is added to each time slot. And α denotes time period used for transmission or reception (we simply call it transmission time). Fig. 3 illustrates the four possible shift scenarios of two neighboring slots defined in (3). When tags scheduled in slot i and slot $i+1$ drift in the opposite direction as shown in Fig. 3a, and Fig. 3d, an overlap occurs if $\Delta C_n^R(t; i)$ and $\Delta C_{\hat{n}}^L(t; i+1)$ (Fig. 3a). Otherwise, if $\Delta C_n^L(t; i)$ and $\Delta C_{\hat{n}}^R(t; i+1)$ (Fig. 3d), there exists no time overlap between the two tags. On the other hand, as the cases shown in Fig. 3b and Fig. 3c where the clocks drift in the same direction, then the overlap occurs if the accumulated drift of tag n is larger than tag $\hat{n}$ at time t (Fig. 3b), or vice versa (Fig. 3c), i.e. $\sigma_t \langle i, i+1 \rangle > 0$.

When the time overlap σ_t exceeds the guard time φ , synchronization messages are required to compensate the clock drifts. The synchronization cycle defined as the time difference between adjacent synchronization points t_n^1 and t_n^2 of tag n is

Fig. 4. System time efficiency.

expressed as $T_n^{syn} = t_n^2 - t_n^1$. And the corresponded clock drift within one synchronization cycle at time $t_n^d \in [t_n^1, t_n^2]$ is $\Delta C_n(t_n^d)$.

C. Configuration Optimization

To avoid collision, T_n^{syn} of tag n (allocated in slot i) should comply with the following constraints,

- the accumulated clock drift of n within the synchronization cycle should be smaller than half of the guard time φ , i.e. $|\Delta C_n(t_n^d; i)| \leq \frac{\varphi}{2}$ and,
- the overlap time of two neighboring slots within the synchronization cycle should be smaller than the guard time, i.e. $\sigma_t \langle i, i+1 \rangle \leq \varphi$.

The first constraint limits the maximum accumulated drift of each tag. While the second constraint gives the upper bound of time overlap between two neighboring slots. The maximum synchronization cycle can thus be determined based on the two constraints. In addition, for a system using TDMA schedule, the synchronization cycle of tag n follows

$$T_n^{syn} \geq k \cdot T_w \quad (4)$$

where $k \geq 1$ is the *synchronization cycle factor*, and T_w is the frame cycle including w slots, i.e. $T_w = w(\alpha + 2\varphi)$, and $T_{ts} = \alpha + 2\varphi$ is the length of one slot time.

We assume that $\frac{\partial C_n}{\partial t} \in [0, \epsilon_f]$ is the average clock drift of tag n with drift rate ϵ_f at frequency f . Then we can rewrite the first constraint as,

$$t_n^d \cdot \frac{\partial \Delta C_n}{\partial t} \leq \frac{\varphi}{2} \quad (5)$$

Based on (4) and (5), if the frame cycle is too large, although tag n is synchronized in the current frame, collision may occur before the next synchronization point due to limited guard time. Therefore, when the synchronization cycle is the minimum i.e. $T_n^{syn} = T_w$ (the worst case), the best guard time

$\varphi = 2T_w \cdot \frac{\partial \Delta C_n}{\partial t}$ can be achieved. For two tags, the second constraint is rewritten as

$$\left\langle (t^d - t_n^{syn}) \cdot \frac{\partial \Delta C_n}{\partial t}, (t^d - t_{\hat{n}}^{syn}) \cdot \frac{\partial \Delta C_{\hat{n}}}{\partial t} \right\rangle \leq \varphi \quad (6)$$

where pair $\langle \frac{\partial \Delta C_n}{\partial t}, \frac{\partial \Delta C_{\hat{n}}}{\partial t} \rangle$ is the average $\sigma_{td} \langle i, i+1 \rangle = \langle C_n(t^d), C_{\hat{n}}(t^d) \rangle$ of tag n and $\hat{n}$ in slot i and slot $i+1$. t_n^{syn} and $t_{\hat{n}}^{syn}$ are previous synchronization points of tag n and $\hat{n}$, respectively.

III. OPTIMIZATION

In this section, we identify the optimal guard time and synchronization cycle. We assume that there are M tags in the system, and their clocks have the same maximum drift rate. The worse case, i.e. all tags drift at their maximum rate and two neighboring tags drift in face to face direction, is considered. In this case, all tags have the same synchronization cycle, and constraints (5) and (6) are degenerated into the same one. Therefore the synchronization cycle T^{syn} is obtained by

$$k \cdot M \cdot (\alpha + 2\varphi) \leq t^{syn} \leq \frac{\varphi}{2\epsilon_{f,max}} \quad (7)$$

where $\epsilon_{f,max}$ is the maximum average drift rate under frequency f . Usually the drift rate of oscillator used in the micro-controller is less than 200 ppm. Hence we assume that $\epsilon = 100$ ppm under 32 MHz frequency is used in the following analysis.

We define *system time efficiency* as the ratio between the transmission time α and the slot length T_{ts} to describe the time efficiency of the entire system.

$$\gamma = \frac{\alpha}{T_{ts}} = \frac{\alpha}{\alpha + 2\varphi} \quad (8)$$

Although the synchronization cycle increases as the growth of guard time, it leads to large idle period and low time efficiency. The time efficiency under different guard time and transmission time is plotted in Fig. 4. The guard time grows from 1 μ s to 10 ms, the time efficiency for different transmission time can be obtained correspondingly. For a system with required time efficiency γ_g , the upper bound of guard time for a given transmission time α_g can be computed by

$$\varphi_{max,g} = \frac{1}{2} \left(\frac{\alpha_g}{\gamma_g} - \alpha_g \right) \quad (9)$$

Accordingly, based on (7), we can obtain the upper bound of synchronization cycle for different transmission time, i.e. $T^{syn} \leq \frac{\varphi}{2\epsilon_{f,max}}$. Fig. 5 draws the curves of synchronization cycle factor k under different guard time and tag number, where k is obtained by $\frac{\varphi}{2\epsilon_{f,max} \cdot M \cdot (\alpha + 2\varphi)}$. To avoid collisions, $k \geq 1$ should be guaranteed to ensure that the entire tags are synchronized before they exceeds the guard time. It is obviously that the system is more energy-efficient with larger k since it saves more power by reducing the power-on times of the tag's receiver. The figure indicates that when there is a small number of tags, e.g. $M = 10$ to $M = 100$, the minimum required $k = 1$ can be achieved at $\varphi = 1 \mu$ s from $\alpha = 10 \mu$ s to $\alpha = 10$ ms. Whereas when the tag number increases to 5000, the minimum guard time required for $k = 1$ grows to 33.3 μ s and 0.33 ms at $\alpha = 1$ ms and $\alpha = 10$ ms, respectively. From Fig. 5a, for M up to 10000, the value of k reaches to

Fig. 5. The value of k under different transmission time and tag number.

a ceiling point at $\varphi \leq 50 \mu\text{s}$. In other words, the maximum synchronization cycle can be achieved at $\varphi \leq 50 \mu\text{s}$. It can be found from Fig. 4, the corresponded time efficiency is 10%. To achieve higher time efficiency, we can let k to reach half of its ceiling value at $10 \mu\text{s}$ i.e. $T^{\text{syn}} = 0.5T^{\text{syn},\text{max}}$ (half maximum energy efficiency), the time efficiency increases to 30% then.

For a longer transmission time e.g. $\alpha = 1 \text{ ms}$, k reaches its ceiling value at around 2.5 ms, and the time efficiency is around 10%. However, it can achieve half maximum energy efficiency (synchronization cycle) at $80 \mu\text{s}$, which dramatically increases the time efficiency to more than 80%. Similarly, when the transmission time grows to 10 ms, the maximum synchronization cycle is obtained at $\varphi = 10 \text{ ms}$, the time efficiency is more than 30%. For half $T^{\text{syn},\text{max}}$ ($\varphi = 2.2 \text{ ms}$), the time efficiency increases to 70%. Above all, for time efficiency sensitive requirements, an optimal guard time and synchronization cycle can be obtained by decreasing the energy efficiency. System features long-message transmission ($\sim 1 \text{ ms}$) outperforms short-message (μs level) and extremely long-message ($\geq 10 \text{ ms}$) systems by applying the optimization

configuration on time efficiency.

In addition, the maximum tag number can be obtained at $k = 1$, Fig. 6 plots the curves of the maximum tag number with up to 10 ms guard time and up to 10 ms transmission time, i.e. $T_{ts} \leq 30 \text{ ms}$. It can be seen that although applications with short transmission time receive low time efficiency, e.g. $\alpha = 10 \mu\text{s}$ and $\alpha = 100 \mu\text{s}$, it can achieve up to 80 times ($M = 13000$) and 9 times ($M = 1500$) tag number compared to $\alpha = 1 \text{ ms}$ at $\varphi = 1 \mu\text{s}$, respectively. For $\alpha = 1 \text{ ms}$, it requests at least 0.1 ms guard time to achieve the same tag number. Therefore, the short-message system can achieve the maximum tag number (at an optimal extremely short guard time) without considering energy efficiency.

IV. CONCLUSION

In this paper, we explore the optimization between guard time and synchronization for a TDMA based RFID system. Constraints for safe guard time and synchronization cycle to avoid message collision caused accumulated clock drift are proposed. Optimization setups of guard time and synchronization based on the worst case consideration are then

Fig. 6. The maximum tag number under different transmission time.

explored in terms of system time efficiency, energy efficiency and tag number. For different requirements e.g. given time efficiency and tag number, the optimal guard time (minimum) and synchronization cycle (maximum) can be computed based on the suggested relations accordingly. The simulation results indicate that long-message system achieves higher time efficiency with lower trade-off of energy efficiency (maximum synchronization cycle) compared to short-message system. Without considering energy efficiency, the short-message system can afford larger number of tags with shorter guard time.

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