



Interactive RFID for Industrial and Healthcare Applications

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Abstract

This thesis introduces the circuit and system design of interactive Radio-Frequency Identification (RFID) for Internet of Things (IoT) applications. IoT has the vision of connectivity for anything, at anytime and anywhere. One of the most important characteristics of IoT is the automatic and massive interaction of real physical world (things and human) with the virtual Internet world. RFID tags integrated with sensors have been considered as one suitable technology for realizing the interaction. However, while it is important to have RFID tags with sensors as the input interaction, it is also important to have RFID tags with displays as the output interaction. Display interfaces vary based on the information and application scenarios. On one side, remote and centralized display interface is more suitable for scenarios such as monitoring and localization. On the other side, tag level display interface is more suitable for scenarios such as object identification and online to offline propagation.

For tag level display, though a substantial number of researches have focused on introducing sensing functionalities to low power Ultra-High Frequency (UHF) RFID tags, few works address UHF RFID tags with display interfaces. Power consumption and integration with display of rigid substrate are two main challenges. With the recent emerging of Electronic Paper Display (EPD) technologies, it becomes possible to overcome the two challenges. EPD resembles ordinary ink on paper by characteristics of substrate flexibility, pattern printability and material bi-stability. Average power consumption of display is significantly reduced due to bi-stability, the ability to hold color for certain periods without power supplies. Among different EPD types, Electrochromic (EC) display shows advantage of low driving voltage compatible to chip supply voltage. Therefore this thesis designs a low power UHF RFID tag integrated in 180 nm CMOS process with inkjet-printed EC polyimide display. For applications where refresh rate is ultra-low (such as electronic label in retailing and warehouse), the wireless display tag is passive and supplied by the energy harvested from UHF RF wave. For applications where refresh rate is not ultra-low (such as object identification label in mass customized manufacturing), the wireless display tag is semi-passive and supplied by soft battery. It works at low average power consumption and with out-of-battery alert.

For remote and centralized display, the limitations of uplink (from tags to reader) capacity and massive-tag information feedback in IoT scenarios is the main challenge. Compared to conventional UHF RFID backscattering whose data rate is limited within hundreds of kb/s, Ultra-wideband (UWB) transmission have been verified with the performance of Mb/s data rate with several tens of pJ/pulse energy consumption. Therefore, a circuit prototype of UHF/UWB RFID tag replacing UHF backscattering with UWB transmitter is implemented. It also consists of Analog-to-Digital Converter (ADC) and Electrocardiogram (ECG) electrodes for healthcare applications of real-time remote monitoring of multiple patients ECG signals. The ECG electrodes are fabricated on paper substrate by inkjet printing to improve patient comfort.

Key contribution of the thesis includes: 1) the power management scheme and circuit design of passive UHF/UWB RFID display tag. The tag sensi-

tivity (the input RF power) is -10.5 dBm for EC display driving, comparable to the performance of conventional passive UHF RFID tags without display functions, and -18.5 dBm for UWB transmission, comparable to the state-of-the-art performance of passive UHF RFID tag. 2) communication flow and circuit design of UHF/UWB RFID tag with ECG sensing. The optimum system throughput is 400 tags/second with 1.5 KHz ECG sampling rate and 10 Mb/s UWB pulse rate.

Keywords: Radio-Frequency Identification (RFID), Electrochromic (EC) display, energy harvesting, Ultra-Wideband (UWB), remote monitoring, Internet-of-Things (IoT).

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List of Acronyms

ACF	Anisotropic Conductive Adhesives
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
AFE	Analog Frontend
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude-Shift Keying
BLE	Bluetooth Low Energy
BMU	battery management unit
CCU	central control unit
CMOS	Complementary Metal Oxide Semiconductor
ECG	Electrocardiogram
EC	Electrochromic
EPC	Electronic Product Code
EPD	Electronic Paper Display
EP	Electro-Phoretic
EW	Electro-Wetting
FoM	Figure of Merit
HILD	Harmonic Injection-Locked Divider
if	Intermediate Frequency
IoT	Internet of Things
LCD	Liquid Crystal Display
LDO	low-drop-out
LED	Light Emitting Diode
LO	local oscillator
LPF	Low Pass Filter
LTE	Long-Term Evolution
LUT	Lookup Table
NFC	Near Field Communication
OOK	On-Off-Keying
P2S	Parallel to Serial
PA	Power Amplifier
PDA	Personal Digital Assistant
PIE	Pulse-Interval Encoding
PLL	Phase-Locked Loop
PMU	Power Management Unit
PSD	Power Spectral Density
PVT	Process, Voltage and Temperature
RFID	Radio-Frequency Identification
SAR	Successive-Approximation-Register

SDR	Software-Defined Radio
SDM	$\Sigma\Delta$ modulation
TDR	Time Domain Reflectometry
TFT	Thin Film Transistor
UHF	Ultra-High Frequency
UWB	Ultra-Wide Band
VHDL	VHSIC Hardware Description Language
VNA	Vector Network Analyzer

List of Publications

Papers included in this thesis

- [**Paper I**] Jue Shen, Li Xie, Jia Mao, F. Jonsson, and Li-Rong Zheng, “Intelligent packaging with inkjet-printed Electrochromic paper display - a passive display infotag,” in *NIP & Digital Fabrication Conference*, vol. 2012, no. 1. Society for Imaging Science and Technology, Sept 2012, pp. 164-167.
- [**Paper II**] Jue Shen, Li Xie, Jia Mao, and Li-Rong Zheng, “A passive UHF-RFID tag with inkjet-printed Electrochromic paper display,” in *RFID (RFID)*, 2013 IEEE International Conference on, April 2013, pp. 118-123.
- [**Paper III**] Jue Shen, Jia Mao, Geng Yang, Li Xie, Yi Feng, M. B. Nejad, Zou Zhuo, Hannu Tenhunen, Li-Rong Zheng, “A 180 nm-CMOS asymmetric UWB-RFID tag with real-time remote-monitored ECG-sensing,” in *Proceedings of the International Conference on Biomedical Electronics and Devices*, Jan 2015, pp. 210-215.
- [**Paper IV**] Li Xie, Jue Shen, Jia Mao, F. Jonsson, Li-Rong Zheng, “Co-design of flip chip interconnection with anisotropic conductive adhesives and inkjet printed circuits for paper-based RFID tag,” in *Electronic Components and Technology Conference (ECTC)*, 2011 IEEE 61st, May 2011, pp.1752-1757.
- [**Paper V**] Le-Bo Wang, You-De Hu, Li-Rong Zheng, Jue Shen, Zou Zhuo, “Design of wideband mixer and VGA for software defined radio in RFID application,” in *NORCHIP*, 2014, Oct. 2014, pp.1-4.
- [**Paper VI**] Jue Shen, M. B. Nejad, Jia Mao, Li Xie, Zou Zhuo, Hannu Tenhunen, Li-Rong Zheng, “A Passive UHF/UWB RFID tag with inkjet-printed Electrochromic polyimide display for IoT applications,” under revision by *IEEE Internet of Things Journal (IoT-J)*.
- [**Paper VII**] Jue Shen, M. B. Nejad, Li Xie, Jia Mao, Zou Zhuo, Zhi-Bo Pang, Yi Feng, Li-Da Xu, Hannu Tenhunen, Li-Rong Zheng, “Interactive UHF/UWB

RFID tag for Mass Customization,” submission to *Information Systems Frontiers (ISF)*.

Papers not included in this thesis

[**Paper VIII**] Jue Shen, F. Jonsson, Jian Chen, Hannu Tenhunen, Li-Rong Zheng, “Phase noise improvement and noise modeling of type-I ADPLL with non-linear quantization effects,” in *NORCHIP, 2014*, Oct. 2014, pp.1-4.

[**Paper IX**] Jue Shen, Jia Mao, Geng Yang, Li Xie, Yi Feng, M. B. Nejad, Zou Zhuo, Hannu Tenhunen, Li-Rong Zheng, “A 180 nm-CMOS UHF/UWB RFID tag with inkjet-printed paper-based ECG electrodes,” submission to *Healthcare Technology Letters*.

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Chapter 1

Introduction

1.1 Background

The Internet of Things (IoT) has the vision of connectivity for anything, at any-time and anywhere [1, 2]. It extends current Internet to the real physical world (things and people) by attaching them with wireless micro-devices, and hence has always been associated with terms of ‘ambient intelligence’ [3]. More specifically, ambient intelligence describes the ‘embedded-everywhere’ vision in which all objects around human can be connected to Internet and can interact with physical world. It is achieved by massive deployment of the wireless micro-devices integrated with sensors [4]. It enables a wide range of applications and new business opportunities in many areas including medical and healthcare, supply chain and warehouse management, manufacturing and automation, safety and security [5].

Among others, Radio-Frequency Identification (RFID) integrated with sensors has been considered one fundamental technology to realize the vision of ambient intelligence and the notion of IoT [6, 7], because RFID is a low cost, low power, object identification technology, and has been widely used in tracing and tracking of large scale of objects.

An RFID system identifies objects by electromagnetic waves [8]. It typically consists of one or several transponders or tags attached to the objects to be identified, and an interrogator or reader which identifies the tags [8].

From the energy source aspect, an RFID tag can be sorted into passive, semi-passive, and active RFID tags. The active tag integrates a battery to provide the energy for tag operations. It also uses active transmission. Thus not only can it operate at much farther communication distance, but also can it operate as both a reader and a tag. Hence it supports ad-hoc network and is most flexible in network communication layer. But the active tag consumes high cost, large size and operates with limited life time. To the contrary, the passive tag harvests the operation energy from the electromagnetic wave transmitted by the reader [9]. It also replaces active transmission by load modulation or electromagnetic

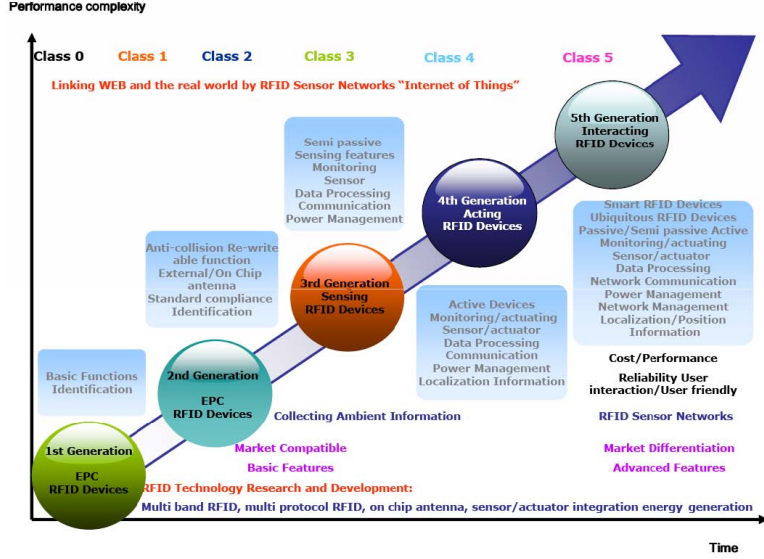


Figure 1.1: From RFID to the IoT [12].

backscattering [8]. Backscattering is the operation that the tag antenna reflects the electromagnetic wave transmitted by the reader back to the reader antenna [10]. When the impedance at the tag antenna port changes, the reflected wave to the reader antenna also changes. This mechanism is utilized as an ultra low power and simple wireless communication scheme from passive RFID tags to the reader. Passive tag is more widely used than active tags because of low cost, small size, and unlimited life time [8]. The semi-passive tag utilizes battery as active tag does, but only uses it for communication and more advanced functions such as sensing. It still employs backscattering for data transmission as passive tag does. It is a common trade-off design between cost and function.

From the air interface and frequency band aspects, an RFID tag can be categorized into the capacitive or inductive coupling tag operating from hundreds of KHz to tens of MHz frequency bands and the radiative coupling tag operating from hundreds of MHz to several GHz frequency bands [11]. For passive tags, compared to the capacitive and inductive coupling tags of which the communication distance is shorter than 1 meter [8, 10], the radiative coupling tags can communicate for much longer distance up to 10 meters typically. However, the path loss of the backscattered signal power scales as the inverse fourth power of the distance, which increases the identification difficulty in specific environments such as nearby water, metal or organic tissues; or in a dense multi-path and multi-user environment [6]. And the data rate is limited to few hundreds of kilo-bit per second (kbps) [8].

1.2 Motivation

1.2.1 Interactive RFID System as an RFID Trend

According to the roadmap of RFID systems illustrated in Figure 1.1 [12], one of the characteristics of the fifth generation interaction RFID devices is to be “user friendly” and “user interaction”. Thus, it is important to design an RFID system with not only sensors but also user-friendly display interfaces [4, 7, 13]. Furthermore, to enable the tag attachment to ubiquitous objects in industrial and healthcare applications, sensors and displays manufactured on flexible substrate are highly demanded. In this dissertation, the RFID system with flexible displays as well as sensors is named as the “interactive” RFID system.

1.2.2 Application Scenarios

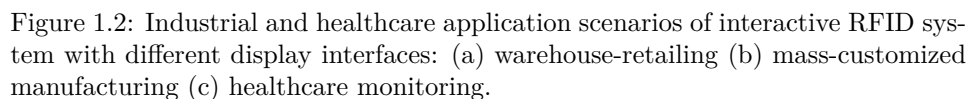
Several advanced applications are enabled by the interactive RFID system with display interfaces. Typical examples include warehouse retailing, mass-customized manufacturing, and healthcare real-time remote monitoring.

- Warehouse-retailing

Warehouse retailing is one retail mode that saves the extra cost for logistics and distribution, increases response speed to customer demands, and decreases customer dependency on retail staff. It has been successful for industries such as furniture, construction materials, etc. In warehouse retailing, customers write down the serial No., location and price of the sample products in show rooms, and find the corresponding products in warehouse by labels. If label information in show rooms mismatch to that in warehouse due to staff ignorance or slow response to object changes, customers face a lot more trouble in finding them. With electronic labels comprising of display and RFID tag, display information of the vast number of objects can be updated automatically. Moreover, the display tags can proactively propagate up-to-date sales information to offline customers instead of requiring customers to initiate the information interaction, saving their time and efforts in scanning the HF RFID tag or checking the online information by mobile phones [7, 13]. The display interfaces are illustrated in Figure 1.2 (a.1), and the application scenario is illustrated in Figure 1.2 (a.2).

- Mass-customized manufacturing

Mass customization (MC) is expected to be an important developing pattern and a new economic growth engine. From the market supply aspect, competition in traditional industries of mass-scale manufacturing has become white-hot in cost reduction due to homogeneous products and services [14, 15]. From the market demanding aspect, customers are no longer satisfied with the standard products provided by manufacturing firms through mass production.



With display integrated RFID tags attached to the to-be-processed objects

as well as the processing machines throughout the simplified manufacturing chain. A certain number of RFID readers, for example one per 100 m², are equipped in the factory [19]. When a number of these tags are sensed close to the processing machines by the reader, the reader inquires the customized information from the tags and transmits them to the processing machines. Machines thus carry out different processing, such as picking up specific material and components, printing specific figures, according to the received information. In cases when manpower is involved in the assembling processes, the offline workers do the jobs according to the information displayed on the tags that are attached to the to-be-processed objects. Because a large number of the tags can be accessed by reader within a second, the information exchange among large number of products and sub-assemblies, with machines and readers can be finished within short communication time. Figure 1.2 (b.1) and (b.2) illustrate the display interfaces, and Figure 1.2 (b.2) illustrates the application scenario.

- Healthcare real-time remote monitoring

One of the most common healthcare signals measured in clinical practice is Electrocardiogram (ECG). For long-term continuous monitoring, conventional solutions adopt Holter devices. It requires a large number of cumbersome wires, and does not support real-time feedback to hospitals. Comparatively, wireless ECG tags which are attached to the patient body by flexible electrodes and transmit signals to cloud in real time greatly improve patient comfort and increase response accuracy. As one resultant example, for patients recovering from serious diseases, such tags facilitate them to do rehabilitation exercises and shorten recovering periods while ECG signals are simultaneously and continuously monitored at the backend central server. Figure 1.2 (c.1) illustrates the display interface, and Figure 1.2 (c.2) illustrates the application scenario.

1.2.3 Remote and Tag-Level Display Interface

Display interfaces of the interactive RFID system vary significantly according to different applications. On one side, information for object monitoring and localization is more efficient to be interfaced with remote and centralized display. On the other side, information for object identification and propagation is more effective to be shown alongside each individual object. With display interfaces embedded at daily objects, IoT is no longer a closed loop where information communicated from machine-to-machine or device-to-device can only be interacted with limited sophisticated interfaces such as smart phones and remote readers installed with correspondent programs; instead, it becomes a most direct and “embedded-everywhere” medium where human can interact.

1.2.4 Design Challenges

Although there have been substantial amount of research works for the sensing interface design of RFID systems, few works address the display interface for the discussed IoT applications, and several design challenges must be solved to implement the display interfaces in the interactive system.

For tag-level or local display interaction, one most vital challenge is the limited power budget to drive displays for low power low cost RFID tags, especially for passive tags. Conventional display technologies such as LED (light emitting diode) and LCD (liquid crystal display) are designed for high pixel density and high image refresh rate applications, not suitable for integration with RFID tags featuring with low power, low cost, small size, and low refresh rate. The other challenge is the dilemma of display size and tag minimization. For user interaction, sizes of display are not expected to be minimized. However, conventional electronic displays are fabricated on rigid substrates. As a result, integrating display with RFID tag would make the entire tag very bulky and hard to attach with daily objects.

For remote display interaction, information is to be transmitted to and displayed at the back-end control unit, and one consequential challenge is information transmission efficiency. In IoT applications, huge amount of sensing data are transmitted from large numbers of objects. And in typical applications such as healthcare monitoring, the data are required to be transmitted in real time. Therefore, high data rate transmission is needed. Current passive RFID tags mostly adopt backscattering or load modulation with data rate limited to a few hundreds of kbps [20–23], causing large communication latency. Therefore, tag with higher data rate and not much increased power consumption is demanded.

1.3 Work Contribution

Due to the aforementioned motivations and design challenges of the interactive RFID systems, this dissertation proposes the design of passive and semi-passive RFID tags with inkjet-printed EC display, ECG sensor and high data rate Ultra-Wide Band (UWB) transmitter. They are targeted for industrial and healthcare applications under the context of IoT. Inkjet-printed display and sensor on flexible substrates are utilized to achieve ambient intelligence. The dissertation is thus a multidisciplinary research work covering application specific integrated circuit (ASIC) design and inkjet-printed components study. Research contributions are as follows.

[Paper I] Jue Shen, Li Xie, Jia Mao, F. Jonsson, and Li-Rong Zheng, “Intelligent packaging with inkjet-printed Electrochromic paper display - a passive display infotag,” in *NIP & Digital Fabrication Conference, vol. 2012, no. 1. Society for Imaging Science and Technology*, Sept 2012, pp. 164-167.

Paper contribution: This paper analyzes the electrical characteristics of inkjet-printed Electrochromic (EC) display. It is the first work that extracts an equivalent circuit model for EC display and the first work that discusses the crosstalk effects of EC display from circuit aspects. The results of capacitive model and energy sensitiveness of EC display lay the foundation for the circuit design of power management unit (PMU) and display driver of passive UHF RFID display tag in the subsequent papers.

Work contribution: The author discovered the crosstalk phenomena and the energy sensitiveness of EC display, carried out the measurements, analyzed the experimental results from circuit design aspects, and wrote the manuscript.

[**Paper II**] Jue Shen, Li Xie, Jia Mao, and Li-Rong Zheng, “A passive UHF-RFID tag with inkjet-printed Electrochromic paper display,” in *RFID (RFID)*, 2013 *IEEE International Conference on*, April 2013, pp. 118-123.

Paper contribution: This paper propose a passive UHF RFID tag integrated with an inkjet-printed Electrochromic (EC) paper display. The switching power (refreshing power) of the EC display is much larger compared to the conventional passive UHF RFID tag power budget. The equivalent capacitance of EC display is also much larger than conventional loads of passive UHF RFID tag, resulting in significantly prolonged powering-up time of voltage regulator. This paper therefore modifies the design of a dual-supply duty-cycling power management unit (PMU) so as to accumulate display charging energy by multiple PMU duty cycles and to increase chip powering-up speed when display is charged. A dual-supply power management unit separates the power supply for display driving and that for other circuit functions (1.8 V for display output buffers and 1.2 V for the core circuit). 1.8 V supply voltage is switched off when output of voltage rectifier is lower than a threshold value (2.0 V), and is switched on for display driving only when the output increases higher than another threshold value (2.8 V). Due to the capacitive and energy sensitivity features of EC display, the refreshing energy of EC display is accumulated over multiple cycles of rectifier charging and display charging. Meanwhile, since 1.2 V supply voltage is kept switched on when output of voltage rectifier is higher than 1.8 V, the power management unit charges EC display while keeps the 1.2 V supplied core circuit functions not impacted. The design is fabricated in a 0.18- μm CMOS process with an area of 2.25 mm². Experimental results demonstrate correct refresh of 4 cm² EC displays with the write command of EPC Class 1 Generation 2 protocol.

Work contribution: The author performed the power analysis, proposed the power management unit for passive display tag based on a previous work, proposed the feedback driving method for EC display, implemented the analog and

RF parts of the chip, participated in digital parts implementation, set up the tests, and wrote the manuscript.

[Paper III] Jue Shen, Jia Mao, Geng Yang, Li Xie, Yi Feng, M. B. Nejad, Zou Zhuo, Hannu Tenhunen, Li-Rong Zheng, “A 180 nm-CMOS asymmetric UWB-RFID tag with real-time remote-monitored ECG-sensing,” in *Proceedings of the International Conference on Biomedical Electronics and Devices*, Jan 2015, pp. 210-215.

Paper contribution: This paper proposes a Ultra-High Frequency / Ultra-Wideband RFID (UHF/UWB RFID) system for real-time transmission of undistorted Electrocardiogram (ECG) data for hospital applications. In this system, each patient is attached with a semi-passive UHF/UWB RFID tag with inkjet-printed paper-based ECG electrodes. Printed paper-based ECG electrodes are utilized to improve patient comfort. UWB transmission of which the data rate is much higher than ECG sampling rate transmits the ECG data of multiple patients to UHF/UWB RFID reader and subsequently to the remote monitor in real time. A corresponding communication protocol which interleaves ADC sampling and burst-mode UWB transmission of each tag is proposed based on a modified Frame-slotted ALOHA protocol. The optimal system throughput is analyzed to be 400 tags/second at 1.5 KHz ECG sampling rate and 10 Mbps UWB pulse rate. The tag in this system consists of an UHF RFID receiver, an UWB transmitter, an ECG analog front-end, a multi-input ADC and the baseband circuitry. To verify the system, the tag is implemented in two silicon dies of 180 nm CMOS process and 6 mm² silicon size. Experimental results show that the tag transmits ECG data by UWB pulses at 1 Mbps rate with 18 μ W power, and the printed electrodes conduct ECG waveform comparable to the commercial electrodes.

Work contribution: The author proposed the idea of real-time ECG data transmission with high speed UWB link for hospital applications, modified the communication protocol based on a previous work, implemented the chip blocks besides the ECG amplifying and filtering frontend, measured the system, and wrote the manuscript.

[Paper IV] Li Xie, Jue Shen, Jia Mao, F. Jonsson, Li-Rong Zheng, “Co-design of flip chip interconnection with anisotropic conductive adhesives and inkjet printed circuits for paper-based RFID tag,” in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, May 2011, pp.1752-1757.

Paper contribution: This paper studies the radio frequency performance of the interconnect using anisotropic conductive film (ACF). A series of experiments are conducted in order to measure and model the electrical characteristics of inkjet-printed circuits on paper substrate as well as the impedance param-

ters of ACF interconnect at high frequency. Four-point measurement structure, Time Domain Reflectometry (TDR), Vector Network Analyzer (VNA) and de-embedded technology are used to ensure the accuracy of the experiments. Equivalent circuit models are built based on the experimental results. Finally, these models are considered as parts of the matching network and the circuit design for the RFID receiver, which can be co-designed for paper-based electronic systems. It is found that since the difference between RFID tags with and without ACF interconnects is negligible, the influence of ACF interconnects can be ignored for paper-based UHF RFID tag. As a conclusion, ACF is a feasible interconnect material for paper-based RFID tags.

Work contribution: The author participated in the layout design and manufacturing of the test devices in this work, and co-authored the paper.

[Paper V] Le-Bo Wang, You-De Hu, Li-Rong Zheng, Jue Shen, Zou Zhuo, “Design of wideband mixer and VGA for software defined radio in RFID application,” in *NORCHIP, 2014*, Oct. 2014, pp.1-4.

Paper contribution: This paper presents Software Defined Radio (SDR) focusing on wideband mixer and VGA design for RFID sensing applications. The wideband receiver can support UHF, UWB band for mostly used long range RFID standards ranging from 400 MHz to 6 GHz. The wideband mixer is of folded topology with switching biased technique, achieving maximum 11.5 dB conversion gain with only 8 dB double-sideband (DSB) noise figure and 16 dB flicker noise at 10 kHz. The VGA utilizes four-stage modified Cherry-Hopper amplifier, along with DC-offset canceling and common-mode feedback. A maximum gain of 67 dB can be achieved with more than 600 MHz bandwidth. The design is implemented in a 65 nm CMOS process. The total power consumption of the mixer and the VGA is 7 mW by simulation. The die area of these two blocks is 0.045 mm².

Work contribution: The author analyzed RFID bands link budget, Flash ADC performances, and all-digital polar transmitter performances to participate in the system specifications and system architecture designs of the Software-Defined Radio (SDR) transceiver for multi-band RFID communication, and co-authored the paper.

[Paper VI] Jue Shen, M. B. Nejad, Jia Mao, Li Xie, Zou Zhuo, Hannu Tenhunen, Li-Rong Zheng, “A Passive UHF/UWB RFID tag with inkjet-printed Electrochromic polyimide display for IoT applications,” under revision by *IEEE Internet of Things Journal (IoT-J)*.

Paper contribution: This paper proposes a passive UHF/UWB RFID display tag with -10.5 dBm sensitivity (input RF power) for EC display refreshing and

-18.5 dBm sensitivity for UWB transmission. It is used for information display in the Internet-of-Things (IoT) - both remotely by UWB transmission of tag status information to cloud end and locally by EC displaying of object identification and propagation information at tag side. The UHF part remotely powers-up and controls the tag as conventional passive RFID tag does. To overcome the limitations of uplink capacity and massive-tag information feedback, UWB transmitter replaces UHF RFID backscattering to achieve Mbps transmission data rate and 2000 tags/sec tag identification rate. For UWB transmission, based on the previous researches in passive UHF/UWB RFID tags, PMU operates in duty-cycling scheme and UWB transmission is activated only when enough energy has been stored. For EC display refreshing, to improve tag sensitivity and maintain it as display area increases, single-pixel addressing scheme is proposed by exploiting the bi-stability feature of EC display. In this scheme, it is the EC display discharging current that limits the tag sensitivity. The cost it pays is much prolonged display refreshing time. For IoT display applications such as electronic shelf labels in warehouse and retailing where the object identification and propagation information is updated just several times per day, such passive wireless display tag is a suitable solution. Compared to Paper II, this paper defines the application scenarios of such tag, further studies the theoretic limit of tag sensitivity with display and UWB functions, improves tag sensitivity by single-pixel addressing scheme, and tests the sensitivity. The experimental results demonstrate that the EC display can be refreshed with tag sensitivity (input RF power) of -10.5 dBm at 11.7 sec/cm² update rate, and the UWB transmitter can be powered up for 2 Mbps pulse rate and 35% operation duty cycle with tag sensitivity of -18.5 dBm.

Work contribution: The author improved and quantified tag power analysis based on paper II, improved tag sensitivity by adding single-pixel addressing scheme to the dual-supply duty-cycling power management unit, implemented the analog and RF parts of the chip, participated in the digital parts implementation, performed more experiments than in Paper II, and wrote the manuscript.

[Paper VII] Jue Shen, M. B. Nejad, Li Xie, Jia Mao, Zou Zhuo, Zhi-Bo Pang, Yi Feng, Li-Da Xu, Hannu Tenhunen, Li-Rong Zheng, “Interactive UHF/UWB RFID tag for Mass Customization,” submission to *Information Systems Frontiers (ISF)*.

Paper contribution: Mass Customization (MC) under the context of the Internet of Things (IoT) is expected to reform traditional mass manufacturing by offering personalized products at large scale with low cost. An interactive UHF RFID tag with Ultra-wideband (UWB) transmitter and flexible Electrochromic (EC) display can contribute to MC as follows. From the information communication aspect, by attaching the wireless display tags to assemblers and products and installing readers in factories, the varied customized information can be

exchanging between each product and machines in real time. From the user interaction aspect, the automatically refreshed display tags save the offline workers the extra time for scanning the bar-code or HF RFID tag one by one. They also reduce the error probability which is much higher in manual change of bar-code or HF RFID tag. Refresh rate for tag displays in the MC applications are not low, therefore a soft battery is included in the tag. To save the average power consumption and increase battery life, display driver with feedback comparator is utilized. To reduce battery maintenance cost and manpower, a battery alert unit is designed to transmit alert signals from tags to reader when battery voltage drops below a threshold value. For verification, the tag implemented in 180 nm CMOS process is tested. Compared to pure UHF RFID systems, it demonstrates shorter reader-to-tags communication time by Mbps UWB transmission rate and pipeline operation of UHF reception and UWB transmission of the tags. The functions of feedback display driving and out of battery alert are also verified. As a conceptual demonstration for the next tag version that targets ubiquitous integrations, a flexible tag prototype on polyimide substrate is presented at the end of this work.

Work contribution: The author proposed the application scenarios of the UHF/UWB RFID tags for Mass Customization, defined the corresponding tag architecture, performed the measurements, participated in manufacturing the printed version prototype, and wrote the manuscript.

1.4 Thesis Organization

This dissertation is organized as follows. Chapter 2 introduces the emerging technologies and the architecture of the interactive RFID system. The performance of UWB communication, inkjet-printed Electrochromic (EC) display and inkjet-printed ECG sensors are studied to be selected for the architecture of the interactive RFID system. Specifically, the study of EC display lays the theoretic foundation for the chip design of the display tag [*paper I*]. Based on the system architecture, Chapter 3 and 4 propose the different tag designs based on one chip implementation. The chip is implemented in UMC 180nm CMOS process. Chapter 3 focuses on the power design and circuit implementation of a passive UHF/UWB RFID tag integrated with inkjet-printed EC display and UWB transmitter for tag-level display interaction [*paper II, paper VI*]. Chapter 4 focuses on communication design and circuit implementation of a semi-passive UHF RFID tag with inkjet-printed ECG sensor and UWB transmitter for real-time remote display interaction [*paper III, paper IV, paper VII*]. Chapter 5 presents the system specification and circuit design for a software-defined radio (SDR) transceiver communicating with the proposed tags [*paper V*]. Chapter 6 concludes the dissertation and outlooks the future work. Figure 1.3 illustrates the thesis organization.

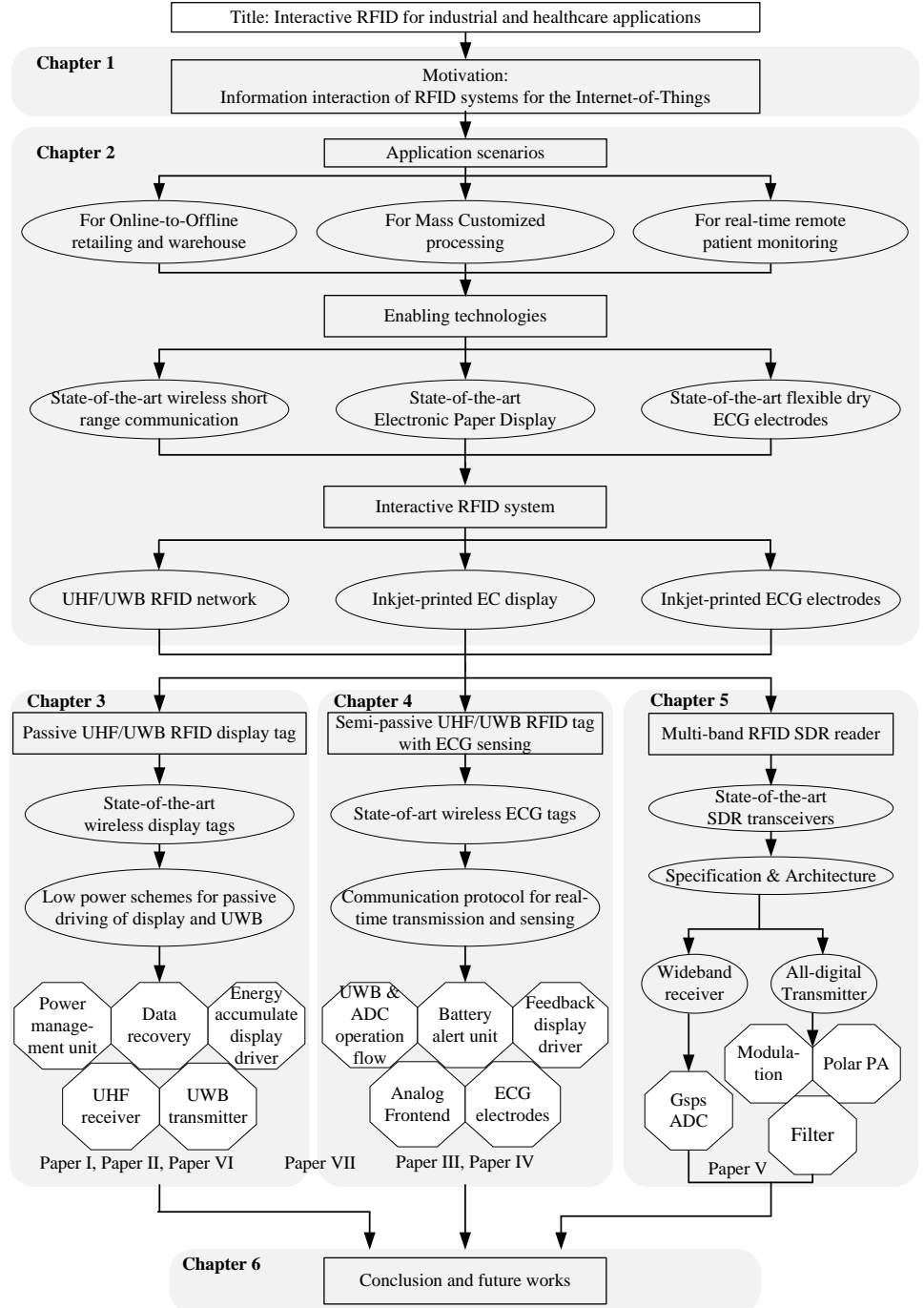


Figure 1.3: Thesis Organization

Chapter 2

Interactive UHF/UWB RFID Tag

This chapter introduces the architecture of the interactive UHF/UWB RFID system. It first introduces the emerging technologies in the areas of short range communications, flexible displays and sensors to cope with the design challenges discussed in 1.2.4. It then describes the proposed system that is composed of the UHF/UWB RFID communication network and the UHF/UWB RFID tag with inkjet-printed display and sensor. Varied tag structures are presented for different applications.

2.1 Enabling Technologies for Interactive RFID System

The design challenges for interactive RFID system are 1) low power and flexible electronic display 2) low power and high rate data transmission. Several technologies have emerged recently to deal with the challenges and lay foundations for the interactive RFID system.

2.1.1 Flexible Electronic Paper Display

The inkjet-printed Electronic Paper Display (EPD) has been a revolutionary technology enabling ubiquitous display in IoT. Although none of the EPD technologies is suitable for conventional video applications, they are very useful for application featuring with ultra-low power consumption and small display size. The EPD resembles ordinary ink on paper by characteristics of substrate flexibility and pattern print-ability [24]. Most EPD technologies are also referred to as “reflective displays” compared to “emissive display” such as conventional LCD. In emissive displays, light from a backlight is projected through the display towards user eyes. In reflective displays, no backlight is used; rather, ambient light from the environment is reflected from the surface of the display back to user eyes. As with any reflective surface, the more ambient light, the brighter the display looks. The backlight can also consume up to 40% of the power used in electronic product [25]. Therefore, eliminating the need for a backlight further decreases the power consumption of

display driving. Most importantly, a few EPD technologies have the characteristic of bi-stability. Bi-stability is the ability to hold color for certain periods without power supplies [24, 26–32]. Average power consumption is significantly reduced due to bi-stability, making it possible to integrate display functions in RFID tags. EPD can be summarized into electro-phoretic (EP) display, electro-wetting (EW) display, electro-chromic (EC) display, organic LED (OLED), and cholesteric LCD (Ch-LCD) display technologies.

- EP Display

The core material in EP display is electronic ink. Electronic ink is made up of millions of tiny microcapsules, about the diameter of a human hair. Each microcapsule contains positively charged white particles and negatively charged black particles suspended in a clear fluid. When a positive or negative electric field is applied, corresponding particles move to the top of the microcapsule where they become visible to the viewer. This makes the surface appear white or black at that spot [25]. Figure 2.1 (a) illustrates the principle.

- EW Display

EW describes a scheme which modifies the wetting properties of a solid material by voltage, that is when a voltage is applied to a hydrophobic surface, it becomes less hydrophobic and extends the contact surface of the liquid droplet above it [33]. Figure 2.1 (b) illustrates the application in EW display [33]. In equilibrium the colored oil naturally forms a continuous film between the water and the hydrophobic insulator (Figure 2.1 (b.1)) due to the fact the surface tension force is more than 1,000 times stronger than the gravitational force. As a result, the oil film is stable in all orientations and stays in lowest energy in this form. When a voltage difference is applied across the hydrophobic insulator, an electrostatic term is added to the energy balance and the stacked state is no longer energetically favorable. The system thus lowers its energy by moving the water into contact with the insulator, thereby displacing the oil (Figure 2.1 (b.2)) and exposing the underlying reflecting surface. EW is not bi-stable.

- Ch-LCD Display Ch-LCD has two stable states: planer state in which the helical axis is more or less perpendicular to the cell substrates as shown in Figure 2.1 (c.1), and the focal conic state in which the helical axis is more or less parallel to the substrates as shown in Figure 2.1 (c.2). Incident light is reflected in planer state and scattered or diffracted in focal conic state. Applying a medium value voltage on Ch-LCD display in planer state switch it into focal conic state. Yet, to switch it back to the planar state, first a high voltage must be applied, which switches the liquid crystal into an intermediate homeotropic state where the helical structure is unwound as shown in Figure 2.1 (c.3). And then removes the voltage to relax the liquid crystals into the

planar state. The arrows in Figure 2.1 (c) illustrate Ch-LCD display responses to applied voltages [34].

- OLED Display

As illustrated in Figure 2.1 (d) [35], a voltage is applied across the OLED such that the anode is positive with respect to the cathode. This causes a current of electrons to flow through the device from cathode to anode. Thus, the cathode gives electrons to the emissive layer and the anode withdraws electrons from the conductive layer; in other words, the anode gives electron holes to the conductive layer. Soon, the emissive layer becomes negatively charged, while the conductive layer becomes rich in positively charged holes. Electrostatic forces bring the electrons and the holes towards each other and they recombine. This happens closer to the emissive layer, because in organic semiconductors holes are more mobile than electrons. The recombination causes a drop in the energy levels of electrons, accompanied by an emission of radiation whose frequency is in the visible region. OLED is neither bi-stable or reflective.

- EC Display

Architecture of inkjet-printed EC display is shown in Figure 2.1 (e) [24]. Display cell is made up of two adjacent electrodes and a transparent electrolyte covering them. PEDOT:PSS works as both the electronic conducting and the Electrochromic material. PEDOT:PSS is transparent in pristine semi-oxidized state. When applying a driving voltage (typically no less than 1.8 V), the counter electrode is further oxidized and becomes more transparent, while the active electrode is reduced and becomes blue [24].

[24, 36, 37] provide two key characteristics. First, the condition of switching EC display to the reduced state is the amount of electronic charge per cm^2 and the driving voltage. Because the relationship among charge, voltage and energy is $Q \cdot V = E$, the amount of the supplied energy can be alternatively utilized as the display switching condition. Such threshold energy amount is named the switching energy (E_{sw}) in the following paragraph. Second, Electrochromic feature of EC display is bi-stable. It indicates that if the supply energy is removed after the EC display is switched to the reduced blue state, it takes a period of time before the color starts to degrade. This period is called retention time in the following paragraph. To be noticed, the time for EC display color to totally fade out to initial transparent color is much longer than retention time. This work measures the retention time by fully reducing the display sample by a DC current source and disconnect the supply afterwards. For display material when aging has not occurred, the retention time is around 900 seconds and the time for color to totally fade out is at orders of magnitude of several hours [38, 39].

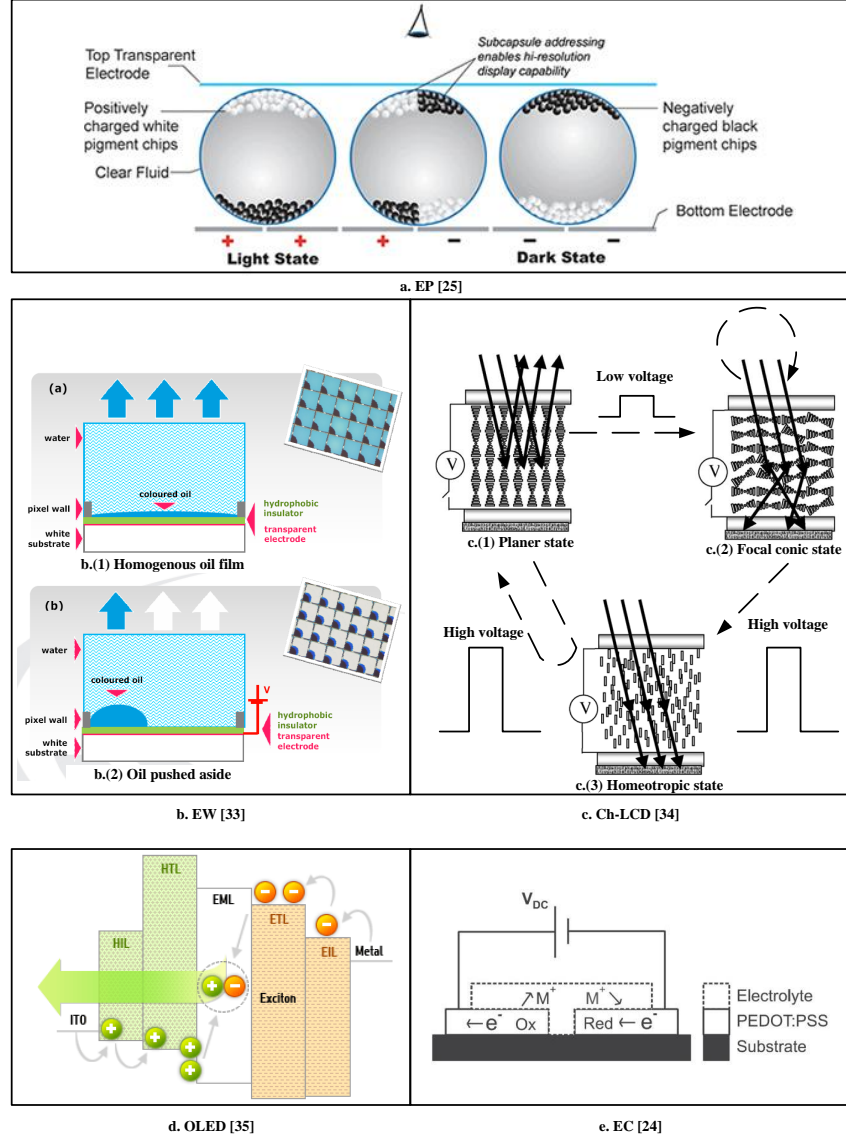


Figure 2.1: Introduction of state-of-the-art EPD technologies.

Figure 2.2 summarizes the performance comparison of EPD technologies. Among them, EP, Ch-LCD and EC technologies have bi-stability. And EC display distinguishes from other EPD in terms of driving voltage [26–32]. Most EPD technologies

Technology	Drive Voltage (V)	Response Time (ms)	Contrast Ratio (%)
Electrophoretic / Microencapsule	15	50	10-15
Electrophoretic / Air-Gap	70	0.2	
Electrowetting / Electrofluidic	20-60	3-10	>10
Flexible OLED / Polymer LED	NA*	<1	100
Ch-LCD	>40	1750	25
Electrochromic	1-3.3	<16000	>15

*OLED is supplied by current at tens of micro-ampere.

Figure 2.2: Performance comparison of electronic paper display technologies.

demand driving voltages surpass 10 V, while EC display on polyimide substrate can be driven by as low as 1.8 V, well compatible with CMOS operating voltage and sparing complexity of analog charge pumps. As a result, inkjet-printed EC polyimide display is most suitable for low power, low voltage, and low refresh rate RFID tag applications.

2.1.2 UWB Technology

Ultra-wideband Impulse Radio (UWB-IR) using short pulses for data transmission has the potential of Mbps data rate, tens of meters operating range and centimeter-level positioning without significant increase in power consumption and implementation cost.

Different from narrow-band short range communications such as UHF-RFID and Bluetooth Low Energy (BLE) which transmit continuous carrier wave, UWB transmits ultra-narrow impulses with orders of hundreds pico-second (ps) in the time domain, as illustrated in Figure 2.3 [40]. Therefore, compared to the pulse duration, the pulse repetition period is much longer and the activated duty cycle is very low, greatly reducing the average power consumption of data transmission. Transforming to the frequency domain, because its transmission energy is accumulated by very low Power Spectral Density (PSD) over very wide bandwidth, it can operate at high data rate and ultra-wide bandwidth without interfering other narrow band communications. According to UWB standards, more accurately, it covers a wideband at least 500 MHz in the 3.1 to 10.6 GHz band and that meets the spectrum mask in [41].

UWB impulses can be generated by delay of digital circuits and digital buffers [8, 42]. The only non-digital part is the filter to shape the pulse. It does not require finely-tuned analog-intensive power amplifiers which are required for maximum RF power efficiency in narrow-band wireless signaling. UWB communication pays cost in UWB receiver at the reader side. It is very area and power hungry, and requires finely-designed synchronization algorithm. Communication range of tag-to-reader by UWB is above 10 meters [41]. Figure 2.4 summarizes the performances of tags that are implemented by UWB transmission and other common short range com-

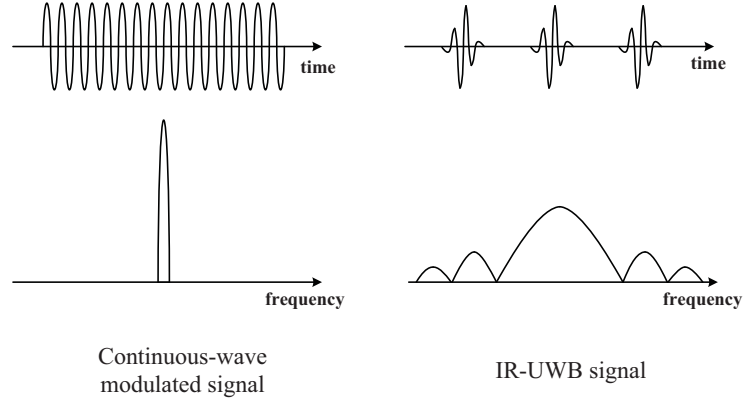


Figure 2.3: Comparisons between narrow-band signals and UWB-IR signals [40].

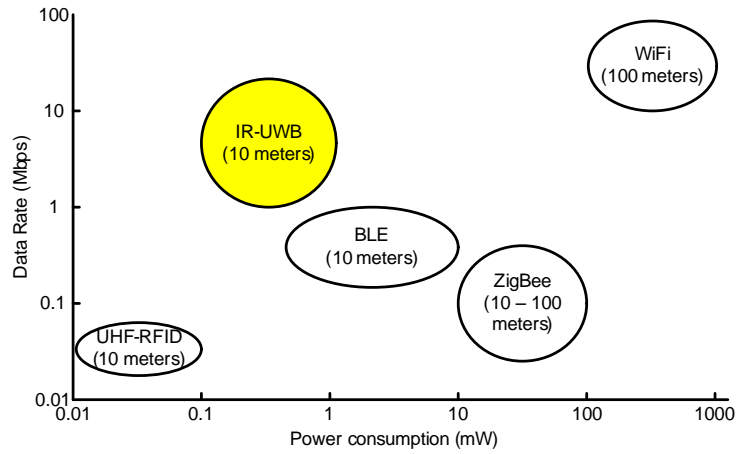


Figure 2.4: Performance of tags implemented by different short range wireless communications.

munications - UHF RFID, BLE, ZigBee and WiFi, in terms of power consumption, data rate, and communication distance [43–45]. It can be concluded that the UWB technology is one most suitable choice to achieve high data rate transmission while maintaining low tag power consumption.

2.2 Proposed Interactive RFID System

Based on the enabling technologies, an interactive RFID system featuring with 1) asymmetric UHF/UWB RFID network 2) UHF/UWB RFID tag integrated with printed display and sensor is proposed in this section. Multiple tags transmit the information of location and sensed object status to reader for remote display. Reader transmits commands to program the operation of multiple tags. Readers also transmit to tags the different user interactive information such as object identification and propagation for display at tag side.

2.2.1 Network Architecture

A two-layer asymmetric UHF/UWB RFID network architecture is illustrated in Figure 2.5. A number of readers divide the communication architecture into two layers, and relay the communications between largely deployed tags and the Central Control Unit (CCU). Otherwise, the transceiver at tag side would be too complex and power-area hungry to communicate with CCU directly.

In the lower layer, readers communicate with multiple tags by low power short range communication links. The downlink from the reader to tags employs UHF-RFID signals using amplitude-shift keying modulation with pulse-interval encoding (ASK-PIE). It is because the UHF RFID receiver at tag side can be implemented with a simple non-coherent envelop detector, much simpler than other receivers. And according to the state-of-the-art passive RFID tags works, such receiver can work with RF sensitivity around -18 dBm [21, 46, 47]. The uplink communication from tags to the reader is UWB-IR signals with on-off-keying (OOK). As introduced in Section 2.1.2, the UWB transmission shows better performance trade-off between data rate and power consumption compared to other conventional short range wireless communications, enabling real-time communication of large number of physical objects with still low tag power consumption. It also shows better multi-path performance due to the ultra short pulse in time domain. The circuit design of powering up UWB transmission by passive UHF RFID tag is described in chapter 3. In the higher layer, readers communicate with CCU by high performance communication links such as WiFi or Long-Term Evolution (LTE) depending on application scenarios. A reader consists of UHF RFID transceiver, UWB receiver and communication module with CCU.

2.2.2 Tag Structure

The interactive RFID tag is composed of application specific integrated circuit (ASIC), inkjet-printed EC display, flexible sensor, UHF antenna, UWB antenna, and flexible battery, as illustrated in Figure 2.5.

Functional blocks of the ASIC chip is illustrated in Figure 2.6. The power management unit (PMU) generates the chip supply voltage from different energy sources. The envelope detector (EnvDet) extracts the envelope of the received UHF-

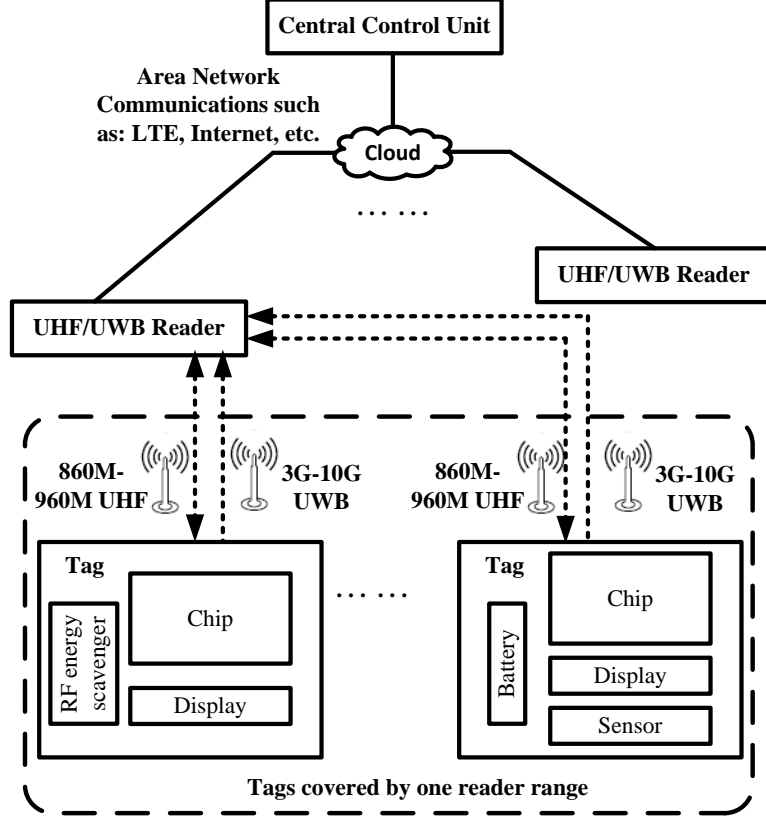


Figure 2.5: Proposed system architecture

RFID wave. The clock and data generator amplifies the envelope and decodes the data information in the envelope. The baseband (BB) circuitry controls the chip function and stores baseband data. The oscillator (OSC) generates another independent on-chip clock. The bias generator generates the bias current. The UWB transmitter generates the UWB-IR pulses for transmission. The EC display driver manages the display driving scheme. The sensor interface transfers the signal from sensors to the effective input signals for ADC.

Different energy sources and display driving schemes are utilized for different applications. In the specific healthcare applications where bio-signal sensing must be activated continuously, battery is utilized as the energy source, and passive-matrix display driving scheme is adopted. Comparatively, in the specific industrial applications where display can be refreshed at low frequency and sensing is limited within basic functions like temperature and humidity, UHF RF wave is employed as the energy source, and single-pixel/segment display driving scheme is designed.

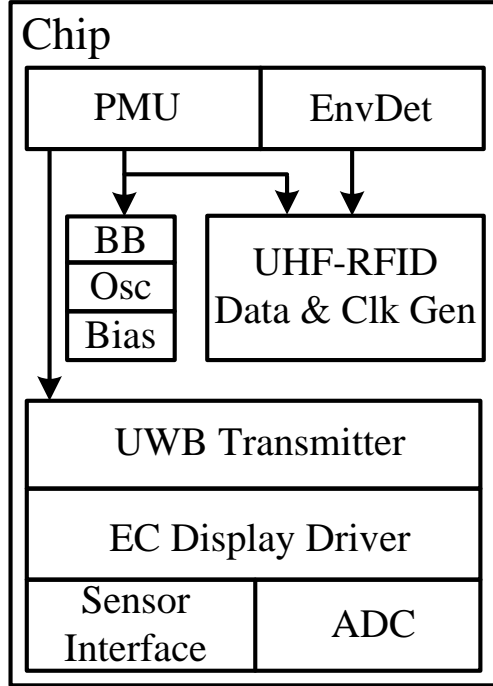


Figure 2.6: Functional blocks of the ASIC chip.

Therefore, the ASIC chip is designed to be programmable so that the functional blocks can be selected according to different applications. Two circuit block diagrams - passive tag version without battery and semi-passive tag version with soft battery as shown in Figure 2.5, are introduced in the next two chapters, respectively. The varied chip operation flow and correspondent circuit implementation are also discussed in the following two chapters, respectively.

2.2.3 EC Display for Tag

As discussed before, besides bi-stability, EC display on polyimide substrate can be driven by as low as 1.8 V, well compatible with CMOS operating voltage and sparing complexity of analog charge pumps. Therefore this work selects inkjet-printed EC polyimide display for the interactive RFID tag. However, EC display still suffers problems from material aging and high instantaneous power consumption. Therefore, the performances of the EC display are studied as the foundation for both the passive and the semi-passive tag designs.

2.2.3.1 Equivalent Circuit Model

An equivalent circuit model is extracted for low power display tag design. Extraction is made up of two steps: step 1 defines equivalent RC structure, and step 2 measures the equivalent RC values. The tested display samples are two displays, each with 8 columns and 2 grounds.

Step 1 is made up of one assumption and three measurements.

- Assumption

First, because the display is switched to reduced state by electronic energy and can stay in the reduced state with the absence of power supply for a limited retention period, the display is assumed to resemble the energy storage effect of a capacitor (C) paralleled by a discharge resistor (Rp).

- DC performance measurement

Secondly, the DC performance is measured by driving the display with a constant voltage source. The measured currents keep decreasing yet will never reaches zero. This indicates that the display has a current path consisting of only resistance in both the oxidized state and the reduced state.

- Frequency response measurement

Thirdly, the frequency response is measured by applying a square-wave voltage source with different frequencies and duty cycles under the same voltage amplitude. Results show that the switching behavior of the EC display is sensitivity to the driving frequency and duty cycle. This not only verifies the assumption of capacitance model, but also indicates a resistance (Rs) serial to it, resulting in a low pass filter structure.

- Diode performance measurement

Fourthly, the diode performance is measured by reversing the electrodes connection with supply, and repeating the previous experiments. Results show no obvious difference from the previous ones, indicating that EC display has no diode model as exists in OLED displays. In summary the EC display shows a circuit model in Figure 2.7.

In step 2, the RC values are extracted. Based on the defined RC structure, the voltage of the EC display can be utilized to represent its storage energy by $E = C \cdot V^2$. Further, according to [24, 36, 37], the switching energy (E) is around 0.5 mJ/cm² and the switching voltage is no less than 1.5 V. Therefore C can be evaluated by $E = C \cdot V^2$. When C value has been extracted, Rp value can be directly extracted by the discharging period, i.e., time constant of RC discharging. Rs value can be obtained by Ohm Law $V_s = I_s \times (R_s + R_p)$, of which I_s is a DC current that supplies the display and V_s is the measured voltage.

Figure 2.7 (b) summarizes the electronic parameters tested with the new seven-segment EC display sample. The exact RC values can vary for different display

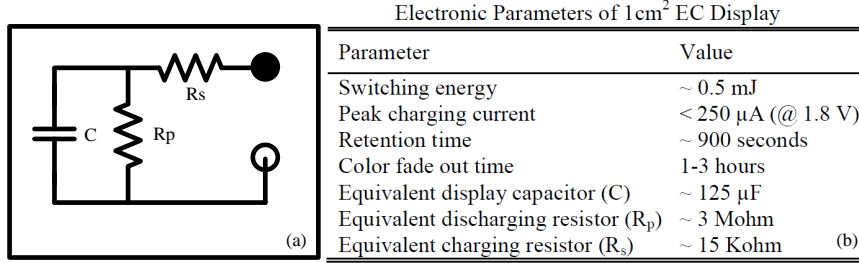


Figure 2.7: Equivalent circuit model (a) (*Adapted from Paper I*) and electronic parameters (b) (*Adapted from Paper I and Paper II*) of the EC display.

samples and when the sample is used for long time. But, the RC structure is tends to be fixed.

2.2.3.2 Material Aging

Figure 2.8 demonstrates the sample variation in terms of discharging speed over 3 months, and the display color corresponding to different values of discharging voltage (referred to the green curve voltage). As illustrated in Figure 2.8, the discharging speed varies significantly yet the threshold voltage at which the color completely fades out does not, indicating that the threshold voltage instead of the retention time can be utilized in the driver design to cope with the material aging problem. From the viewpoint of the equivalent circuit of the EC display, material aging exerts more impact on equivalent resistors than capacitors.

2.2.3.3 Crosstalk Effects

The crosstalk effect of the EC display is also studied. The crosstalk effect describes the phenomena that when one pixel is “light”, a certain number of other pixels which are not intended to “light” will also light. This is specific to passive matrix-addressing because there is always a voltage drop across every pixel as long as one pixel is connected to the supply pair. Based on the switching energy experiments in the previous section, the threshold voltage driving PEDOT:PSS to the reduced state is not sharp enough, especially around the CMOS supply voltage levels (1.0 V to 1.8 V), resulting in significant crosstalk effects in all the three passive-matrix addressing methods as illustrated in Figure 2.9 [38]. The crosstalk effect can be reduced by better patterning of EC display cells with insulators. It can also be reduced by supplying the display cell with just enough, not too much, electric charges or energy related to the reported switching charge or energy [36]. For the single-pixel addressing scheme introduced in the next chapter, crosstalk effect is also less significant because first the charging electric is kept very small and second

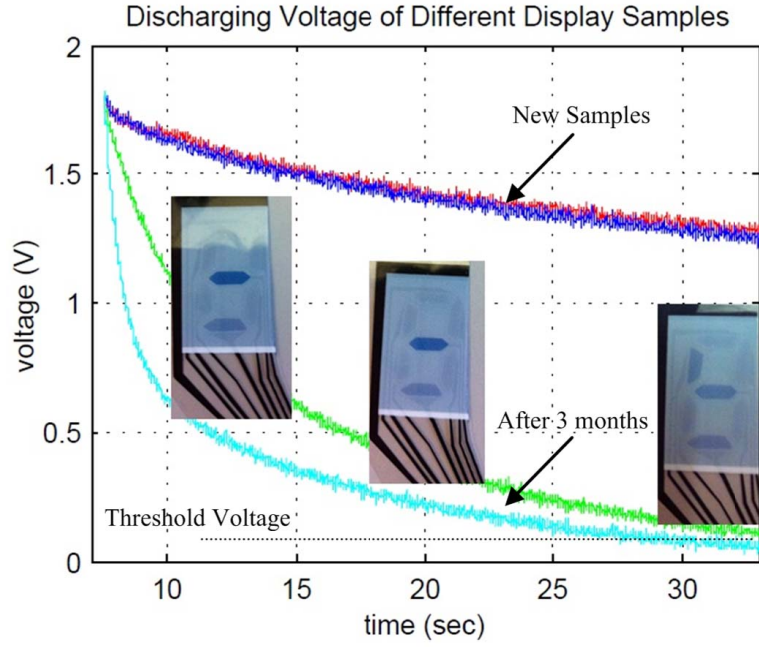


Figure 2.8: The variation of the display discharging speed of 2 samples over 3 months, and the color gradients (of the middle segment) VS the discharging voltages (of the green curve). *Adapted from Paper II.*

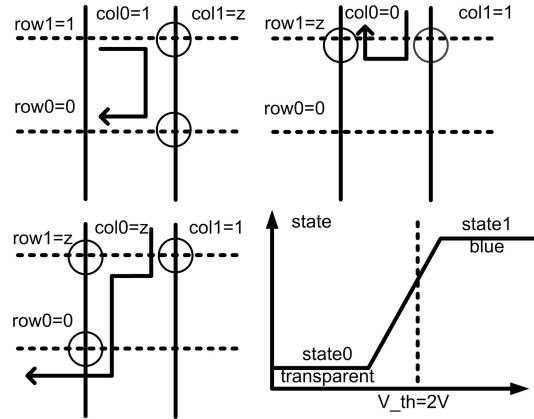


Figure 2.9: Threshold voltage of display state switching and crosstalk effects in 3 passive matrix-addressing methods. *Adapted from Paper I.*

the leakage current further decreases as display area increases in the single-pixel addressing scheme since the leakage path increases.

2.3 Summary

The vision of IoT leads to a boom of new applications of RFID systems. The emerging applications bring about new design challenges in areas of power, flexibility and data rate for RFID tag design. Enabling technologies of flexible display, flexible sensor and UWB communication make it possible to solve the new challenges. An interactive RFID tag based on these technologies is proposed in this chapter. It proposes the two-layer asymmetric UHF/UWB RFID network architecture and the tag structure integrating printed EC display, sensor, and flexible battery for semi-passive mode. The detailed block diagrams and circuit implementation of the interactive RFID tags, in passive and semi-passive modes for different applications, are introduced in the next two chapters.

Chapter 3

Passive UHF/UWB RFID Tag with Printed Electrochromic Display

This chapter describes the design of the passive UHF/UWB RFID tag integrated with an inkjet-printed polyimide EC display. A duty-cycling dual-supply power management unit and a single-pixel addressing display driver are designed to drive the UWB transmitter and the EC display by the energy harvested from the reader. The design is implemented in 3.4 mm²-sized UMC-0.18 μm CMOS technology. This sort of tag is low power and low cost, and can be utilized for industrial applications where display is updated at ultra low frequency.

3.1 State-of-the-art Tags with EPD

From the application aspect, most of the existing researches for tags with EPD focus on the applications of image displays utilized in the standalone handheld devices [34, 48, 49]. However, there are very few researches target the applications of label displays integrated with the wireless intelligent devices such as UHF RFID tags.

From the low power design aspect, though the average power consumption for driving display have been significantly reduced due to the EPD technologies introduced in Chapter 2. The transient power consumption for switching EPD display still surpasses the driving ability of the state-of-the-art passive UHF RFID tags. Driving ability of conventional passive UHF RFID tag which works at several meters operating range is 10s of μW [20–23], while transient power consumption for switching EPD displays is at least 100s of μW [50, 51]. As a result, the existing works compromise by either integrating the display in near field communication (NFC) RFID tags [52, 53] or adding battery to far-field tags working at UHF RFID

or 2.4 GHz industrial, scientific and medical (ISM) bands [54–56], either limiting system applications or increasing system cost.

From the tag flexibility aspect, though there have been progresses in researches integrating EPD with organic thin film transistors (TFTs) circuits to realize fully printed and flexible active-matrix display circuit [49, 57–59], most of them are still under development progress. Comparatively, the heterogeneous integration of silicon chip with flexible substrate and flexible components is much more mature. The most popular method is using metal bumps in conjunction with anisotropic conductive adhesives (ACA) [11]. An ACA is a conductive polymer with carefully adjusted proportions of metal and binder so that the material is conductive when compressed and cured but not in its default state [11]. Such method is self-alignment and requires low temperature adorbable by normal flexible substrate materials. Therefore, for the applications of label display by RFID tags where low cost and stability are more important factors, flexible passive-matrix display integrated with conventional silicon chip is a more suitable design than active-matrix display with switching organic TFTs.

From the communication efficiency aspect, as discussed in Chapter 2, UWB impulse radio (UWB-IR) shows shorter inventory time when accessing multiple numbers of tags due to its ultra narrow pulse width and higher data rate. Therefore, it is expected to design a low power passive tag which replaces UHF RFID backscattering with UWB-IR transmitter.

Therefore, passive UHF/UWB RFID tag with inkjet-printed flexible display is demanded.

3.2 Tag Architecture and Power Management

The architecture of the passive UHF/UWB RFID tag, illustrated in Figure 3.1, consists of a power management unit (PMU), an UHF RFID receiver, an UWB-IR transmitter, a display driver, a data recovery block, a clock generator and the baseband circuitry. The reader powers up and programs multiple tags by UHF RFID signals using amplitude-shift keying modulation with pulse-interval encoding (ASK-PIE). Tags use PMU to harvest the energy and regulate supply voltages. Tags reply the local information by UWB signals. An inkjet-printed EC display on polyimide substrate is interconnected with the chip.

3.2.1 Power Management Scheme for UWB Transmission

UWB transmission consumes high instantaneous power when generating pulses, and the current consumption surpasses the driving ability of the PMU in passive UHF RFID tags. Yet, UWB transmission shows features of high active power and low transmission energy because of high data rate and ultra-short pulse width. And according to the protocol described in [60], its operation duty cycle can be very low, i.e. UWB transmission together with its clock generator can be disabled after reader

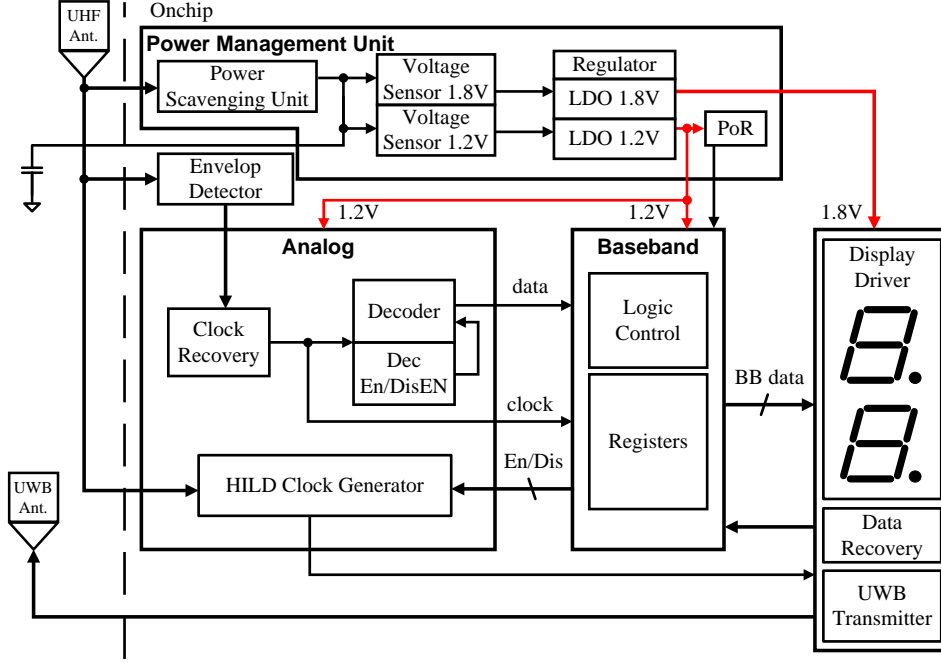


Figure 3.1: Architecture of the passive UHF/UWB RFID display tag. *Adapted from Paper VI.*

acknowledges its transmitted data packet. Therefore, a duty-cycling PMU can switch off the high load current from UWB transmission during power scavenging, and switch it on for one burst of UWB transmission only when enough energy has been accumulated for one complete packet [61]. The principle is illustrated in Figure 3.2 (b). In this power management scheme, it is the power consumption, or in other representation, the load current of voltage sensor ($I_{V_{sen}}$) rather than UWB transmission that limits the tag sensitivity (the minimum input UHF RF power for powering on), besides the powering up currents of the CMOS diode of the voltage rectifier. A duty-cycling PMU is therefore proposed as shown in Figure 3.2 (a). Two voltage sensors switch two regulators separately according to the rectified voltages (V_{rect1} , V_{rect2}) over the storage capacitors, which represents the available energy. The regulators generate 1.2 V supply for the core circuit and 1.8 V for UWB transmitter and display output buffers when V_{rect} is high enough and voltage sensors are switched on.

The voltage sensor for the 1.2 V regulator is added as a bonus for further improvement of system sensitivity when both UWB and display are disabled according to reader commands. In the duty-cycling case, outputs of voltage regulators will

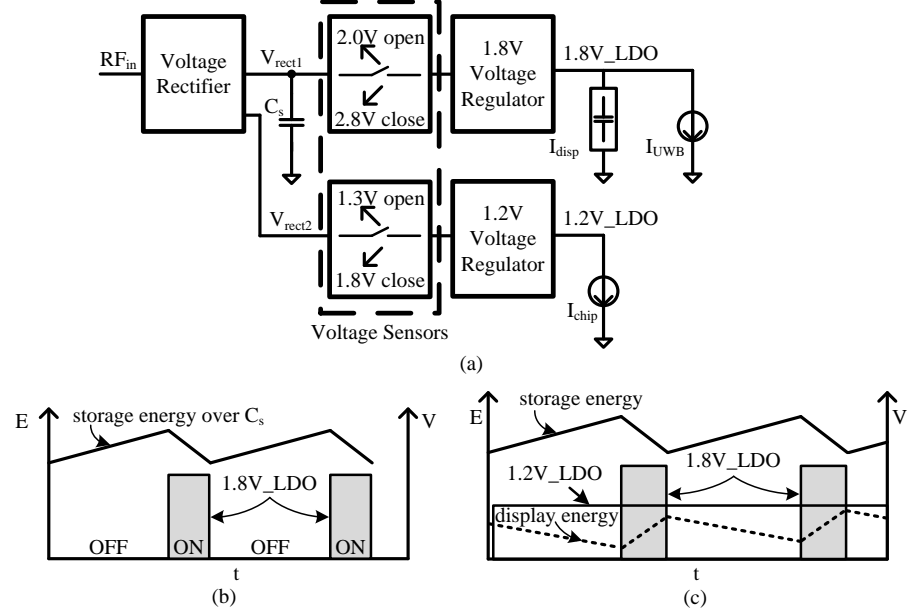


Figure 3.2: Duty-cycling dual-supply PMU. Block diagram of PMU (a), PMU outputs with duty-cycling scheme (b), PMU outputs and display energy with dual-supply duty-cycling schemes (c). *Adapted from Paper VI.*

toggle between the predefined values during operating and zero value during rectifier charging. Dual supply design is motivated by that power consumption scales down as supply voltage does, and that the other circuits of the tag can function with lower voltage. The third motivation is introduced in the next paragraph of power management for display driving.

Critical parameters as follows are defined for UWB transmission: expression eqs. (3.1) to (3.3) analyze how much C_s , V_H and V_L are needed for UWB transmission specifications, where V_H and V_L are rectifier threshold voltages when voltage sensor switches on and off, I_{out} is the output current of the voltage rectifier, I_{UWB} is the current consumption of the UWB transmitter, V_{reg} is the output of the 1.8 V voltage regulator, f_p is the UWB pulse rate, t_{tx} is the transmission time of one burst of transmission packet, and E_0 is the energy consumption per pulse. C_s is divided by E_0 to normalize energy per pulse achieved in different designs. Increasing C_s can provide more transmission power (P) at the cost of more power scavenging time.

$$C_s \cdot (V_H - V_L) = I_{out} \cdot t_{tx} \quad (3.1)$$

$$I_{UWB} = \frac{P}{V_{reg}} = \frac{E_0 \cdot f_p}{V_{reg}} \quad (3.2)$$

$$\therefore \frac{C_s}{E_0} > \frac{f_p \cdot t_{tx}}{V_{reg} \cdot (V_H - V_L)} \quad (3.3)$$

Hence, the following on-off switching voltage pairs are set for the two voltage sensors: 2.8 V and 2.0 V for 1.8 V voltage sensor; 1.8 V and 1.3 V for 1.2 V voltage sensor. C_s is set 221 nF for fixed burst energy with scalable pulse rates.

3.2.2 Power Management Scheme for Display Driving

The power and energy consumption performance of EC display is different from that of UWB transmission, and leads to three extra challenges. The following paragraph introduces the power management schemes for EC display driving.

3.2.2.1 Duty-cycling dual-supply PMU for display energy accumulation

This paragraph discusses the first challenge and solution. Different from UWB transmission, switching energy of EC display is at several hundreds $\mu\text{J}/\text{cm}^2$ scale as shown in Figure 2.7 (b), much higher than the energy amount that can be stored in a feasible-sized capacitor. However, based on the analysis in section 2.2.3.1, EC display works as a large capacitive load and the discharging current is low. Therefore it is possible to accumulate display switching energy over multiple cycles of the duty-cycling PMU. Yet, to be noticed, due to the constant self-discharging behavior of EC display, the discharging electric charge (Q) should be less than the charging Q obtained from the input RF power for each operation cycle to realize positive energy accumulation. Therefore, for display driving, tag sensitivity is further limited by the averaged discharging current of EC display. Figure 3.2 (c) illustrates the above discussions. Tag sensitivity for display driving is deduced from eqs. (3.4) to (3.6) and shown in equation 3.6. I_{chg} is the display charging current, I_{dis} is the display discharging current. t_{rect_dis} is the rectifier discharging i.e. display charging time, and t_{rect_ch} is the energy harvesting time. t_{rect_ch} is in proportional to the equivalent input impedance of the voltage rectifier of which the voltage sensor is the only load it has during energy harvesting. I_{rect} , I_{vsen} , I_{vreg} are the current consumptions of the voltage rectifier, the voltage sensor and the voltage regulator. η is the factor of the averaged rectifier output voltage over the 1.8 V regulator supply voltage. I_{in} is the input current to the tag. V_{reg} is the output of the 1.8 V voltage regulator. In this case, tag sensitivity is further limited by $\frac{I_{dis} \cdot (\eta \cdot I_{vsen} + I_{vreg} + I_{chg})}{I_{chg} - I_{dis}}$; the higher the I_{dis} , the higher the required P_{in} .

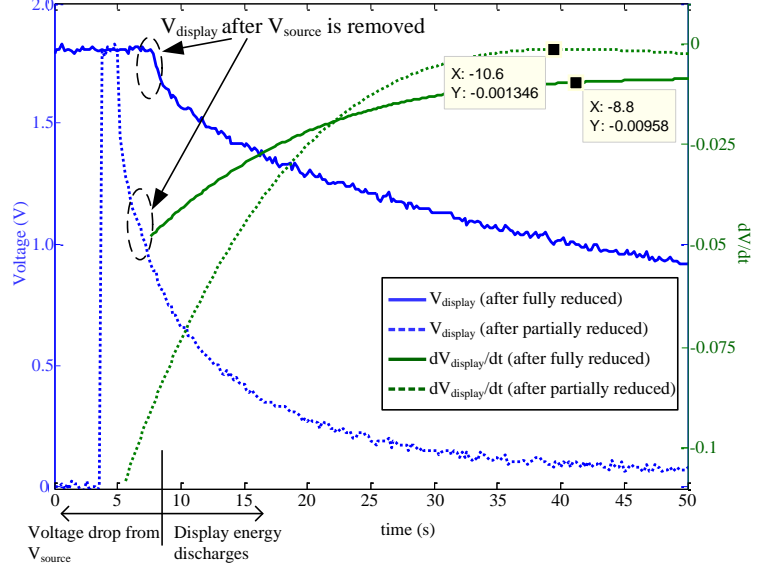


Figure 3.3: Measured discharging behavior of a 22-mm² EC display. *Adapted from Paper VI.*

$$I_{chg} \cdot t_{rect_dis} > I_{dis} \cdot (t_{rect_ch} + t_{rect_dis}) \quad (3.4)$$

$$(\eta \cdot I_{vsen} + I_{vreg} + I_{chg}) \cdot t_{rect_dis} = (I_{in} - I_{rect}) \cdot t_{rect_ch} = C_s \cdot (V_H - V_L) \quad (3.5)$$

$$\therefore (I_{in} - I_{rect}) > \frac{I_{dis} \cdot (\eta \cdot I_{vsen} + I_{vreg} + I_{chg})}{I_{chg} - I_{dis}} \quad (3.6)$$

To evaluate the value of discharging current (I_{dis}), the transient discharging voltages of EC display are measured. I_{dis} is extracted by the voltage discharging speed of a 22 mm²-sized display cell as shown in Figure 3.3. Averaged I_{dis} is obtained by averaging the amount of $C \cdot \frac{dV_{display}}{dt}$, and the C is evaluated by $E = C \cdot V^2$ of which E is the switching energy that fully reduce EC display. The beginning part of $V_{display}$ falling is just the voltage drop from V_{source} , and does not represent the real display energy discharge. As results, the averaged I_{dis} is evaluated around 28.4 $\mu A/cm^2$ [62].

The second challenge is that display switching energy has to be accumulated over multiple PMU cycles and thus display driving must also be controlled over multiple PMU cycles; however, the voltage regulator which generates the chip supply voltage is switched off during energy harvesting period of each PMU cycle. As a result, the chip loses power and any state control during these time intervals. The dual-supply design of the duty-cycling PMU helps to solve this issue. As shown in Figure

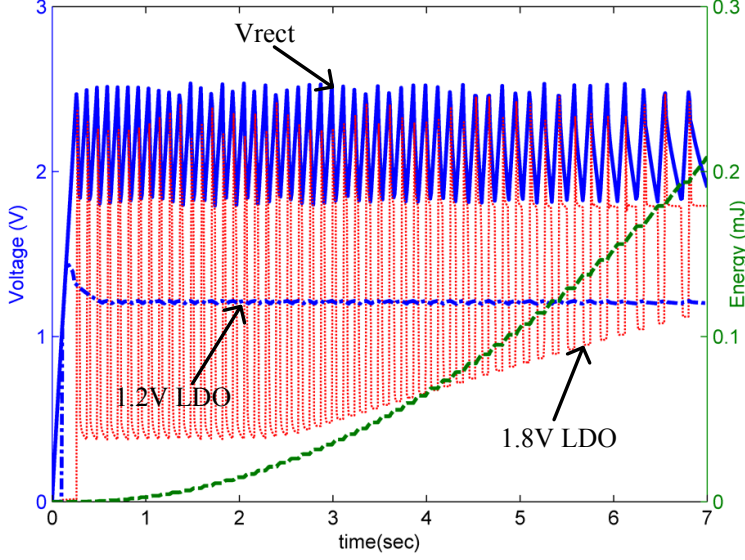


Figure 3.4: Simulated outputs of voltage rectifier, 1.2 V voltage regulator and 1.8 V voltage regulator during display energy accumulation. *Adapted from Paper VII.*

3.2 (a), two voltage sensors switch two voltage regulators separately. Because the switch-off voltage for the 1.8 V voltage regulator is 2.0 V, higher than the switch-on voltage for the 1.2 V voltage regulator which is 1.8 V, the 1.2 V supply is kept stable and hence the core tag functions can be uninfluenced throughout the display switching over multiple PMU cycles. The concept is shown in Figure 3.2 (c). The corresponding simulation results are illustrated in Figure 3.4. This is the third motivation for dual-supply design of the duty-cycling PMU.

3.2.2.2 Single-pixel addressing

The third challenge for display switching is that as display area increases, so does display discharging current (I_{dis}), and in turn, the required input RF power. Increasing C_s cannot solve the problem effectively because t_{rect_ch} and thus the discharging Q also increase linearly as C_s does. Additionally, over-sized C_s impairs tag substrate flexibility benefit from the polyimide EC display, increasing the complexity for attaching the tag with ubiquitous objects. One intuitive solution to keep the tag sensitivity regardless of display area is employing a so-called single-pixel addressing scheme so as to confine the simultaneously-addressed display size as small as possible, for example 1 cm^2 . As illustrated in Figure 3.5, first with the cooperation from manufacturer, one big display pixel is divided into several minimized pixels; secondly, the pixels are addressed one by one (Figure 3.5 (a)) instead of row

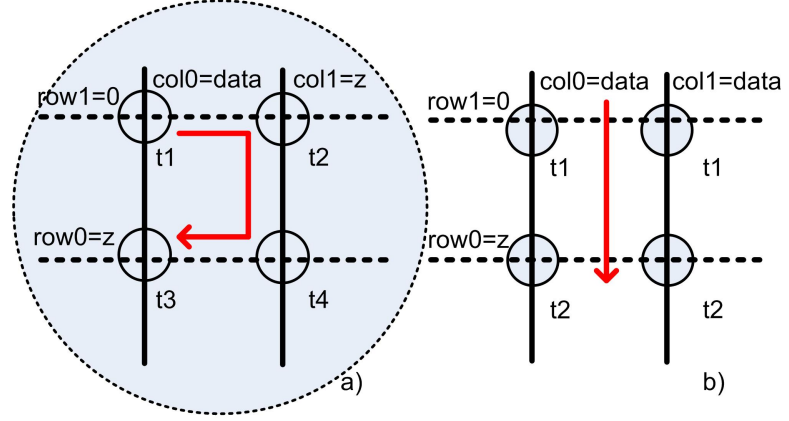


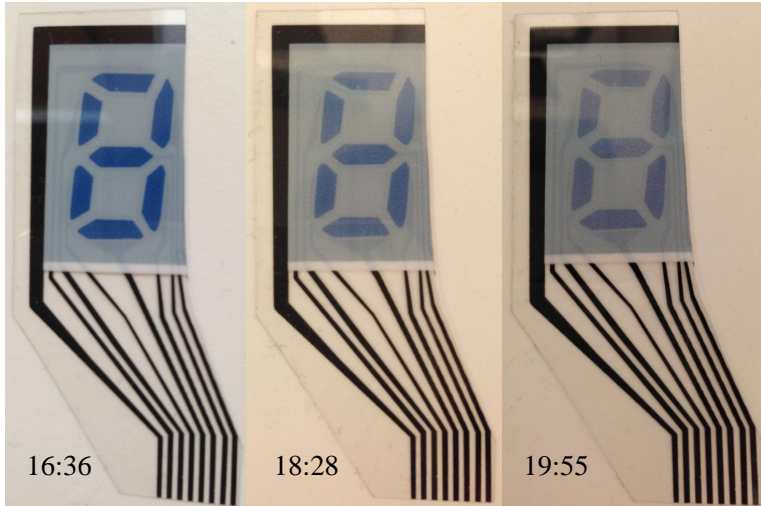
Figure 3.5: Pixel size minimization and single-pixel addressing (a) VS conventional row-to-row matrix addressing method (b). *Adapted from Paper VII.*

by row as conventional matrix addressing method does (Figure 3.5 (b)). In this case, I_{dis} only corresponds to the discharging current of one minimized pixel.

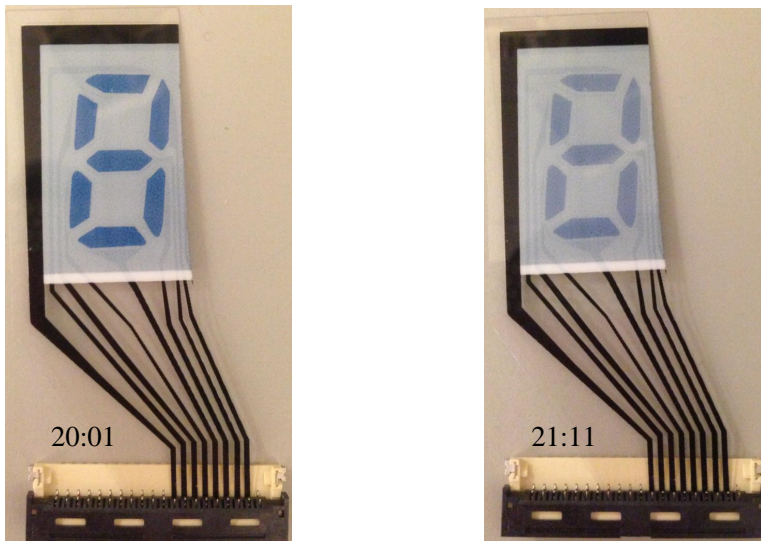
The apparent disadvantage of single-pixel addressing is much-prolonged display refresh time. It will cause huge problem when refreshing the conventional display such as LCD and LED because the display materials are not bi-stable, and thus the refresh time should be less than human visual reaction time. However, EC display, owing to its bi-stability when active material PEDTO:PSS is driven in reduced state, can afford such a far-prolonged time, as long as it is smaller than its retention time. Correspondingly, Figure 3.6 (a) demonstrates the retention time by showing the color status of display samples as time passes from 16:36 to 19:55. Taking material aging of the printed EC display into consideration, the retention time decreases as application time goes on. Figure 3.6 (b) shows the comparative color status of the display samples after three years of application. The time for color to fade out decreases to about 1 hour after three years; however, for display size at the scales for electronic shelf label, the time for color to fade out is still long enough for the single-pixel addressing scheme.

3.3 Circuit Implementation

This section describes the circuit implementation of several key blocks: duty-cycling dual-supply PMU, EC display driver and the data recovery with EC display, UHF-RFID receiver, UWB transmitter and UWB clock generator.



(a) Color changes of display sample after 1-year application



(b) Color changes of display sample after 3-year application

Figure 3.6: Inkjet-printed EC polyimide display color changes VS time. *Adapted from Paper VI.*

3.3.1 Duty-Cycling Dual-Supply PMU

The PMU based on the design in [61] includes one rectifier, two voltage sensors and two regulators for 1.2 V and 1.8 V dual-supply respectively, as well as a reset

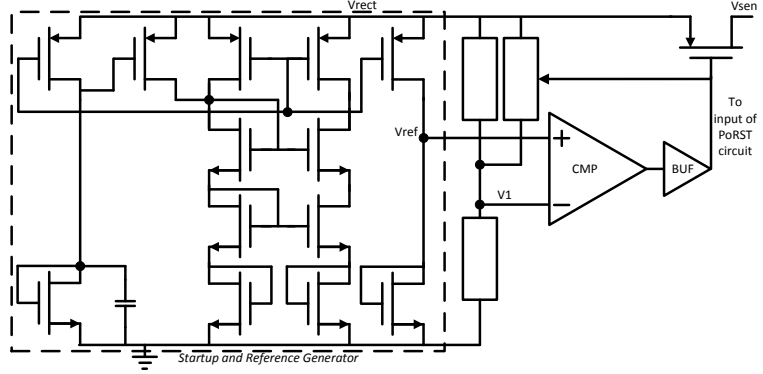


Figure 3.7: Schematic of voltage sensor. Adapted from Paper VI.

generator.

As discussed before, voltage sensors are the only operating parts of the chip in energy harvesting phase and impacts the tag sensitivity directly. Figure 3.7 shows the schematic of the voltage sensor, which includes a reference voltage generator, a voltage comparator and a power switch. A resistor based bandgap structure requires large resistors in order to reduce power consumption, resulting in increased silicon size [63]. Therefore, a CMOS based reference voltage generator is utilized in this work [64]. The different comparison thresholds for switching on and off the voltage sensor are achieved by the following design. During the rising process of V_{rect} , the control voltage of the switch is not zero when the switch is off. During the falling process of V_{rect} , since the control voltage of the switch is low when the switch is on, the control voltage feedbacks and adds more current to the bottom resistor of the voltage divider path compared to that during the rising process of V_{rect} . Thus it changes the equivalent divide ratio of the voltage divider, making the output of the divider during the falling process higher than that during the rising process of V_{rect} . As a result, the comparator output does not toggle from high to low until V_{rect} falls to an even lower voltage. The switching on and off threshold voltages for the 1.8V and the 1.2 V voltage sensors are obtained by using the same structure but sizing the dividing resistors differently [62].

Low-drop-out (LDO) voltage regulators are used because of the low power consumption. Schematic of the 1.8V LDO with driving its loads is shown in Figure 3.8. Schematic of the 1.2 V LDO is same in structure. The same structure of the voltage reference generator in the voltage sensor is re-used.

During display charging, duty-cycling operation of the 1.8V LDO regulator is affected by the instantaneous charging current I_{disp} . If I_{disp} is higher than the regulator driving ability in ultra low input RF power cases, from the PMU circuit viewpoint as illustrated in Figure 3.8, a large part of the regulator output current

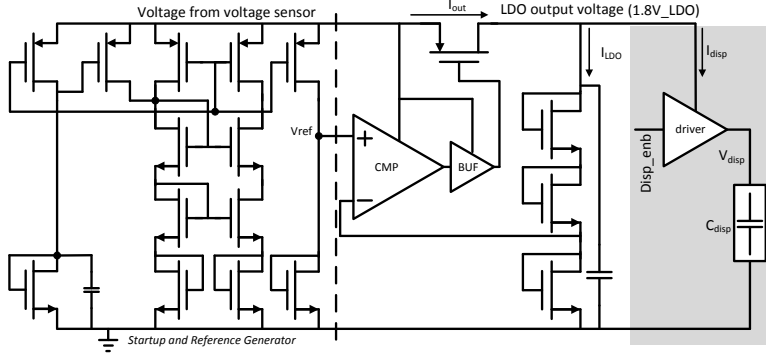


Figure 3.8: Schematic of LDO voltage regulator. *Adapted from Paper VI.*

(I_{out}) is used as I_{disp} , leaving very small remainder (I_{LDO}) flowing through the three diode-connected NMOS transistors at the output of the regulator. In this case, the three transistors cannot work in the saturation region but in the linear region, causing 1.8V_LDO to be lower than 1.8 V. However, as long as the discharging Q is less than the charging Q for each operation cycle, the energy over the EC display will gradually be accumulated over multiple duty cycles, and I_{disp} will decrease as energy increases. Therefore, I_{LDO} will increase and so will 1.8V_LDO. In the final stable state, the entire switching display energy is achieved, and the regulator output stabilizes at the predefined 1.8 V. Due to the duty-cycling operation, 1.8V_LDO, instead increasing linearly, will hop between two values corresponding to the switching on and off states during its rising period to 1.8 V. Known from the previous discussion, the high value of 1.8V_LDO during switching-on state is determined by I_{disp} , and the low value is determined by the discharging speed of the EC display during switching-off intervals. These discussions are verified in the experimental results in the next section.

3.3.2 Display Driver and Data Recovery with EC Display

- Display driver

A digital driver is selected to save circuit complexity. When the display is disabled, the driver is disconnected from display and the display clock controlling the display charging period is also disabled to save power. When the display is enabled, the driver addresses the EC display one pixel by another. The pixels not addressed are connected to high impedance (high-Z). To remove the old image due to the bi-stability and the long retention time of EC display, when tag is reset or when a different packet of display data is received via UHF RFID link, the drivers reversely connect all the pixels (connect all rows to the 1.8 V supply voltage and connect all columns to ground)

for t_{chg} time prior to refreshing the display. After clearing the old image, the driver follows the single-pixel addressing scheme and addresses each pixel for t_{chg} . t_{chg} is the required time to switch a pixel into the complete reduction state. According to previous tests [38, 39], the time to clear a fully-reduced display is approximate to that of switching it to the reduced color state. Since t_{chg} increases as input UHF RF power decreases, a programmable counter is implemented in the display clock generator.

- Data recovery

To reduce tag complexity and power consumption, the proposed tag is not integrated with non-volatile memory (NVM) such as Flash. Yet the capacitive feature and the long retention time of EC display can be used to supply the data registers when tag is accidentally powered off and recover the data when re-powered on. Tag is therefore more robust to temporary power loss due to non-ideal factors in real applications such that tag antenna position is moved to “blind area” temporarily.

There are several solutions to recover data by EC display cell. The most simple and stable solution is illustrated in Figure 3.9 (a). One display sample (EC Display) is used as an energy storage capacitor. When tag is powered on, transistor M1 is switched on and the supply voltage for data memory ($V_{\text{supply_disp}}$) is one n-channel MOS (NMOS) threshold voltage lower than 1.8 V supply voltage. Since core circuits such as digital baseband are all supplied with 1.2 V, so the one threshold voltage loss does not impact circuit operations. When tag is powered off due to lack of UHF carrier wave or reader command, M1 is off and $V_{\text{supply_disp}}$ discharges through the equivalent capacitor and resistor of the EC display cell. Apparently, the bigger the display cell, the longer the $V_{\text{supply_disp}}$ discharging time. Memory data are saved if $V_{\text{supply_disp}}$ is higher than a threshold value around 100 mV when tag is re-powered on. Figure 3.9 (b) demonstrates the test result. The display register bit for Col [0] is stored with value “1” before tag is powered off. During powering off intervals, $V_{\text{supply_disp}}$ gradually discharges. When tag is powered on again, the voltage of $V_{\text{supply_disp}}$ is still higher than 100 mV. As a result, the display register bit for Col [0] recovers to its previous “1” value 22 seconds after tag is powered on. The time interval between the rising edges of $V_{\text{supply_disp}}$ and Col [0] is because tag starts with reset state and display works to remove the old image first after power on reset.

3.3.3 UHF RFID Receiver

Reception (RX) block is composed of envelope detector, envelope recovery and data decoder. The envelope detector shares the similar structure with the voltage rectifier circuit but with 2 stages and different parameters to extract the original envelope. The subsequent envelope recovery shifts it to rail-to-rail voltages for global clock recovery and data decoding [61].

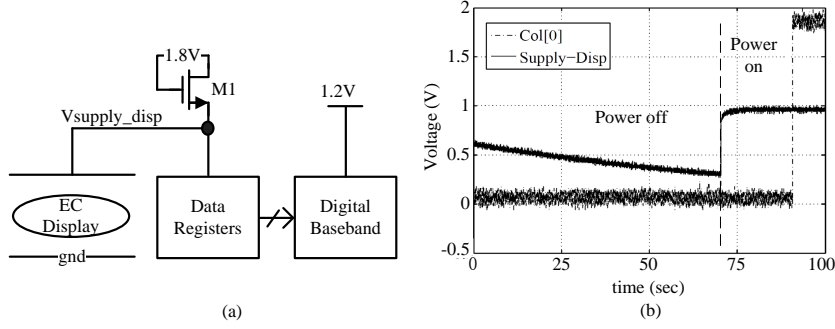


Figure 3.9: Data recovery by EC display: (a) Block diagram (b) Test result.

In data decoding, a decoder-enable block disables the decoder when a high interval of over $40 \mu\text{s}$ is detected in the envelope, and enables it when a falling edge of the envelope is detected. The disable signal switches on and off the bias current for the decoder block. Taking the response time or setup time of the current generator into account, the first two decoded bits in the received package are the redundant bits. The disable signal also serves as the reset for the cyclic redundancy check (CRC) and ID check in baseband control logics which generates a renew signal once the check is correct. The renew signal triggers the data to the baseband registers in this clock period.

To reduce power compared to conventional digital counter which counts the high interval with high frequency clocks, both data decoder and decoder enable blocks utilize clock-free analog integrators which linearly charge capacitors when the envelope is high [65].

3.3.4 UWB Transmitter and UWB Clock Generator

Digital pulse generator, up conversion or Finite Impulse Response (FIR) transmitter is not feasible, since they require on-chip high frequency clock and consume high power consumption [66, 67]. In this work, therefore, digital-dominant architecture of a filtered edge combiner UWB-IR transmitter is presented as shown in Figure 3.10. UWB pulse is generated by the edge combiner in an order of hundreds of ps. A driver stage is used to drive the pulse magnitude and to match the output filter.

Both duration and amplitude of the output pulse are tunable by two control inputs to compensate process, voltage and temperature (PVT) and frequency response of the antenna. On the other hand, it offers the ability to trade-off among performances of data rate, output power, power consumption, and operation range. Amplitude and duration controls enable the module to adjust the transmitted signal to meet bandwidth and power regulations. For example, high data rate is chosen for shorter communication range whereas high amplitude for longer range.

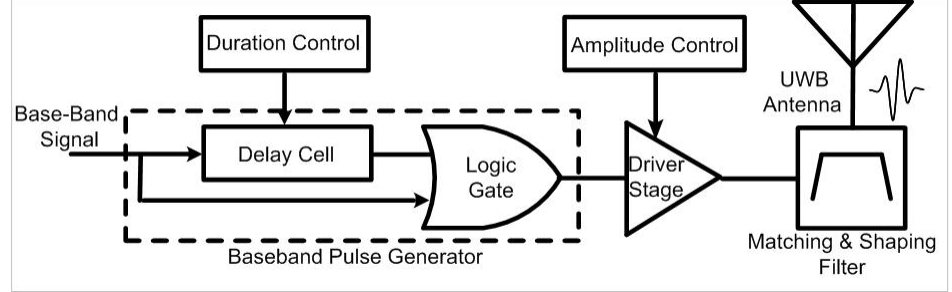


Figure 3.10: Block diagram of the UWB-IR transmitter [68].

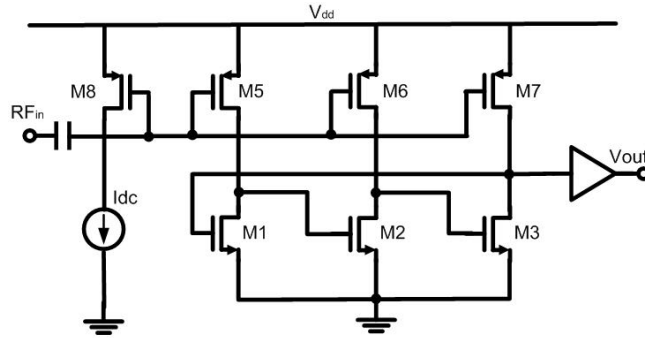


Figure 3.11: Block diagram of one stage of HILD. Adapted from Paper VI.

Furthermore, the ultra-short pulse duration of hundreds of ps allows accurate positioning and ranging [69,70], and high-swing UWB pulse with longer pulse repetition interval is adjusted to prevent the inter-pulse interference in positioning [69].

Compared to the relaxation oscillator specific to KHz frequency range and the ring oscillator vulnerable to PVT, a harmonic injection-locked divider (HILD) is selected to achieve high operation frequency along with low power consumption for the UWB transmission clock. Injection locking happens when a source oscillator is disturbed by an injector operating at a nearby frequency. If the injection is strong enough and their frequencies near enough, it will lock the source oscillator. Otherwise it will “pull” the source and produce unwanted modulation [71]. Making use of the injection locking, one stage of divide-by-three HILD is shown in Figure 3.11. It is fundamentally an oscillator with free-running frequency at the sub-harmonic frequency of the input RF signal and locked in by the received UHF carrier wave. Since the UWB clock of the tag is both frequency-locked and phase-aligned to UHF carrier wave from reader, the synchronization between tags and the reader is significantly simplified. The UWB clock that triggers the UWB baseband data is generated by two stages of HILD and four stages of digital dividers. UHF

carrier wave is divided by 9 times with the two HILD blocks, and subsequently divided by a series of digital dividers. The digital dividers are programmable to adjust the data rates of the UWB transmission.

3.4 Experimental Results

Implemented in $0.18\ \mu\text{m}$ CMOS process, the chip photo is shown in Figure 3.12. Excluding the circuit blocks for other projects, the proposed chip occupies $3.4\ \text{mm}^2$ area.

The chip is packaged with Quad Flat No-leads (QFN) 64 and is mounted on a test PCB. UHF-RFID and UWB communications are tested with connections to SubMiniature Version A (SMA) cables. The printed polyimide EC display is connected by a flexible printed/flat cable (FPC/FFC) BackFlip Housing of which one side of the connection is compatible to conventional PCB pins and the other side can clip the flexible display and conduct currents via the clips. This works use two seven-segment display samples and connect them such that the columns are connected together and the grounds are connected with row [0] and row [1] respectively to emulate the general matrix display.

3.4.1 UWB Transmission Powered by UHF Energy Harvesting

To measure the tag sensitivity with UWB transmission, VNA (Rhode & Schwarz ZVM) is used to measure the minimum powering-up power and the reflection coefficient S11 between the VNA and the tag. Considering the S11 value, the powering-up sensitivity of $-18.5\ \text{dBm}$ is tested for the UWB transmission in burst mode. Off-chip storage capacitor with $211\ \text{nF}$ value is connected at the load of the voltage rectifier. Figure 3.13 (a) shows the transient results of PMU outputs at 2 Mbps

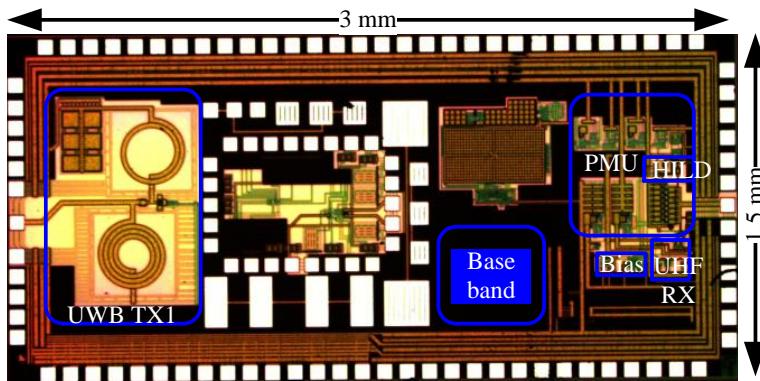


Figure 3.12: Chip photo of the passive UHF/UWB RFID display tag. *Adapted from Paper VI.*

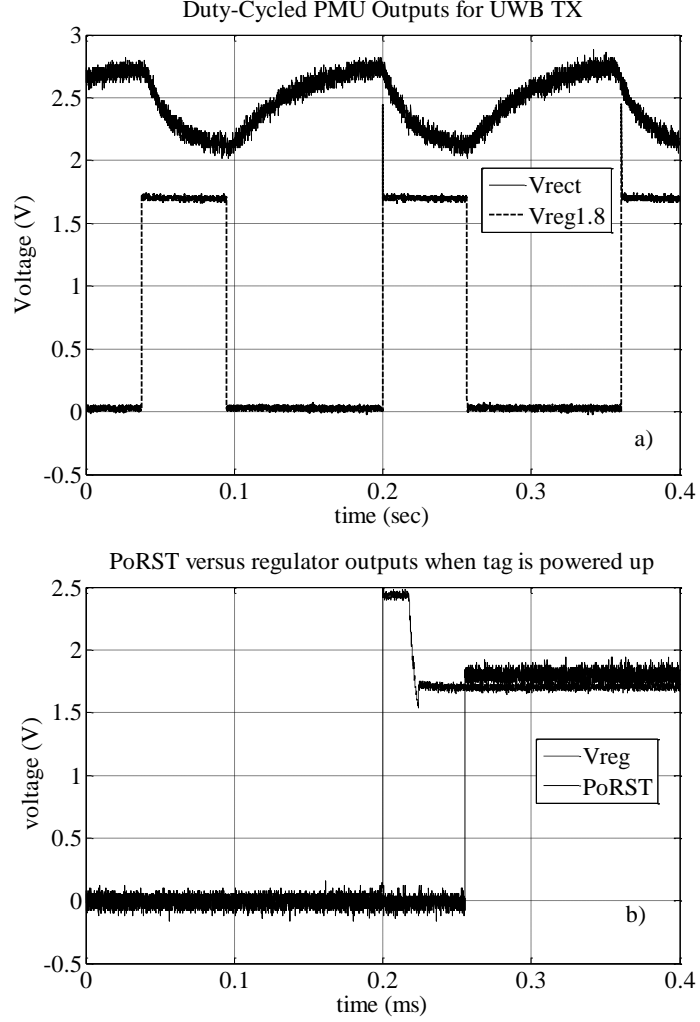


Figure 3.13: PMU outputs for UWB transmission @ 2 Mbps pulse rate: (a) output of voltage rectifier and 1.8 V voltage regulator; and (b) output of 1.8 V voltage regulator and PoRST. *Adapted from Paper VI.*

UWB transmission pulse rate. At 2 Mbps pulse rate, the charging time is 104 ms and the operation time (the period of one burst of UWB transmission) is 56 ms, equaling to a 35% duty cycle. At 10 Mbps pulse rate, the operation time is 11.2 ms, and the duty cycle is 7%. A maximum number of 112000 bits can be transmitted in one transmission burst at 0 dB processing gain. As shown in Figure 3.13 (b), a PoRST is delayed around 55 μ s to reset the circuit after V_{reg} is stable.

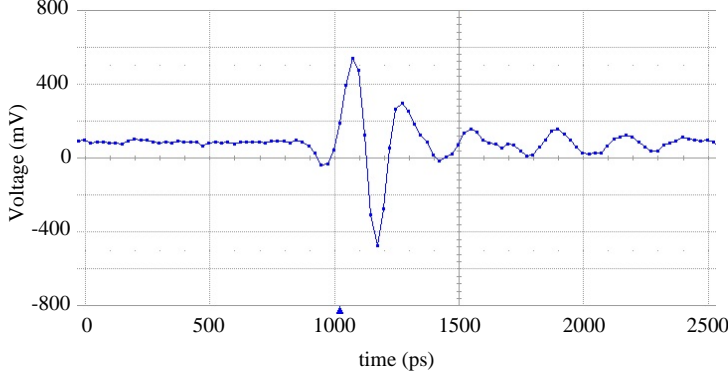


Figure 3.14: UWB transmitted pulse in the time domain. *Adapted from Paper VI.*

The impulse of the UWB transmitter has the amplitude of $1.02 V_{pp}$ and the duration of 900 ps as illustrated in Figure 3.14. The -10 dB bandwidth is 3-5 GHz. Measured by Keithley-2440, it consumes $36 \mu W$ at 2 Mbps pulse rate, corresponding to 18 pJ/pulse.

3.4.2 EC Display Driving Powered by UHF Energy Harvesting

The transient outputs of the voltage rectifier and the 1.8 V voltage regulator with different energy storage capacitors and after different display charging periods are measured and comparatively illustrated in Figure 3.15 [62]. It demonstrates the display switching energy accumulation with the duty-cycling PMU. The rectifier charging time is in proportional to the value of the storage capacitor, similar as the case in UWB transmission. However, different from UWB transmission, the display switching energy is accumulated over multiple duty cycles under the premise that charging Q is larger than discharging Q in every cycle.

In order to measure the tag sensitivity with display driving function, small input UHF RF power is used. During display energy accumulation, when the tag input current is smaller than the ideal peak instantaneous display charging current, output stage of the 1.8V_LDO regulator does not have enough current to operate in the transistors in the saturation region and thus outputs smaller voltage than 1.8 V (the blue curve marked with “1.8V_LDO”). As the display energy increases, the charging current decreases, and its discharging voltage level during power scavenging phases increases, gradually enabling the voltage regulator to operate “normally” (the red curve marked with “1.8V_LDO”). A more general overview of the voltage of 1.8V_LDO throughout display switching can be referred to Figure 3.17. Additionally, 1.8V_LDO discharges much slower in display function than in UWB transmission during power scavenging phases, because the equivalent capacitance of EC display samples is much larger [36, 38, 39].

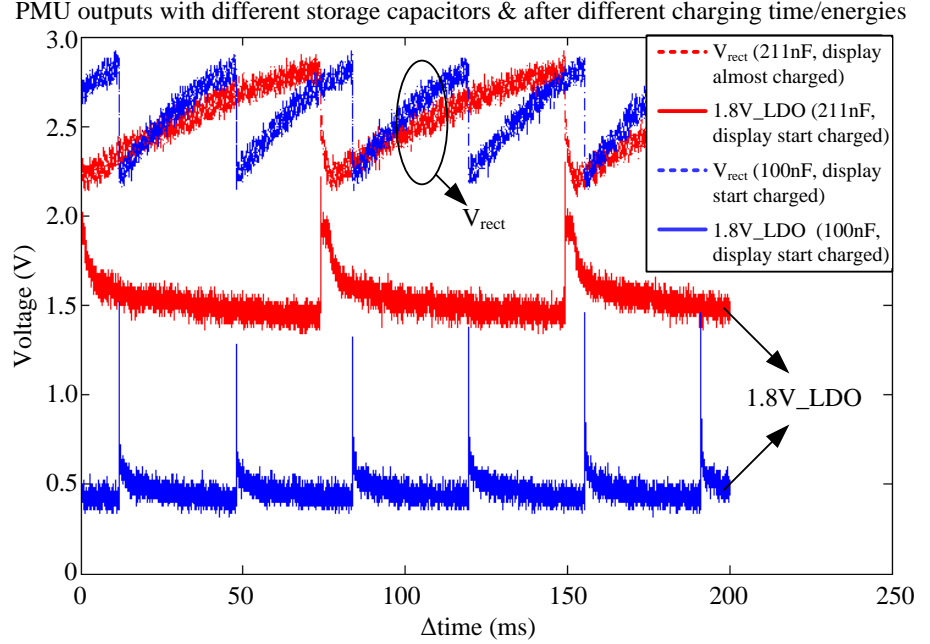


Figure 3.15: Outputs of the voltage rectifier and the 1.8 V voltage regulator with different storage capacitors and after different display charging time/energies for low input RF power: (blue curve represents shorter time and less energy; red curve represents longer time and almost fully-charged energy). *Adapted from Paper VI.*

As a comparison, Figure 3.16 demonstrates the outputs of PMU in test cases when input UHF RF power is much increased. In this case, the input current is larger than the ideal peak instantaneous display charging current, enabling the transistors in the output stage of the 1.8V_LDO regulator to operate in the saturation region and outputting 1.8 V.

Figure 3.17 shows the refresh time for the 7-segment display versus the input driving current which is measured by Keithley-2440 through the 1.8 V regulator supply and recorded by Labview [62]. This test demonstrates the results of the combined power management solution of single-pixel addressing scheme and duty-cycling PMU scheme. Limited by the available EC display samples, the minimized pixel size is around 22 mm², which is the size of one segment.

When the display is addressed one segment by one with 2.5-sec charging time for each to reach the reduced color state, the entire 1.5 cm² (lighting all 7 segments) display can be refreshed by an effective input power of 43.2 μ W (input current of 24 μ A), at approximate rate of 17.5 sec/7-pixel, equaling to 11.7 sec/cm². When rectifier efficiency and power consumption of other tag blocks are included, the

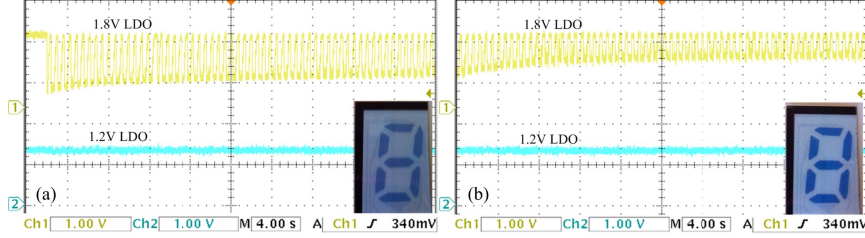


Figure 3.16: Outputs of the 1.8 V voltage regulator after different display charging time/energies for higher input RF power: (a) shorter time/less energy (b) longer time/more energy. *Adapted from Paper VI.*

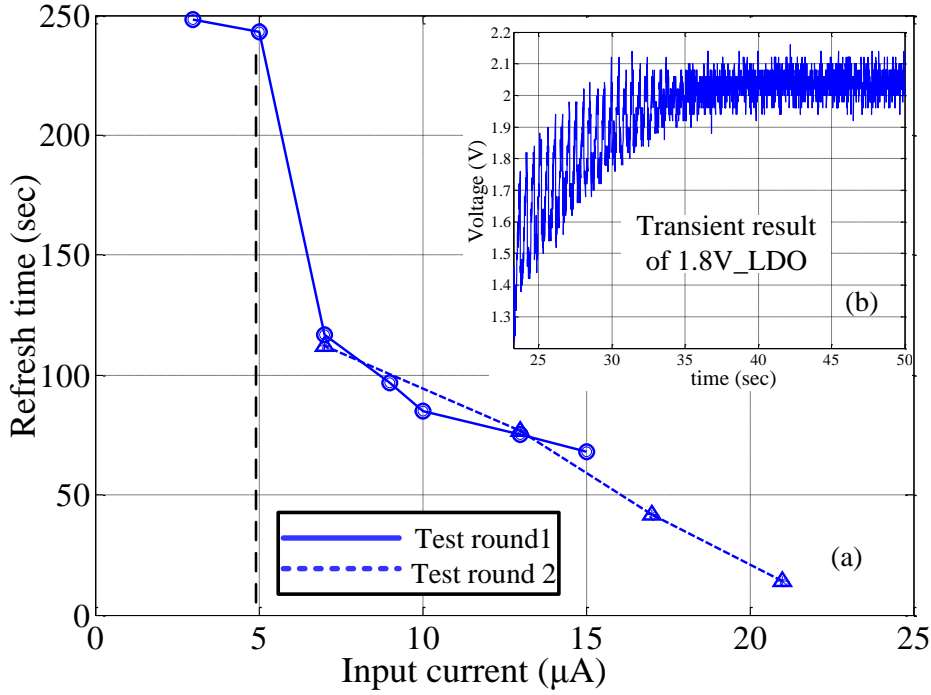


Figure 3.17: Display refresh time VS the input driving current of a 1.5 cm^2 EC display. *Adapted from Paper VI.*

tag sensitivity is approximate -10.5 dBm . As the effective input power further decreases from $43.2 \text{ } \mu\text{W}$ (input current of $24 \text{ } \mu\text{A}$), the refresh time increases as shown in Figure 3.17 because the time to completely charge each segment increases as the available display charging current I_{chg} decreases. When it approaches $9 \text{ } \mu\text{W}$ (input current of $5 \text{ } \mu\text{A}$), the refresh time increases significantly, because the input

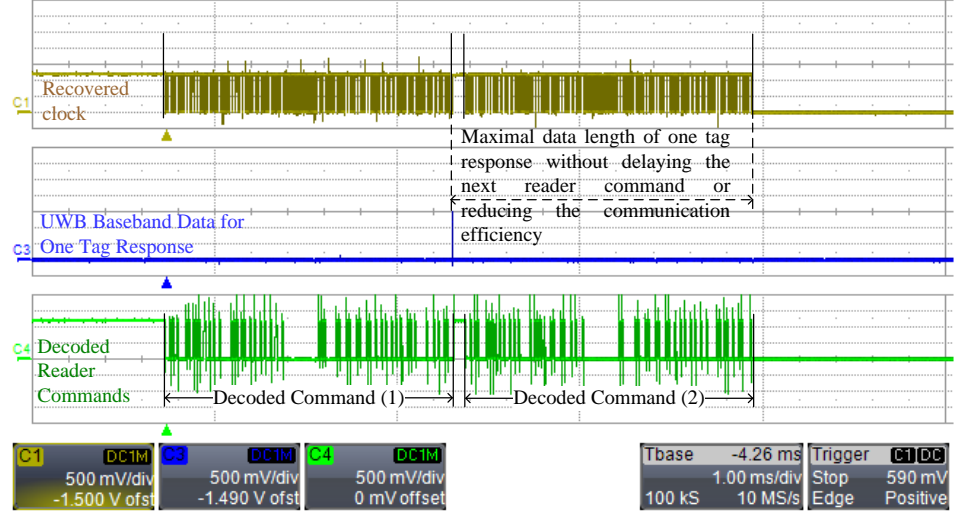


Figure 3.18: Multi-tag communications and the pipeline of tag response with reader command. *Adapted from Paper VI.*

current almost equals the display discharging current which is no less than $6 \mu\text{A}$ for each 22 mm^2 -sized pixel ($28.4 \mu\text{A}/\text{cm}^2$ in section 3.2.2.1), unable to accumulate the positive net Q as discussed in section 3.2.2.1. Therefore, a reasonable effective input power limit for display switching is above $20 \mu\text{W}$.

3.4.3 Reader-to-Tags Communication

Same as RFID communication, tags are written by reader sequentially based on tag ID match. To intuitively show the communication, UWB transmission is activated in the reader command so that tag transmission signals in the oscilloscope can be used to judge whether a read command is successfully received and reacted by the tag. Figure 3.18 demonstrates the related signals of writing tags by the reader write command. When tag ID is matched to the correspondent data in the reader command, tag registers are configured and written, triggering UWB transmission as shown after the command (1); when tag ID is not matched and the command is for another tag, tag ignores the command and thus no UWB transmission is triggered as shown after the command (2).

Compared to UHF backscattering, the communication efficiency is much improved due to the much higher data rate of UWB transmission as demonstrated in Figure 3.19. It is due to both the higher data rate (6.25 Mbps) of UWB transmission shown in Figure 3.19 and the possibility to pipeline tag response and reader command as marked in Figure 3.18 by the improved frame-slotted-ALOHA protocol [60]. The protocol pipelines the reader acknowledgment command and tag data

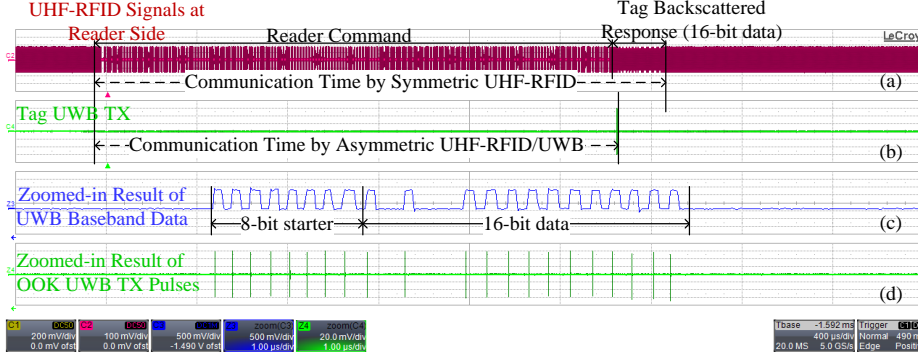


Figure 3.19: Comparison of symmetric (a) and asymmetric (a-b) reader-to-tags communication. UWB-IR transmitted data (c) and UWB-IR transmitted pulse (d) of one tag response in asymmetric communication. *Adapted from Paper VI.*

transmission by making use of the asymmetric UHF reception and UWB transmission. In this demonstration case, the pipeline result is not apparent because the transmitted length of each tag is far smaller than the length of reader command, but for other application cases with long tag transmission length, the pipeline mechanism is much more obvious and helpful.

3.4.4 Tag Performance Summary and Comparison

Figure 3.20 compares the UHF/UWB RFID display tag with other wireless display tags, display drivers and UWB tag [49, 51, 52, 54, 58, 72–74]. For display interface at tag level, this work shows least refresh power consumption at the cost of slowest refresh rate, making it a promising solution for applications requiring low power yet not high refresh rate. The retention power of EC display is around $4 \mu\text{W}/\text{cm}^2$ [38] while that of EP display is reported 0. This is the cost this work pays for the 1.8 V low driving voltage of EC display to avoid the extra power of the charge pump circuits. This work and the tag from Omni-ID [54, 73] are the only reported works that passively drive displays by UHF RFID wave. [54, 73] drives Electrophoretic (EP) display by active-matrix addressing and shows comparable UHF RF sensitivity (-11 dBm) to this work. Yet the off-chip storage capacitor is evaluated at several hundreds of μF scale according to the EP display refresh energy provided in the data sheet [74]. It is much larger than the 221 nF capacitor in this work, making the entire tag more bulky and difficult to integrate with normal objects. For applications where the sensed information of massive tags is transmitted for remote monitoring, the UWB transmitter utilized in this work offers better figure of merit (FoM). The FoM is defined as $\frac{f \cdot A}{P}$, of which f is data rate, A is pulse amplitude, and P is power consumption [72].

		This work	[70]	[71-72]	[52]	[51]	[49]	[57]
Process technology		3.4-mm ² 180-nm CMOS process	0.3-mm ² 130-nm CMOS process	NA	NFC-WI SP board	NA	Amorpho us silicon TFTs on stainless steel substrate	NA
Uplink	Band	3.1 - 10.6 GHz UWB	306 MHz	866 - 928 MHz	13.56 MHz NFC	NA	NA	NA
	Data rate	1 - 10 Mbps	4 Mbps	NA	1.6 - 26.48 kbps	NA	NA	NA
Downlink	Band	902 - 928 MHz	918 MHz	866 - 928 MHz	13.56 MHz NFC	NA	NA	NA
	Data rate	40 - 160 kbps	20 kbps	NA	1.6 - 26.48 kbps	NA	NA	NA
Display	Technology	EC	NA	EP	EP	EP	EP	EP
	Address scheme	single pixel	NA	row-to-ro w AM ^a	row-to-ro w AM	row-to-ro w AM	row-to-ro w AM	row-to-ro w AM
	Driving voltage	1.8 V	NA	NA	15 V	15 V	10 V	15 V
	Refresh power	43.2 μ W @ 11.7 s/cm ² rate	NA	NA	2.0 mW @ 0.82 s/cm ² rate	6.0 mW @ 0.15 s/cm ² rate	3.4 W @ 7 ms/cm ² rate	4.0 mW @ 0.21 s/cm ² rate
	Retention power	4 μ W/cm ² ^d	NA	0	0	0	0	0
	Sensitivity	-10.5 dBm	NA	-11 dBm ^c	NA	NA	NA	NA
UWB	Battery	No	NA	No	No	Yes	Yes	Yes
	TX power	36 μ W @ 2 Mbps ^b	50.6 μ W @ 4 Mbps	NA	NA	NA	NA	NA
	Pulse amplitude	1.02 V ^b	15.2 mV	NA	NA	NA	NA	NA
	Sensitivity	-18.5 dBm	-10 dBm	NA	NA	NA	NA	NA
	FoM	56.7*10 ⁹	1.2*10 ⁹	NA	NA	NA	NA	NA

^aAM: active-matrix

^bResults and detail analysis can be found in [3].

^cStorage capacitor is evaluated at hundreds of μ F scale according to the EP display parameters in [73]. The storage capacitor in this work is 221 nF.

Figure 3.20: Performance summary and comparison with other wireless tags and display tags. *Adapted from Paper VI.*

3.5 Summary

As a conclusion, a passive UHF/UWB RFID tag with inkjet-printed EC polyimide display is implemented in 3.4 mm²-sized UMC-0.18 μ m CMOS technology for the

IoT applications featuring low power, high uplink data rate, and low display refresh rate. Display switching and UWB transmission can be powered as well as programmed by the UHF RFID signals from the reader. This is achieved by two power management schemes: 1) aggressive duty-cycling dual-supply power management unit to accumulate display switching energy over multiple cycles and to enable UWB transmission in burst mode; 2) single-pixel addressing scheme to reduce instantaneous display charging and discharging power by increased refresh period which makes use of the bi-stability of EC display. Measurement results demonstrate the powering-up sensitivity of -18.5 dBm for a scalable 2-10 Mbps UWB transmission, and -10.5 dBm for a 1.5-cm^2 7-segment display switching by 17.5 seconds, which can be further decreased if increased refresh time is permitted by application scenarios.

Chapter 4

Semi-Passive UHF/UWB RFID Tag with Printed ECG Sensor for Healthcare

This chapter proposes a wireless system for real-time transmission of undistorted Electrocardiogram (ECG) data for hospital applications. In this system, each patient is attached with a semi-passive Ultra-High Frequency / Ultra-Wideband (UHF/UWB) RFID tag with inkjet-printed paper-based ECG electrodes. Printed paper-based ECG electrodes are utilized to improve patient comfort. UWB radio of which the data rate is much higher than ECG bandwidth (BW), transmits ECG data of multiple patients to UHF/UWB RFID reader and subsequently to remote monitor in real time. A corresponding communication protocol which interleaves ADC sampling and burst-mode UWB transmission of each tag is proposed based on a modified Frame-slotted ALOHA protocol. The optimal system throughput is analyzed to be 400 patients/second at 1.5 KHz ECG sampling rate and 10 Mbps UWB pulse rate. The tag in this system consists of an UHF RFID receiver, an UWB transmitter, an ECG analog front-end, a multi-input ADC, and the base-band circuitry. To verify the system, the tag is implemented in two silicon dies of 180 nm CMOS process and 6 mm² silicon size. Experimental results demonstrate that the tag can transmit the ECG signals buffered during transmission intervals in one short UWB transmission burst, and the printed electrodes conduct ECG waveform comparable to the commercial electrodes.

4.1 State-of-the-art Wireless ECG Monitoring Solutions

The state-of-the-art wireless ECG monitoring solutions can be divided into three categories as illustrated in Figure 4.1. In the first category, each user carries a set of ECG tag and personal digital assistants (PDA) such as smart phone. ECG tag stores sampled ECG data in large-sized tag memory and transmits them to PDA by

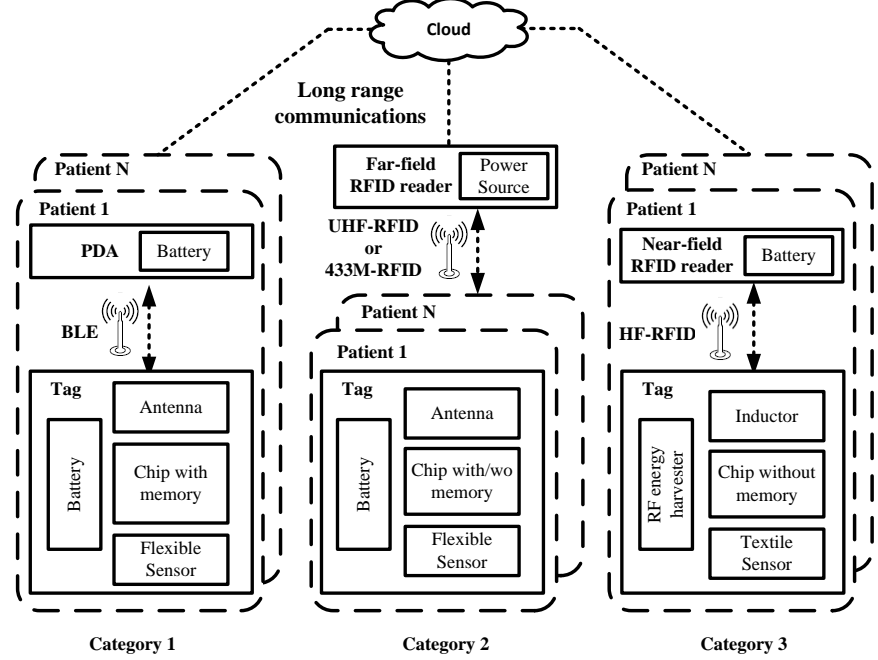


Figure 4.1: State-of-the-art solutions for wireless ECG monitoring system.

short range communication technologies such as BLE. Subsequent communication from the large numbers of PDAs to Internet is implemented by long range mobile phone communication technologies such as LTE [75]. In the second category, each user carries a wireless ECG tag only. A gateway or reader communicates with multiple ECG tags by UHF RFID or 433MHz RFID radio technology. Subsequent communications from the large numbers of readers to Internet is also carried out by long range communication technologies [76, 77]. The third category differs from the second one in that each user wears a set of one HF RFID reader and multiple ECG tags implemented on wearable materials such as Planar-Fashionable Circuit Board (P-FCB), a planar printed circuit technology on fabric. The reader provides both power and communication to multiple ECG tags [78].

The state-of-the-art solutions share similarity to sacrifice data completeness and monitoring accuracy for tag simplification considering patient comfort. In the first category, due to the high power consumption of mobile phone communication technologies, it is not activated unless a set of simplified predefined abnormal conditions are detected [75]. In the second category, owing to the limited data rate UHF RFID (below 640 Kbps), the tag either transmits ECG data at lower rate (sub-1Ksps) than the required ECG sampling rate, or requires large size of memory to buffer the sampled data and yields long communication latency [76]. Although data rate of

433MHz RFID can reach up to 1 Mbps [77], the power consumption of transmitter which consists of the conventional integer-N phase-locked loop (PLL) and the fully integrated power amplifier (PA) is significantly increased above 600 μ W [77]. In the third category, the reader worn on patient body is supplied by battery with large capacity; and the sensors harvest energy by strong inductive coupling of HF RFID link [78]. Both the battery and the strong inductive coupling can cause potential danger to hospital patients. Hence, they are not entirely suitable for hospital applications demanding both patient comfort and real-time monitoring.

4.2 Tag Architecture and Communication Process

This section describes the tag circuit block diagram and the communication process for real-time ECG signal transmission.

4.2.1 Tag Architecture

Figure 4.2 illustrates the tag architecture. To realize real-time transmission of ECG signals in multi-tag accessing scenarios, UWB transmission replaces UHF RFID backscattering for tag transmission because it offers high data rate transmission and still low power consumption as discussed in previous chapters.

Though UWB transmission can be activated in burst mode and supplied by RF energy scavenged by duty-cycling PMU as discussed in Chapter 3, ADC sampling of the ECG signals must be activated continuously and has to be supplied by battery energy. In view of this, battery is utilized to supply the tag energy.

Inkjet-printed electrodes as demonstrated in Figure 4.3 are integrated in this work. The ECG signals propagate from inside the human body to the skin in the form of ionic currents [79]. The electrode transforms the ionic currents flowing in the body into the electronic currents. Compared to silver/silver chloride electrode for common clinical applications, flexible dry electrodes are spared from irritation possibility to gel material and signal degradation due to gel dehydration. The state-of-the-art researches can be categorized into electrodes based on textile [80–83], electrodes based on a planar metal [84, 85], spiked electrodes [79, 86], and inkjet-printed electrodes on paper or polymer substrates [87]. Among these technologies, inkjet-printed electrodes are used in this work because [88]: 1) it shows the performances comparable to commercial wet electrodes for clinical applications; 2) it is flexible and lightweight; 3) its additive manufacturing characteristic facilitates the customization of electrode pattern. The inkjet-printed electrodes integrated are fabricated by direct printing of NPS-JL (nano-particle silver inkjetable low temperature ink from Harima Chemicals) with a 10 pL print-head on commercial polyimide (PI) foil (Kapton 500HN, DuPont) substrate [87]. The substrate has advantages of smoother surface, less shrinking, and more stable chemical and moisture conductance. They are sintered at 145 $^{\circ}$ C for 1 hour [87]. More detailed introduction of fabricating process and performance can be found in [89].

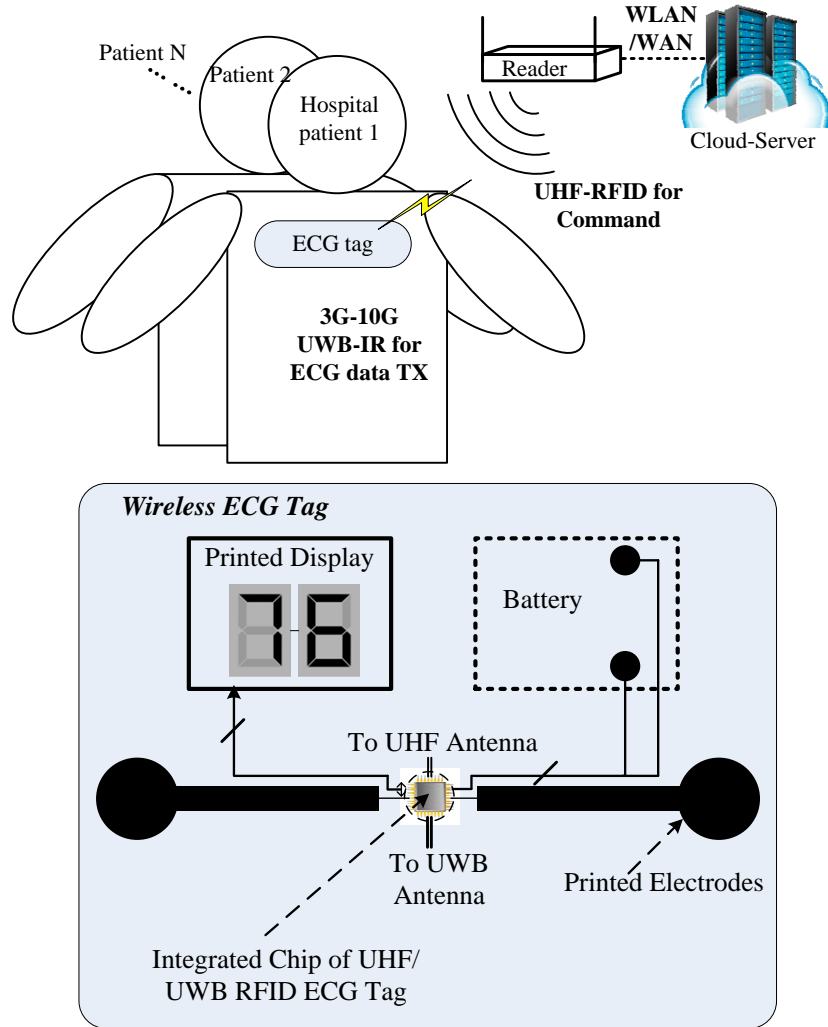


Figure 4.2: System Architecture of the UHF/UWB RFID ECG tag. *Adapted from Paper III.*

While ECG signals of multiple patients can be monitored remotely and simultaneously, it is also necessary to demonstrate basic information and emergent alert directly at every patient side. Tag integrated with display offers a simple user-interface compared to the media such as hand-held reader. EC display introduced in Chapter 2 and 3 shows features of low average power, low driving voltage and substrate flexibility; it also offers a response time less than 1 second given enough

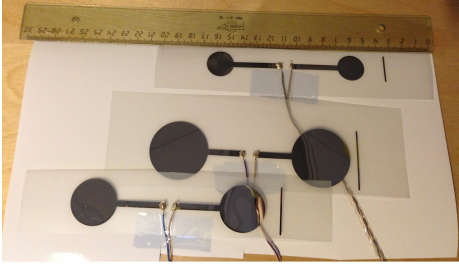


Figure 4.3: Inkjet-printed ECG electrodes. *Adapted from Paper III.*

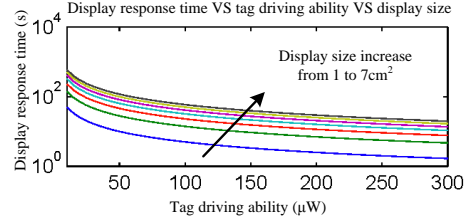


Figure 4.4: EC display switching time VS passive UHF RFID tag power for different display sizes. *Adapted from Paper VII.*

switching power according to table EPD in Chapter 2. Therefore, EC display is also integrated in the proposed ECG tag.

In medical applications, display must change at fast speed to show time-critical information. In this case, high instantaneous driving current is demanded. This current is in proportion to display area, and the instantaneous amount during display switching can reach several milli-amperes [90]. The relationship of display response time of different display sizes versus the driving ability of passive UHF RFID tag is illustrated in Figure 4.4. The required display driving currents surpass the driving ability of the passive display tag in Chapter 3 as well as the state-of-the-art passive UHF RFID tags [46,47,91]. As results, battery is demanded for the wireless ECG tag from the aspect of display driving as well.

As a summary, a semi-passive UHF/UWB RFID tag integrated with inkjet-printed ECG electrodes and EC display is proposed.

4.2.2 Communication Process for Real-Time ECG Transmission

Figure 4.5 illustrates the UHF/UWB RFID communication process for real-time transmission of multiple ECG tags. In general, ECG sampling and UWB transmission are interleaved for each tag based on the improved frame-slotted-ALOHA protocol [60].

ECG data are sampled and buffered during transmission intervals of each tag. The buffered data are transmitted in the next transmission window. To reduce the complexity of tag data storage, ECG sampling is temporarily disabled during UWB transmission. Since UWB transmission rate is much higher than ECG sampling rate, UWB transmission window is much shorter than ECG sampling window of each tag, and thus the missing percentage of ECG data is very low. For an example of 3.75 ms UWB transmission window, missing percentage for ECG data at 1.5 Ksps sampling rate is 5.625%.

UWB transmission window is designed no shorter than reader command window to decrease transmission gap and increase communication efficiency. In the opti-

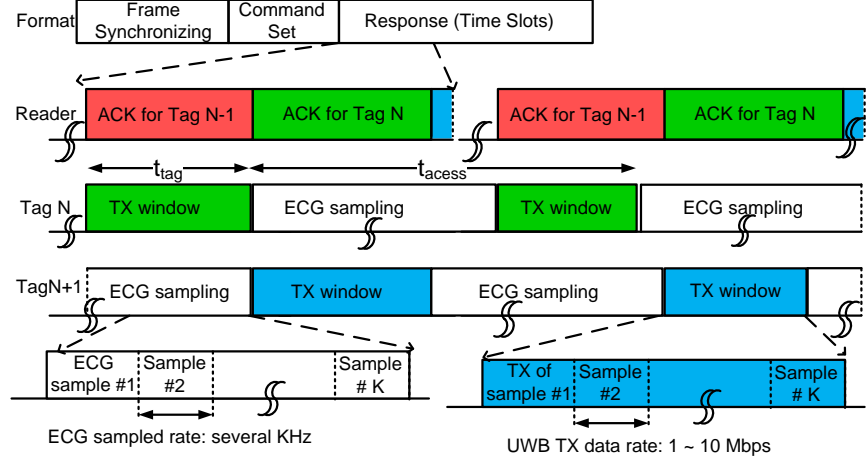


Figure 4.5: UHF/UWB RFID communication process for real-time ECG transmission. Adapted from Paper III.

mized case, there is no time gap or no idle slot between consecutive transmission windows of multiple tags. Therefore, the maximum number of accessed tags per second is shown in eqs. (4.1) to (4.5), of which the related parameters are shown in table 4.1. For ECG signals with 1.5 K sampling rate and 16-bit UWB data per sample, it offers approximate 400 tags/s accessing capability at 10 Mbps UWB-IR transmission rate and 0 dB processing gain. However, in real case, tag selects transmission slots in each frame randomly; moreover idle slots and tag collision cannot be eliminated. Thus, system accessing ability is lower than the value and is dependent on the trade-off of frame size and collision probability in proportional to N_{opt} [60].

$$N_{opt} = 1/(t_{tag}) \quad (4.1)$$

$$K = \frac{t_{access}}{t_{ECG}} \quad (4.2)$$

$$avg(t_{access}) = (N_{opt} - 1) \cdot t_{tag} \quad (4.3)$$

$$t_{tag} = K \cdot N_b \cdot PG \cdot t_{tx} \quad (4.4)$$

$$N_{opt} \approx \frac{t_{ECG}}{N_b \cdot PG \cdot t_{tx}} \quad (4.5)$$

Because UWB transmission is aggressively duty-cycling in the communication process, average power consumption of UWB transmission is much lower than active power as shown in eqs. (4.6) and (4.7) where P_{active} is the power consumption of UWB transmission and P_{avg} is the averaged power consumption of UWB trans-

Table 4.1: Parameters of UHF/UWB RFID communication process for real-time ECG transmission.

N_{opt}	Optimized number of accessed ECG tags per second
K	ECG samples per transmission window
t_{tag}	tag transmission window (length)
t_{access}	tag transmission intervals or access period
t_{ECG}	ECG sampling period
t_{tx}	UWB transmission pulse period
N_b	UWB transmission bits per sample
PG	UWB transmission processing gain (PG), i.e. pulse number per bit

mission in the proposed communication process [61], increasing battery life of the semi-passive tag.

$$P_{active} = E_{pulse}/t_{tx} \quad (4.6)$$

$$P_{avg} \approx \frac{P_{active}}{N_{opt}} \quad (4.7)$$

4.3 Circuit Implementation

Figure 4.6 illustrates the circuit diagram for the semi-passive UHF/UWB RFID tag with inkjet-printed ECG electrodes and EC display. The circuit blocks are implemented in two silicon dies in UMC 180-nm CMOS technology. The analog frontend (AFE) which amplifies and filters ECG signals from inkjet-printed electrodes is implemented in a separate die. Besides the AFE, the circuit is composed of UWB-IR transmitter, UHF RFID receiver, battery management unit (BMU), successive-approximation-register ADC (SAR ADC), baseband (BB) circuitry, and feedback display driver for EC display.

Amplitude of ECG signals varies according to the diameter and pair distance of the printed electrodes [89]. Therefore, the AFE is programmable in gain and bandwidth. It is composed of a differential instrument amplifier with high input impedance and two single-end amplifiers with programmable capacitor arrays for gain and bandwidth tuning. The AFE outputs up to 49 dB gain from 0.35 Hz to 1.5 KHz bandwidth with 2.76 μ W power consumption [92, 93].

Battery enables continuous ADC sampling as well as increases tag communication distance. Recent progress in flexible battery helps to keep tag flexibility. However, extra cost for maintaining the vast numbers of tag batteries is considerable. Therefore, a battery management unit is designed to include the following

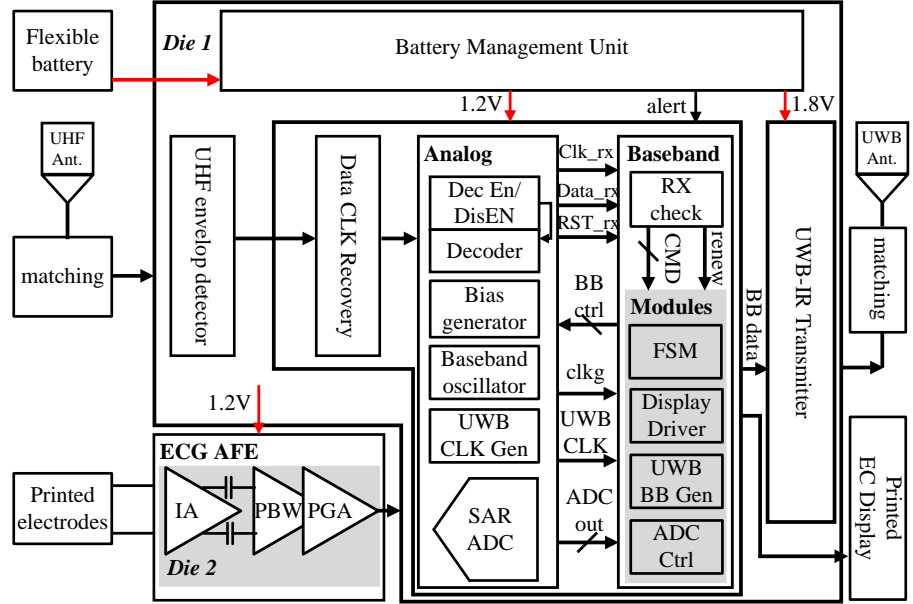


Figure 4.6: Circuit block diagram for the semi-passive UHF/UWB RFID tag with ECG sensing and EC displaying. *Adapted from Paper III.*

functions: 1) regulates battery voltage to generate the two supply voltages for tag (1.8 V for the UWB transmitter and the EC display driver whereas 1.2 V for other circuit blocks), 2) monitors the battery voltage and triggers an alert signal when the voltage drops below a pre-defined threshold value. Battery alert circuit can be implemented by the same circuit structure of the 1.8 V voltage sensor of the passive display tag in Chapter 3. The only modification is that the output of the alert circuit is parameterized to toggle from high to low when the battery voltage drops below 2.0 V while the 1.8 V voltage sensor toggles when the battery voltage further drops below 1.8 V. The UWB transmitter is enabled by the alert signal to transmit the information. Printed batteries with voltage above 2.8 V can be used in this work [94,95].

The operation flow for the out-of-battery alert, the display driving, and the interleaved ADC sampling and the UWB transmission is illustrated in Figure 4.7. According to the communication process in the previous section, UWB transmission and ADC sampling are both controlled by the reader. A renew signal marks the reception of a new reader command and triggers the assignment of tag registers. ADC enabling registers (ADC_en) trigger the tag to transition from idle state to ADC sampling state. UWB enabling registers (UWB_en), together with pseudo number counter (PN_count) [96], trigger the tag to transition from ADC sampling

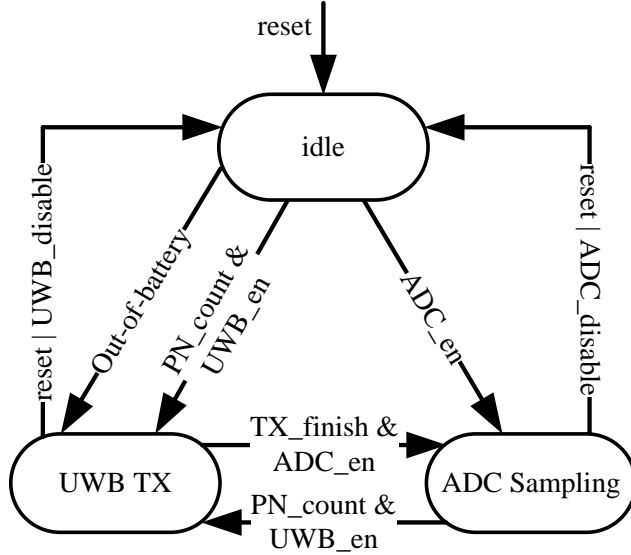


Figure 4.7: State transition of the UHF/UWB RFID ECG tag. *Adapted from Paper III.*

state to UWB transmission state for data transmission in random slots. When data buffered during transmission intervals are all read out and successfully received, the reader acknowledges the tag and disables UWB transmission. The tag is then re-transitioned to ADC sampling state. If out-of-battery alert is generated by the BMU, UWB transmission is activated regardless of the current states by a level-sensitive signal “UWB_Trigh”. Display driving is an isolated state relative to UWB transmission and ADC sampling. It is enabled by display enabling registers and disabled by both the configure registers and the out-of-battery alert.

4.3.1 Interleaved UWB Transmission and ADC Sampling

The circuit block diagram for real-time UWB transmission of ECG samples is illustrated in Figure 4.8. AFE output of the ECG signals is sampled and converted to 8-bit digital data by SAR ADC at ADC clock rate. Data are continuously buffered until UWB transmission is activated. When UWB transmission is activated according to the operation flow in Figure 4.8, ID and ADC data are read out in serial by rising edge of UWB transmission clock (UWB_CLK), and each bit are repeated by processing gain (PG) times (the number of pulses per bit). The rising edge of the output data triggers the UWB-IR transmitter. Transmitter NORs the rising edge and its delayed inverted result, and filters the output to generate the pulses [68]. Two clock domains are used. ADC clock is divided from the global clock and the di-

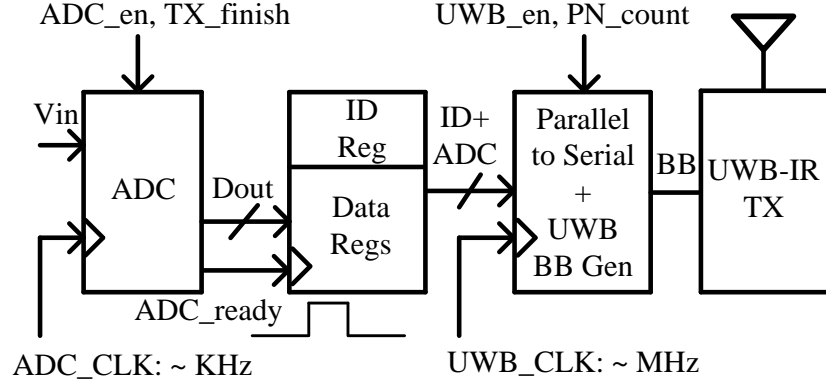


Figure 4.8: Circuit block diagram of the UWB transmitter and ADC for real-time ECG data transmission. *Adapted from Paper III.*

vision ratio is received from the reader for different applications. It is further gated by ADC enable signal to reduce power consumption. UWB transmission clock are generated by down-scaling UHF carrier wave (CW) with harmonic injection locked divider (HILD) first [68] and then with a series of digital dividers according to the reader-commanded data rate [62].

4.3.2 Feedback-Comparator Display Driver

As introduced in Chapter 2, EC display is bi-stable and shows long retention time. For applications where display contrast ratio is not a fatal problem, the long retention time can be used to reduce the average tag power consumption and thus increase the battery life, since $P_{avgdisp} = \frac{E_{sw}}{t_{sw} + t_{ret}}$. t_{sw} is display switching time per cm^2 and t_{ret} is the retention time, $P_{avgdisp}$ is average power consumption of display switching and E_{sw} is energy consumption of display switching.

One intuitive solution to make use of the long t_{ret} is to pre-calculate the retention time and disable display driver during this period. However, as demonstrated in Chapter 3 Figure 3.6, due to material aging, retention time varies from time to time. Moreover, it is inefficient from power aspect to calculate such long retention periods by the global clock which operates at much shorter periods. As an alternative solution, since the state change of PEDOT:PSS is energy-sensitive, and the energy can be represented by the value of display floating voltage by $E = C \cdot V^2$ considering its capacitive feature, the discharging voltage at which EC display returns to the pristine transparent semi-oxidized state can be utilized as the threshold voltage that alerts the re-activation of display driver. Compared to passive display tag which is both power and energy limited, semi-passive display tag is only energy-limited due to battery integration. Therefore, simultaneous power consumption can be high and conventional passive-matrix addressing scheme instead of the single-pixel

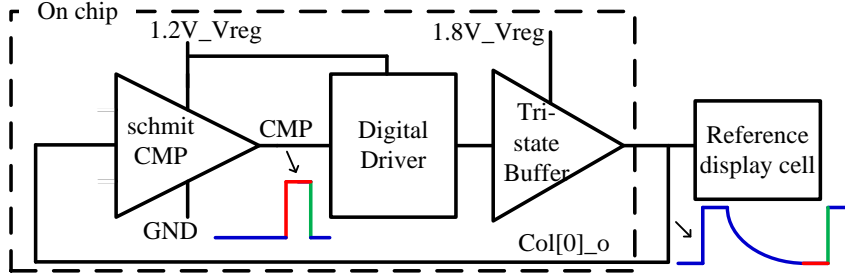


Figure 4.9: Circuit block diagram of the feedback display driver. *Adapted from Paper II.*

addressing scheme discussed in Chapter 3 can be used in the semi-passive display tag. (Same with the case in Chapter 3, two segment display samples are connected in a way that their columns are connected together and the rows are connected separately so as to emulate the structure of passive-matrix display.)

As a result, as illustrated in Figure 4.9, display driver is composed of a feedback comparator and the conventional matrix-addressing digital display driver. The feedback comparator monitors the column voltage of a reference display pixel ($\text{Col}[0]_o$) of which the counter-electrode is connected to ground and the electrode is always written by value “1” when the display is enabled. The comparator disables the display driver after the driver works for a pre-defined programmable set of switching time, and re-enables it when the floating voltage of the reference pixel drops below the threshold voltage. The feedback comparator is implemented by a Schmitt trigger circuit. Two different supply voltages are used to save power consumption. The core circuit is supplied by 1.2 V ($1.2V_V_{\text{reg}}$) and the display tri-state buffer is supplied by 1.8 V ($1.8V_V_{\text{reg}}$). As for the passive tag in Chapter 3, duty-cycling energy accumulation and single-pixel addressing are designed to fit the display driving power into the budget of passive RFID tags. Hence, the refresh rate is already very low, and subsequently the display switching period is already very long. So, in this case, the long retention time is already made used of and the feedback display driving is not needed.

Based on the feedback operation, the entire display driver operates in three different states: refresh, clear and wait. In refresh state, the driver addresses the display row by row, of which the addressed row is connected to ground while the non-addressed rows are connected to high-Z. In clear state, it counter-connects display rows and columns - connects all the rows with 1.8 V supply and columns with ground - to remove the remained image due to the bi-stability and the long retention time of EC display. In wait state, the driver sets display rows and columns to high-Z connection and disables clock circuitry for display driver (the divider circuit to generate clock period for display switching period) until re-enabled by the output from feedback comparator. A majority of power is saved by operating

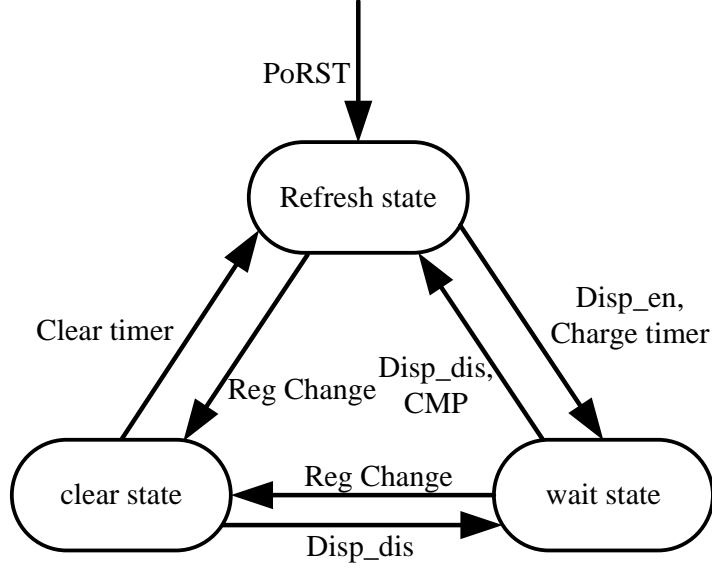


Figure 4.10: State transition of the feedback display driver. *Adapted from Paper II.*

the display driver and clock circuit in wait state.

The transition among the three states is shown in Figure 4.10. When the system is powered on, the power on reset (PoRST) triggers the driver into refresh state to show the default display data. It keeps in this state before a whole packet of reader command is completely received. If the newly received display data differs from that stored in the registers, the baseband circuit generates a signal (“Reg Change”) and triggers it to transit into clear state. The time for clearing the display is similar to the switching time. Once the clear time is achieved, the display goes into refresh state. Similarly, it in turn goes into wait state when the switching time is reached. When it is stayed in wait state, the output from the feedback comparator triggers it to transit from wait state to refresh state; the ‘Reg Change’ signal triggers it to clear state; the display enable signal (“Disp_en”) triggers it to refresh state. When disabled by “Disp_dis”, the display goes into wait state.

As a summary, the feedback display driver is designed to save tag power consumption of clock circuitry and to be robust to display performance variations.

4.4 Experimental Results

Figure 4.11 illustrates the die photos of the UHF/UWB RFID tag with ECG-sensing implemented in UMC 180 nm CMOS technology process. Die of the UHF/UWB RFID tag is shown in Figure 4.11 (a) and AFE for ECG is shown in Figure 4.11 (b).

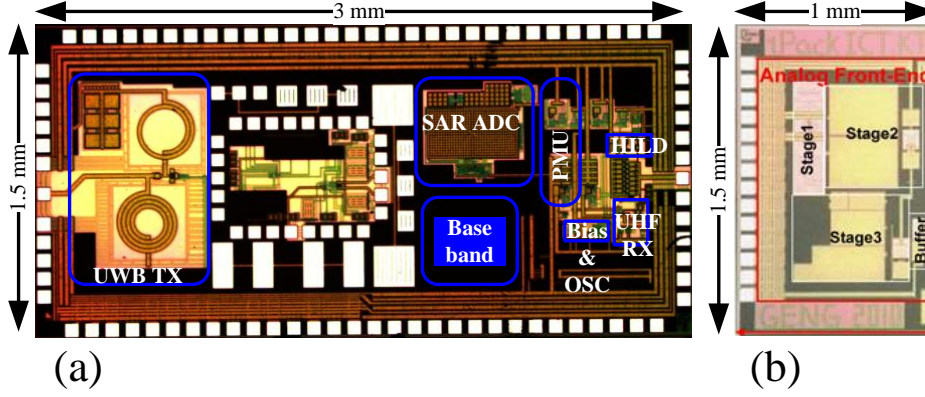


Figure 4.11: Die photos (a) of the semi-passive UHF/UWB RFID circuit and (b) of the AFE circuit. *Adapted from Paper III.*

Inductors of UWB transmitter, capacitors of SAR ADC and the tunable capacitor array of AFE are the components that consume most of the die area. In current design, the UHF/UWB RFID die is tested separately by inputting ADC block with emulated amplified cardiac signals from signal generator (Agilent 33250A). In future design, both dies will be integrated in a single die and the output of signal generator will be replaced by that of AFE.

4.4.1 Real-time UWB-IR Transmission

Figure 4.12 (a) (b) demonstrate UWB transmission interleaved with ECG samplings of one tag. Figure 4.12 (a) is the result of UWB baseband (BB) data and Figure 4.12 (b) is the result of UWB transmission pulse. UWB transmission takes place in the response phase according to the communication process illustrated in Figure 4.5. For implementation simplicity, reader ACK command re-uses reader write command format in current system. Corresponding to the reader command window length which is 2.3 ms at 40 - 80 kbps UHF RFID data rate, 3.75 ms of tag transmission window is selected as an example. For an assumed multi-accessing scenario of 40 tags at 1 Mbps tag transmission rate, the transmission interval is thus 146.25 ms and is left for the UWB transmission of the other 39 ECG tags in ideal case. ECG signals sampled by ADC at 1.5 Ksps rate are buffered during the transmission intervals, and the number of buffered samples is around 219. They are transmitted together with tag ID in burst mode at 1 Mbps data rate in the next transmission window.

Figure 4.13 shows the zoomed-in result of UWB transmission for one ECG sample. It consists of eight-bit tag ID and eight-bit ADC data. UWB signals are transmitted at 1 Mbps pulse rate (Figure 4.13 (a)) with on-off-keying (OOK)

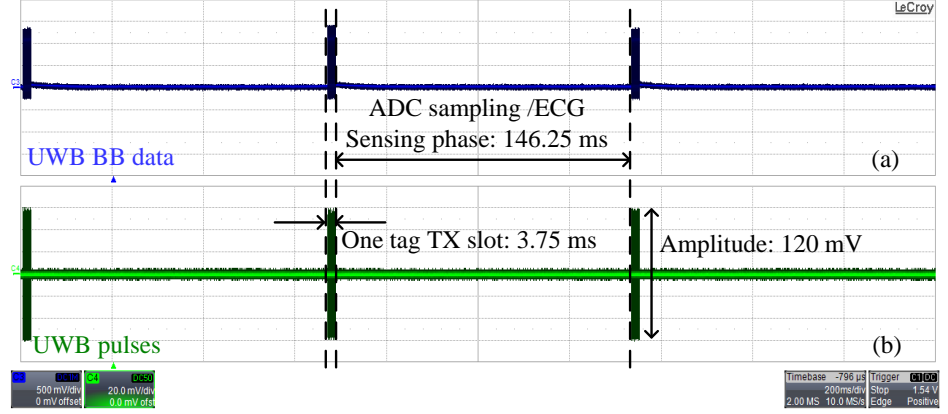


Figure 4.12: UWB transmission interleaving with ADC sampling. *Adapted from Paper III.*

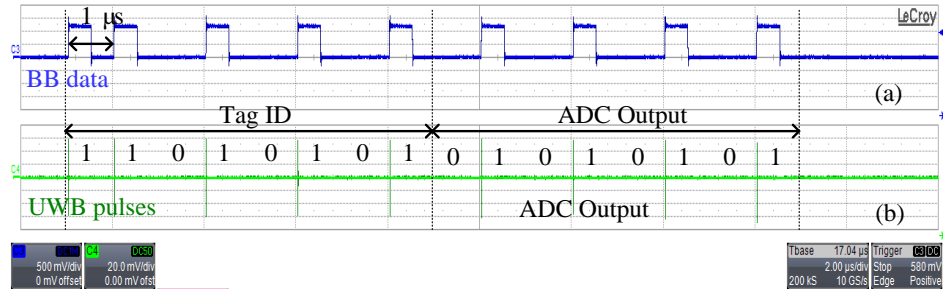


Figure 4.13: UWB transmission for one ADC data of one tag at 1 Mbps pulse rate. *Adapted from Paper III.*

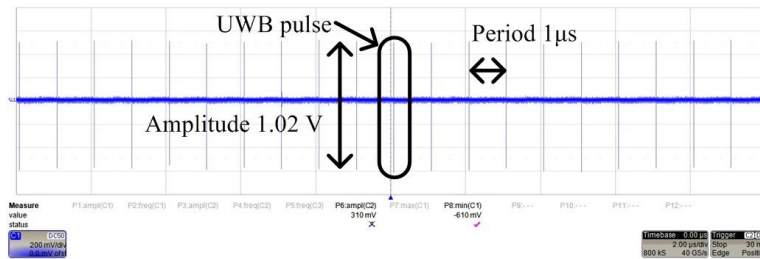


Figure 4.14: UWB pulses at 1 Mbps pulse rate. *Adapted from Paper III.*

modulation (Figure 4.13 (b)). As described in Section 3.3, UWB pulse is generated at the rising edge of UWB baseband data.

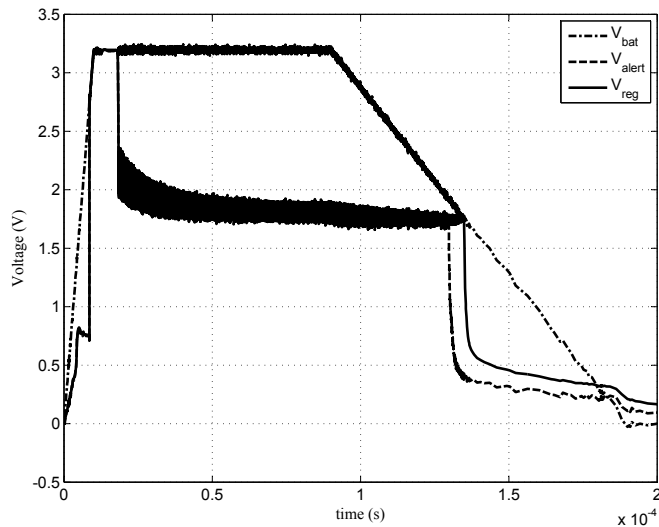


Figure 4.15: Out-of-battery alert when battery voltage drops below 2.0 V *Adapted from Paper VII.*

Figure 4.14 demonstrates the consecutive UWB pulse at 1 Mbps rate with 1.02 V amplitude and 620 ps duration when enabled by the out-of-battery alert signal. Pulse amplitude and duration can be tuned by the amplitude control in the UWB transmitter [68].

4.4.2 Out-of-Battery Alert

The waveforms of battery voltage (V_{bat}), alert voltage (V_{alert}) and 1.8 V regulator voltage (V_{reg}) are demonstrated in Figure 4.15. When the battery voltage drops below 1.8 V, the voltage regulator stops working. Prior to that, when the battery voltage drops below 2.0 V, the alert voltage toggles from high to low first, and enables UWB transmitter when 1.8 V voltage regulator is still high.

4.4.3 Feedback Display Driver

The experiment utilizes two seven-segment display samples. To emulate the matrix structure of 7 columns and 2 rows, their columns of two samples are connected together and the grounds are connected with row [0] and row [1] respectively.

If the received UHF command is checked to be effective, and the received display data is different from the value previously stored in the display data registers, EC display begins with clearing the old image by connecting rows to 1.8 V supply

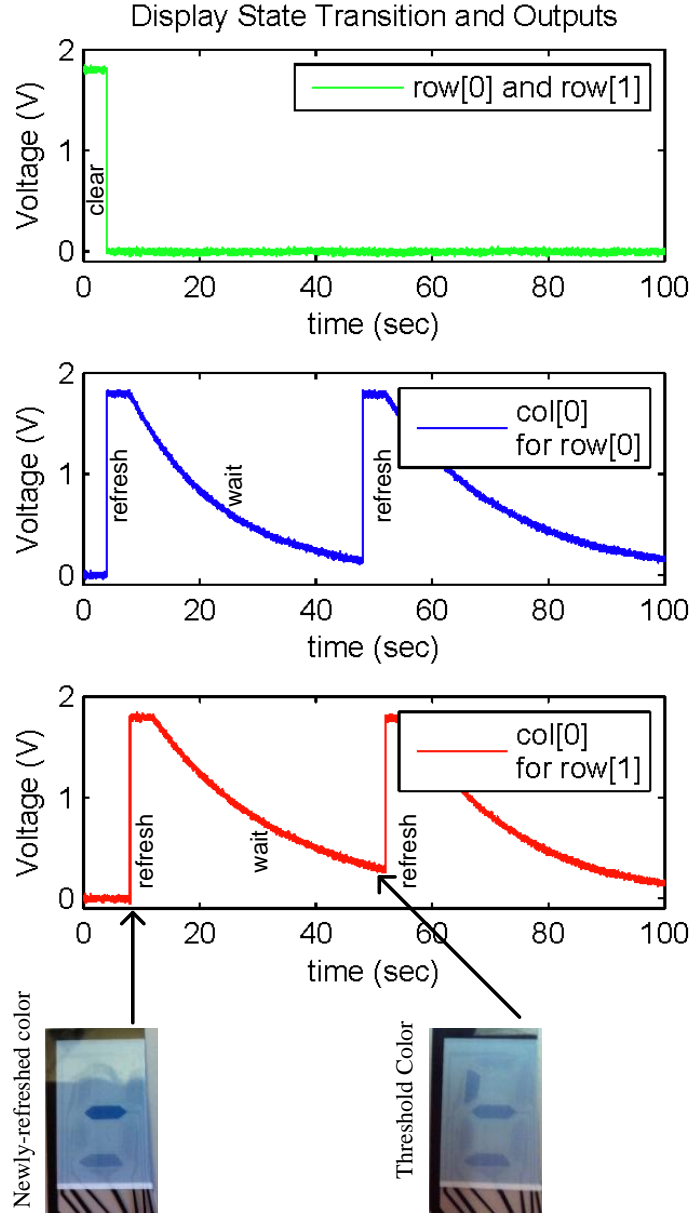


Figure 4.16: Display column and row outputs in the time domain and the corresponding states and images demonstration *Adapted from Paper VII.*

and columns to ground, and follows by addressing the columns row by row, as demonstrated in Figure 4.16. After reaching the switching time (four seconds as an example case), the driver stops driving the display, leaving the floated column voltage to discharge. Since the reference display is defined as the intersection cell of ground and column [0], the display is refreshed again when the voltage of column [0] drops below V_{th} , as demonstrated in Figure 4.16. Figure 4.16 also demonstrates the photos when the EC display is newly-refreshed and when its remaining voltage drops to V_{th} . To shorten the T_{ret} and decrease the oscilloscope sampling points, an older display sample is tested in this demonstration. Tested by the source meter of Keithley-2440, the current consumption of the display driver is around $70 \mu A$ in the refresh state and less than $1.2 \mu A$ in the wait state per EC display of 1 cm^2 . Thus the average power consumption of the EC display driver is reduced to about $1.1 \mu A$ for sustaining the image.

4.4.4 ECG by Inkjet-Printed Electrodes

Figure 4.17 shows the ECG signals captured by the inkjet-printed electrodes and is measured at AFE output. Although the electrodes have different sizes and pair distances, the effects on electrode impedance are compensated by the large input impedance and the variable gain bandwidth of AFE.

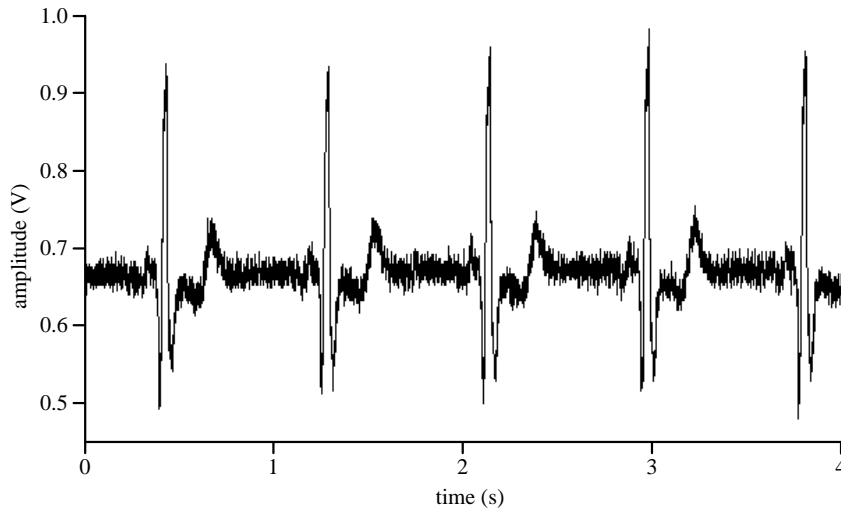


Figure 4.17: The ECG signal at AFE output by the inkjet-printed electrodes. Adapted from Paper III.

	This work		Tee, H./JSSC2010	Yoo, J./JSSC2010		Medtronic 2014
ASIC process	180 nm CMOS		180 nm CMOS	180 nm CMOS		-
Power	sensor interface	$\sim 71.4 \mu\text{W}$ @ 1.5 Ksps	12 μW	sensor interface	$\sim 49.7 \mu\text{W}$ @ 0.1-300 Hz	$\sim 1.3 \text{ mW}$
	transmitter	18 μW @ 1 Mbps		transmitter	670 - 690 μW	
TX radios	3.1 - 10.6 GHz UWB-IR		13.56 MHz RFID	433.92 MHz RFID		2.4 GHz BLE
data rate	1 - 10 Mbps		10 - 120 kbps	19.2 kbps - 1 Mbps		few Mbps
display	Yes		No	No		No
chip size	6 mm ² *		4.8 mm ²	5.29 mm ²		-
distance	10 meters **		several centimetres	5 meters		9 meters
patches/s	several hundreds		several tens	-		-

*Added size of two ASIC dies

** Results based on measured sensitivity.

Figure 4.18: Performance comparison of the UHF/UWB RFID ECG tag with related works.

4.4.5 Performance Comparison

Figure 4.18 summarizes the performance comparison of the proposed tag with the related works. It shows a better trade-off of transmission rate and power consumption compared to the others. It also has the display function implemented by bi-stable flexible EC display.

4.5 Summary

This paper proposes a UHF/UWB RFID tag with ECG sensing ability for low power and real-time patients remote monitoring in hospital applications. For the transmissions of undistorted ECG signals of multiple patients, high data rate UWB transmission and ECG sampling are interleaved based on an improved frame-slotted-ALOHA protocol. It suggests a maximum accessing capability of 400 tags/s at 10 Mbps UWB transmission data rate and 1.5 Ksps ADC sampling rate. The battery management unit is integrated to enable automatic monitoring of out of battery as well as generate the dual supply voltages for tag circuit. EC display is also integrated to offer a most direct interface for alert and basic information demonstration. The tag is implemented in two silicon dies manufactured in UMC 180nm CMOS technology process. Total die area is 6 mm². As a foundation for future wearable ECG-patch, both ECG electrodes and tag display are fabricated by printing techniques on flexible substrate. Experimental results show that UWB transmitter consumes 18 μW at 1 Mbps rate, corresponding to 18 pJ/pulse. The AFE output of the ECG signals conducted by the printed electrodes is comparable to that by commercial electrodes. Display driver controls EC display in a feedback scheme to lower power consumption and be more robust to material variations. Future works based on the current prototype are to integrate the AFE block in the same die with the circuit blocks of UHF/UWB RFID tag, and to replace the conventional antenna with flexible UHF and UWB antenna as introduced in [97, 98].

Chapter 5

Multi-Band SDR Reader for Interactive RFID System

Different IoT applications demand different RFID bands. For example, 433 MHz RFID shows less propagation loss for in-body and on-body communication in healthcare applications [99], while UHF RFID has the advantages of smaller antenna size and broader bandwidth and is more suitable for IoT applications such as smart warehouse and smart manufacturing. Similarly, UWB communication also have different bands for different protocols and one most popular band introduced alongside Wireless Personal Area Network (WPAN) is sub-1GHz band with 500 MHz bandwidth (249.6 to 749.6 MHz) [100]. As a result, a generic wireless reader that can work with multi-band, multi-rate and multi-standard communications is very attractive for IoT applications.

One possible solution is software-defined radio (SDR) architecture of which digital circuits replace analog and RF circuits as much as possible. With CMOS process scaling-down, digital circuit shows faster speed, less power consumption, and smaller size, making SDR a more and more feasible solution.

Under such circumstances, an all-digital polar transmitter and a moderate-to-high speed ADC for multi-band receiver is studied in this chapter.

5.1 State-of-the-art SDR Transceiver

This section reviews the architecture and characteristics of the state-of-the-art receiver and transmitter for SDR design.

5.1.1 Direct Conversion Transmitter

One most popular transmitter architecture is direct conversion transmitter as shown in Figure 5.1 [101]. Digital baseband signals are divided into (in-phase and quadrature component) I/Q paths, and are converted to analog signals by digital-to-analog

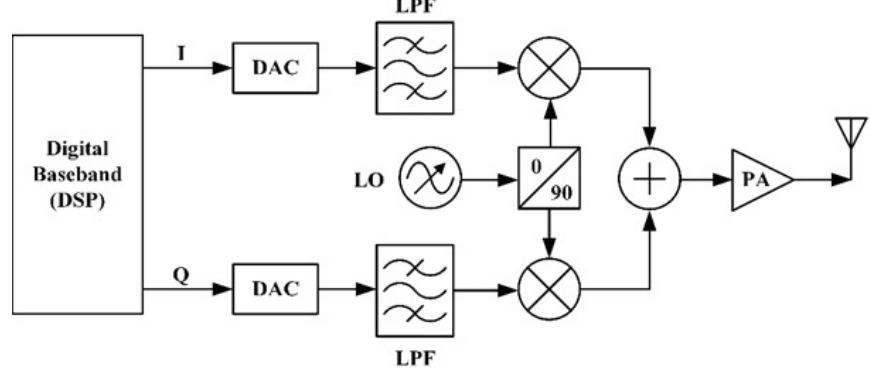


Figure 5.1: Architecture of direct conversion transmitter.

converter (DAC). The subsequent low pass filter (LPF) removes high frequency harmonics. Mixers up-converted the signals to RF frequency by local oscillator outputs with 0 degree and 90 degree phase shifts respectively. The two branches of outputs are added together and power amplified before fed into the antenna.

The I/Q baseband signals are presented in expression 5.1:

$$I(t) = R(t) \cos(2\pi f_{bb}t), Q(t) = R(t) \sin(2\pi f_{bb}t) \quad (5.1)$$

f_{bb} in expression 5.1 is the frequency of baseband signal, and hence the signals after up-conversion can be expressed as:

$$Y(t) = I(t) \cos(2\pi f_{LO}t) + Q(t) \sin(2\pi f_{LO}t) = R(t) \cos[2\pi(f_{LO} - f_{bb})t] \quad (5.2)$$

Judging from expression 5.2, the output of up-conversion only contains the frequency component of $f_{LO} - f_{bb}$ while the frequency component of $f_{LO} + f_{bb}$ is canceled out.

Despite its popularity, one most significant limit of direct conversion transmitter is analog intensive circuit implementation. First, intrinsic performances of analog circuits are sensitive to matching and PVT, resulting in inevitable I/Q mismatch in this architecture. Complicated compensation circuits are required to achieve specified performance [102]. Second, the reconfigurability of analog circuits are one largest design challenge for multi-band SDR transmitter.

5.1.2 Polar Transmitter

An alternative description to Cartesian coordinate is Polar coordinate and the I/Q signals can be expressed as:

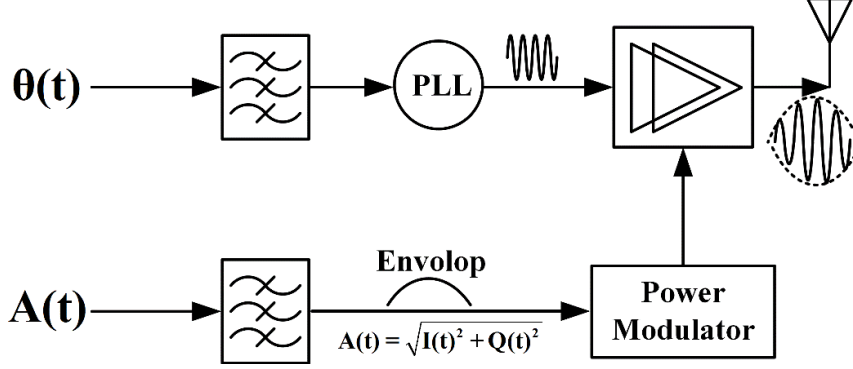


Figure 5.2: Architecture of conventional polar transmitter.

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \quad (5.3)$$

$$\theta(t) = \arctan\left(\frac{I(t)}{Q(t)}\right) = \arccos\left(\frac{Q(t)}{A(t)}\right) \quad (5.4)$$

Based on expression 5.5, the up-converted signals can be expressed as:

$$f(t) = I(t) \cos(\omega t) + Q(t) \sin(\omega t) = A(t) \cdot \cos[\omega t + \theta(t)] \quad (5.5)$$

Correspondingly, the architecture of conventional polar transmitter is illustrated in Figure 5.2 [103, 104]. RF power signal is generated in two steps: first the power modulator converts DC power supply into envelop power; secondly the envelop is combined with phase modulation that are the direct carrier wave output of phase-locked loop (PLL). It shows the following advantages. First, the power amplifier is always working in saturation mode and therefore can generate high efficiency. Second, the phase noise from PLL only has impact on the phase modulation path not the amplitude modulation path. Therefore, compared to direct conversion transmitter where the phase noise of PLL impacts both IQ branches, polar transmitter has lower requirement on PLL phase noise. The disadvantages are as follows. First, the matching of phase and amplitude modulation paths is important. Second, the signal conversion from Cartesian coordinate to Polar coordinate is nonlinear and subsequently results in bandwidth expansion. It can cause system design limits for modern communication transceivers which targets wider bandwidth. Third, efficiency of power modulator is impacted by Rayleigh distribution of envelop amplitude. Forth, the off-chip matching filter must be a trade-off between allowing expanded bandwidth of amplitude modulation and filtering out modulation switching noise nearby [105].

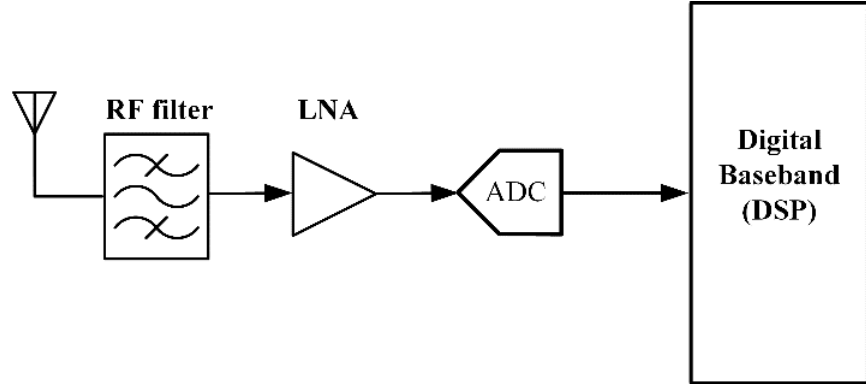


Figure 5.3: Architecture of direct RF sampling receiver.

5.1.3 Direct RF Sampling Receiver

Architecture of direct RF sampling receiver is illustrated in Figure 5.3 [101]. Instead down-converted to intermediate frequency (IF) in advance, the received RF signal is directed sampled after filtered by RF filter and amplified by low noise amplifier (LNA). Although it shows best flexibility for SDR design and has good potential as CMOS process scales down and transistor speed increases, it poses very high challenges on circuit design and is very power hungry. One most challenging and power inefficient block is ADC. ADC has to operate at at least twice of the RF frequency, which is usually at GHz scale for modern communications. Power consumption of such high-speed ADC with four to five effective number of bits (ENoB) is already at orders of magnitude of hundreds of μW to mW. Higher ENoB increases the power consumption significantly. Therefore, it is still more suitable to down-convert the RF signals and leads to the following two architectures.

5.1.4 Low IF Receiver

Architecture of low IF receiver is illustrated in Figure 5.4 [101]. This is basically a superheterodyne radio, but in this design the IF frequency is chosen to be so low that both the IF and baseband processing can be performed in the digital domain. The RF circuitry can be as simple as that of a zero-IF receiver which directly converts the RF signal to baseband, but it does not suffer from the DC offset problem and flicker noise in zero-IF receiver. The main problem with a low IF receiver is that the image frequency will now be very close to the desired sideband, making it hard to be filtered out [101]. Another problem for SDR applications is that the very limited bandwidth of IF receiver requires very wide tuning range of PLL, significantly increasing the design challenge of PLL and is thus not suitable for SDR.

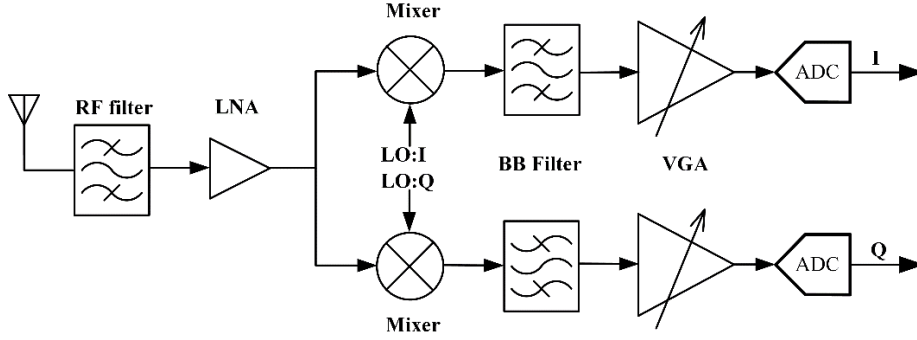


Figure 5.4: Architecture of low IF receiver.

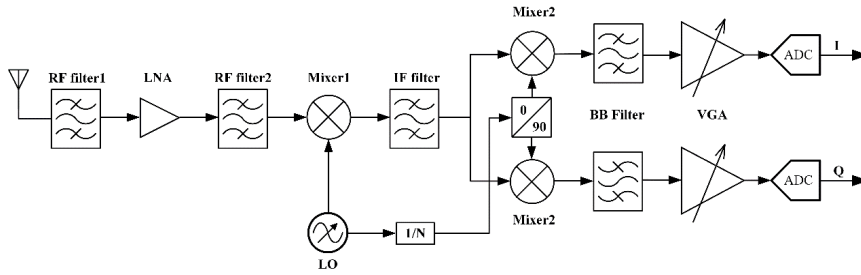


Figure 5.5: Architecture of sliding-IF receiver.

5.1.5 Sliding-IF Receiver

Architecture of sliding-IF receiver is illustrated in Figure 5.5. It differs to superheterodyne receiver by deriving different mixing frequencies by only one local oscillator (LO). The different frequencies are derived by dividing the one LO by some fixed number. As a result, the IF frequency is not fixed, but “walks” in step with a fraction of the frequency of the RF LO [101]. Compared to traditional superheterodyne receiver, it removes the need of the extra synthesizer and avoids the possibility of two synthesizer output frequencies mixing together to produce beat frequencies possibly in the baseband [101]. Compared to low IF receiver, it shows better image rejection performance. It is suitable for SDR applications, the flexibility in fraction selection of the LO frequency greatly expands the bandwidth coverage of the receiver and increases the flexibility of frequency planning of the receiver.

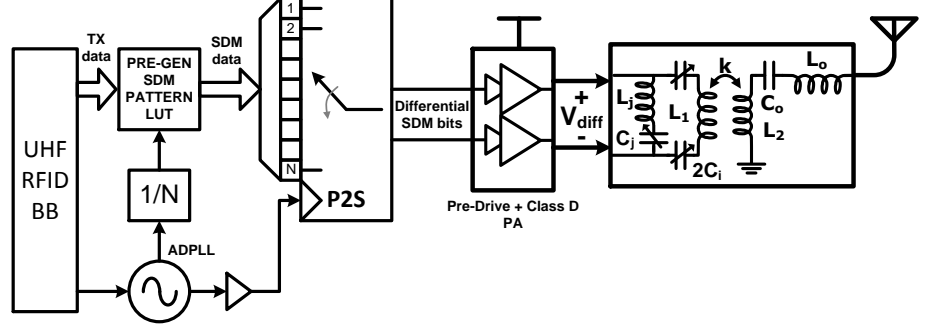


Figure 5.6: All-digital transmitter architecture.

5.2 All-Digital Polar Transmitter

This section introduces the architecture [106] and design of all-digital polar transmitter for multi-band RFID communications. Except the filter circuits, the transmitter can be implemented by digital IC tools.

5.2.1 Transmitter Architecture

The architecture of the all-digital transmitter is illustrated in Figure 5.6. Compared to traditional polar transmitter which includes analog power modulator and combines amplitude and phase signals in Class-E power amplifier, the all-digital polar transmitter modulates envelop information in digital domain. It reduces loss in power modulator and enables digital mixing of amplitude and phase information by high speed AND logic or PLL triggered digital flipflop (DFF), making it a suitable solution for multi-band SDR transceiver [106].

The analog envelop information is converted to digital representation of “SDM data” by low pass (LP) $\Sigma\Delta$ modulation (SDM). The principle of LPSDM is transferring amplitude into the density of digital pulses.

To reduce power consumption, the SDM patterns for envelop of defined communications are pre-generated (PRE-GEN) and stored in the memory. When transmission is started, the SDM data are generated by finding and calling out the corresponding SDM patterns in the PRE-GEN SDM pattern Lookup Table (LUT) block. Taking UHF RFID for example, the pre-generated SDM patterns for envelop include rising edge (R), falling edge (F), high level (H), and low level (L), as illustrated in Figure 5.7. The SDM data are then converted from parallel to serial (P2S) SDM bits at RF frequency. Because the P2S conversion is implemented by digital register, so the register is working at twice of the RF frequency to generate outputs at RF carrier frequency. The digital clock for P2S converter is the quantized result of all-digital PLL (ADPLL) output. The PRE-GEN SDM pattenr LUT block is triggered at N division of P2S clock frequency for continuous operation.

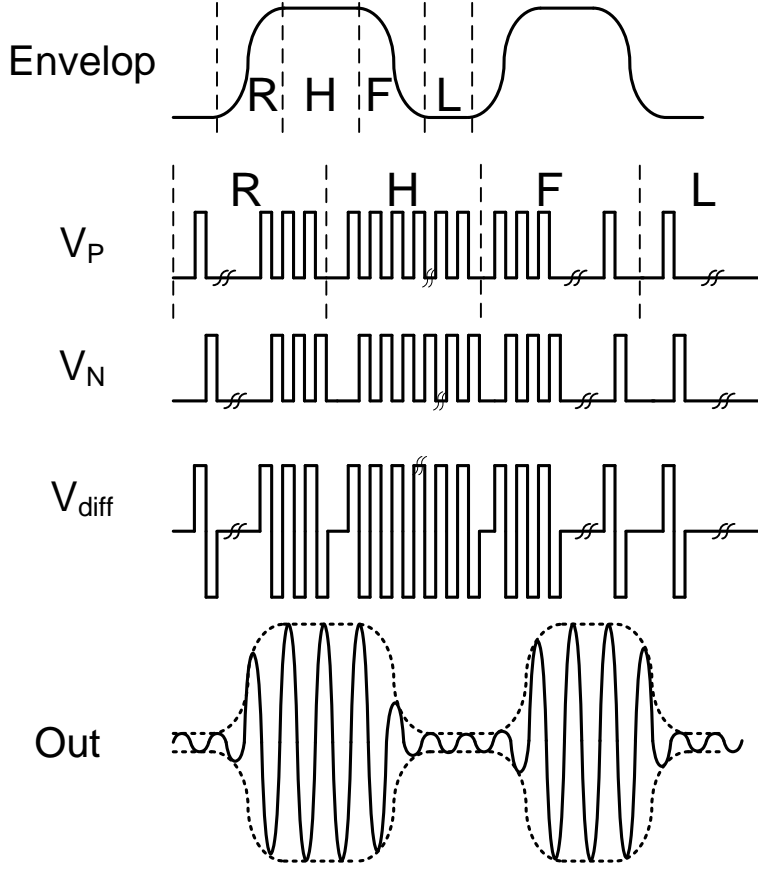


Figure 5.7: All-digital transmitter signals at time domain.

The differential outputs are generated by delaying one serial path of the SDM bits by one clock period of the P2S converter.

The differential streams of the SDM bits are amplified and shaped by the high speed digital pre-driver and the digital amplifier to generate “ V_{diff} ” in Figure 5.6. A class-D power amplifier (PA) referring to the design in [106] is utilized. Although class-E PA can generate higher efficiency, the prerequisite condition that switching transistor sustains a small voltage when current is flowing and carries small current when voltage is on [107] is not met in case of the LPSDM signals. A 3rd-order bandpass filter (BPF) suppresses the harmonic signals of V_{diff} in the frequency domain, generating the transmitted signal “Out” in Figure 5.6. The 3rd-order BPF is designed based on the 2nd-order filter in [106]. L_j and C_j as shown in Figure 5.6 are added to suppress the 3rd-order harmonics of the RF frequency. The filter is off-chip for higher Q value and better reconfigurability. Figure 5.7 illustrates the

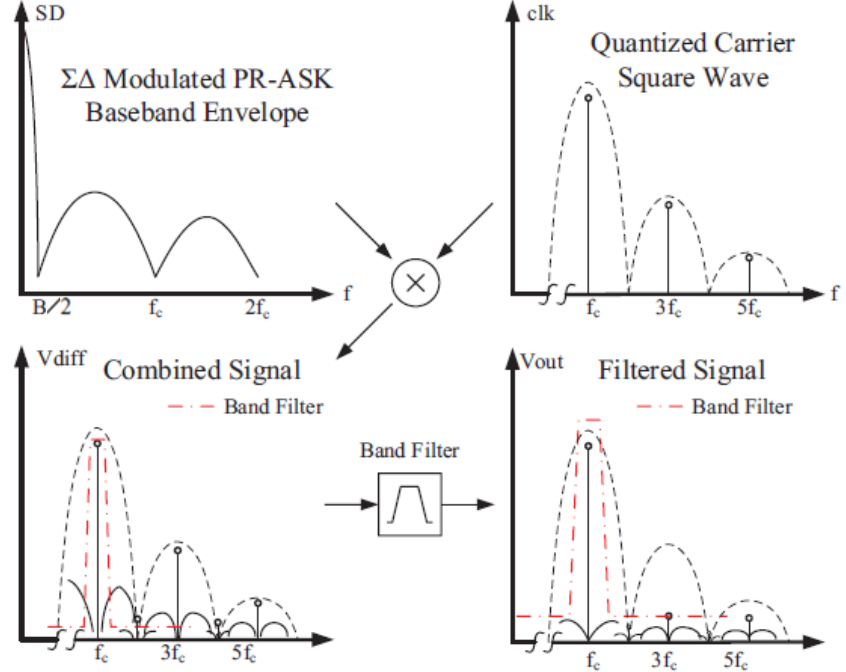


Figure 5.8: All-digital transmitter signals at frequency domain [106].

transient time domain behavior of the all-digital polar transmitter.

5.2.2 Transmitter Spectrum

Since the oversampling ratio (OSR) of SDM equals to $\frac{f_{RF}}{2 \times B}$ of which f_{RF} is RF frequency and B is bandwidth of the transmitted data, the OSR is very high and the quantization noise of the quantized ADPLL clock can be pushed far away from the RF frequency, relaxing the design specifications for the off-chip filter compared to traditional polar transmitter.

5.2.3 Transmitter Implementation and Simulation Results

All the digital blocks of the transmitter is described by VHSIC Hardware Description Language (VHDL) and implemented by digital IC design tools for UMC 65nm CMOS process. The operation flow and data flow are shown in Figure 5.9. High frequency serial register (HFSR) is the only digital circuit that operates at twice of the RF carrier frequency.

Figure 5.10 simulates the transmission spectrum of ASK signals at 960 MHz UHF RFID compared to the multi-tag and dense-tag spectrum masks.

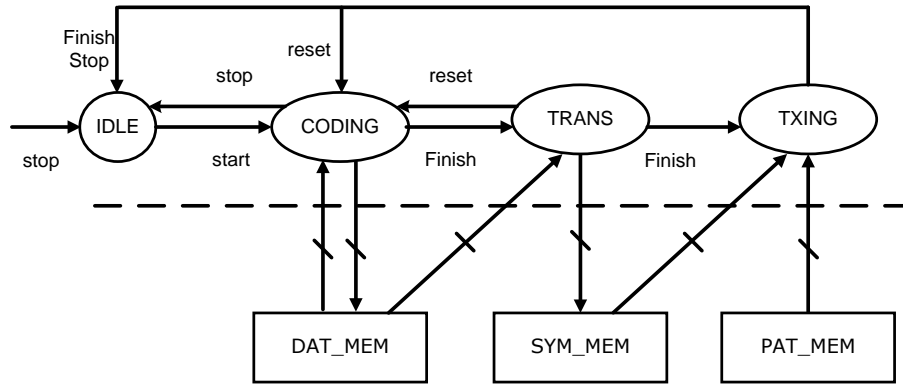


Figure 5.9: All-digital transmitter operation and data flow.

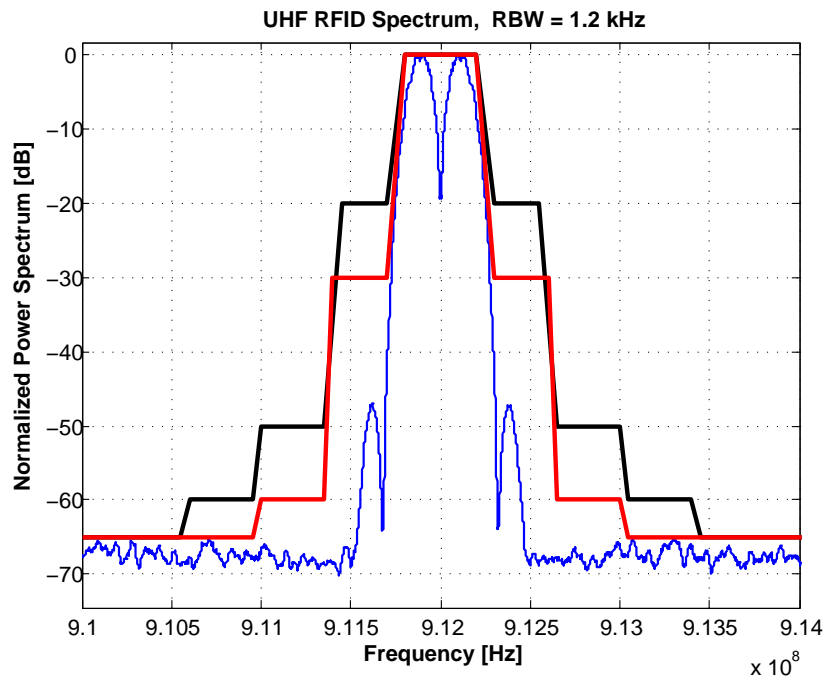


Figure 5.10: All-digital polar transmitter output spectrum and spectrum mask.

5.3 Flash ADC for Multi-Band Receiver

This section introduces the receiver architecture for multi-band RFID communications and the design of Flash-ADC for the receiver.

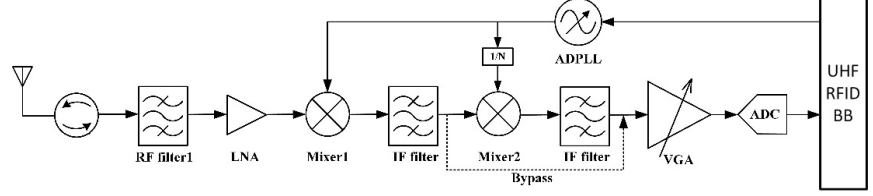


Figure 5.11: Receiver architecture for multi-band SDR.

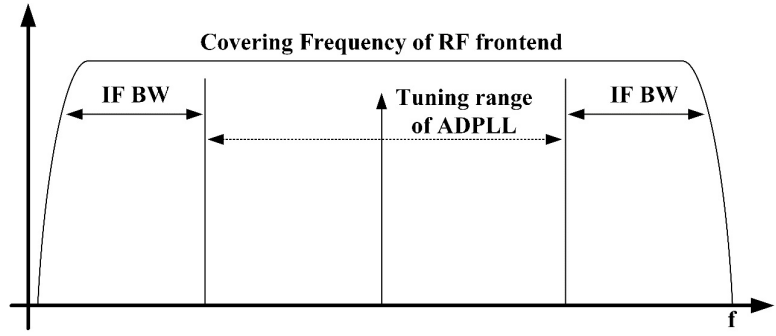


Figure 5.12: RF frequency cover range of the multi-band SDR receiver.

5.3.1 Receiver Architecture

The proposed receiver architecture is based on that of sliding-IF receiver and is shown in Figure 5.11. The ADC operates at high speed, offering very wide IF bandwidth. Combining with the tuning range of ADPLL the receiver can cover very wide range of received frequencies as well as achieve fine ADPLL tuning step. Figure 5.12 illustrates the idea. It enables simultaneous reception of multi-band signals.

5.3.2 ADC Architecture

ADC in the proposed receiver serves to transfer the amplified analog IF signals to digital signals for baseband data processing. The bandwidth of IF signal is from moderate to high according to the system design. Compared to $\Sigma\Delta$ ADC and SAR ADC, flash ADC can operate at higher sampling rate because they perform multi-bit conversion simultaneously. For N-bit ADC, 2^N-1 comparators are connected in parallel. Reference voltages of the comparators are spaced by $V_{FS}/2^N$ where V_{FS} is the full swing of the input signal. Digital outputs of the comparators are in thermal code style, and are translated by a thermo-to-binary coder to generate the final binary digital outputs. As a cost of the high sampling rate, the resolution of flash-ADC is highly limited by the chip size and the effective input

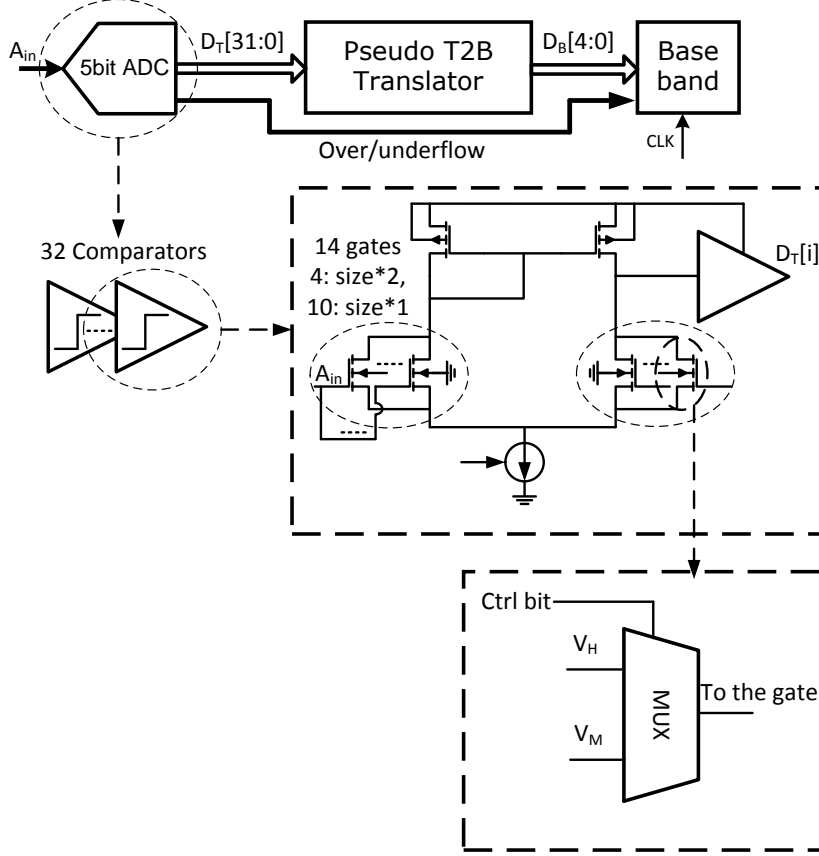


Figure 5.13: ADC architecture and circuit diagram.

capacitance as well as power consumption by the system specification. Referring to the $FoM = \frac{P}{2^{ENoB} \times f_s}$ of state-of-art solutions [108, 109], where FoM is the the figure of merit, P is the ADC power consumption, ENoB is the effective number of bits, and f_s is the sampling rate, a feasible resolution limit of basic flash-ADC is 5-bit to keep power consumption lower than several mW at Gsps sampling rate. To improve the resolution within the limits, subranging or folding architecture can be added to flash ADC. It can realize 2N-bit resolution with N-bit flash-ADC. The N-MSB bits are obtained by ADC conversion of the input signal with the N-bit flash ADC. After that, the original input is subtracted by the DAC conversion of the N-MSB bits, and is converted with the N-bit flash ADC again to generate the N-LSB bits [110]. To partially compensate the speed loss due to subranging, this architecture can be further modified by a pipelined structure. Track and hold circuit (T/H) are inserted between the adjacent conversion stages. Therefore, the

entire ADC converter does not have to wait for all the stages to finish conversion before sampling a new data, but rather wait for the first stage to finish conversion [110, 111]. However, pipelined structure brings about new design challenges in nonlinearity. Folding in the pipelined structure can be implemented by switched capacitor to reduce the static power consumption of conventional folding amplifier [109, 112–114]. Heavily-used in such ADC, the parasitic capacitances cannot be neglected. They lead to different amplification gains of different stages, resulting in folding gain error. They also attenuate the comparator reference voltages of different stages, resulting in comparator trip point error. Both of them contribute to additional nonlinearity of the ADC. A lot more calibration capacitors and careful as well as customized design of the capacitors are required to cope with such challenges [109, 115]. As a result, flash-ADC is required for the targeted SDR reader while pipelined structure can be spared if the required ADC resolution is less than 6 bits.

The following analysis is carried out to evaluate the required ADC resolution. One network uplink of the reader is UHF RFID. Reader receives backscattered UHF RFID carrier wave from tags when the number of accessed tags is small. Backscattering is physically realized by modulating the reflected radiating wave from reader antenna with varied equivalent load impedance seen by the reader. Modulation depth varies with the equivalent tag impedance difference when switching on and off the driving transistor in serial to the tag antenna. For backscattering with FM0 coding for UHF RFID and backscattering with Manchester coding for 433M RFID [116, 117], system simulation of bit error rate (BER) versus signal-to-noise ratio (SNR) results in an required SNR around 25 dB for BER below 10^{-3} [10, 118, 119]. The other network uplink is UWB-IR. Reader receives UWB-IR signals from tags when the number of accessed tags is large. OOK is utilized as the modulation scheme for UWB-IR signals. The system simulation result of BER versus SNR is approximate 13 dB SNR for 10^{-3} BER [120]. Therefore, a 5-bit ADC is suitable for the SNR specification according to the expression of $SNR = 6.02 \times N + 1.76 + 10 \lg(\frac{f_s}{2 \times f_0})$, where f_s is the sampling rate and f_0 is the signal frequency.

Based on the foregoing analysis and system specification, a 5-bit 1-Gsps flash ADC without pipelined structure is selected for the SDR reader. The spare of pipelining saves the design of switched capacitor and the extra circuit complexity to compensate the discussed challenges. The following paragraph discuss the block diagram and circuit implementation for the ADC.

5.3.3 ADC Implementation and Simulation Results

Distinguished from conventional flash-ADC structure, the comparators integrate functions of thresholds generation and signals amplification so that the separate circuits of reference ladder and pre-amplifier are spared and power consumption and circuit size are reduced. Only [108] and its sequent works [121] have proposed the similar integration. In [108], different thresholds are obtained by intention-

ally unbalancing the size the input differential pairs. The linearity of the different thresholds relies on the approximation accuracy of the linear relationship between I_{ds} and $(V_{gs}-V_{th})$. I_{ds} is the current from the transistor drain node to source node, V_{gs} is the voltage between the transistor gate node and source node, and V_{th} is the transistor threshold voltage. As CMOS process advances, the linear relationship is more and more accurate. However the induced mismatch of differential amplifier structure leads to noise increase which would have been compensated by matched differential pairs. [109] has also reported the idea of only integrating threshold generation but not signal amplification in comparators. It adds a transistor whose gate is connected to supply voltage in parallel to one of the input differential pairs. Different thresholds are achieved by sizing the additional transistor accordingly to add different current in one of the differential pairs. Because the sufficient range of supply voltage, the sizing of the additional transistor can be smaller than that of the differential pairs in [108, 121], reducing power and maintaining speed. However, similar to [108, 121], it also leads to larger offset variation than symmetrical differential pairs and sensitivity to supply variation, and thus required careful calibration [109].

Figure 5.13 illustrates the proposed comparator with the built-in threshold generation and the signal amplification. In this method, size matching of the input differential transistors is maintained. Alternatively, different thresholds are obtained by different combinations of two reference voltages (V_h and V_m). V_h is the “high” reference voltage and V_m is the “low” reference voltage. The current of the left branch of the comparator is $N \times g_m \times (V_{in} - V_{th})$. The current of the right branch of the comparator is $(N - M) \times g_m \times (V_h - V_{th}) + M \times g_m \times (V_m - V_{th})$. N is the number of transistors at each branch, m is the number of transistors that are gated by V_m , g_m is the transistor transconductance, V_{in} is the input voltage, V_{th} is the transistor threshold voltage. The comparator compares the two currents and buffers the output to the rail-to-rail voltage. The comparators generating higher threshold consists of fewer transistors that are gated by V_m whereas more that are gated by V_h . Therefore, the threshold step equals to $\frac{V_h - V_m}{N}$, and the threshold number is N . On one hand, in order to decrease the number of the paralleled transistors for reduced power and increased speed, a portion of the transistors are double-sized compared to the others to offer different weighing. On the other hand, due to the layout structure differences, the simulated relationship between the current conducted by the transistors and the transistor width is not strictly linear when the size is multiplied by larger factors, thus the transistors are not sized to four or eight times. The proposed combination is also shown in Figure 5.13.

Input signal is also amplified by the load transistors and further amplified to rail-to-rail full swing by the subsequent buffers. The amplifier is currently implemented in a static mode. Due to the static amplifier structure, input voltage should also be biased with the common-mode voltage V_m . To reduce the nonlinearity impacts, only the linear operating range of the amplifier is used, which is half of the input range above the V_m based on simulations. For the other input half, its differential input is used instead. Therefore, as illustrated in Figure 5.13, the combination

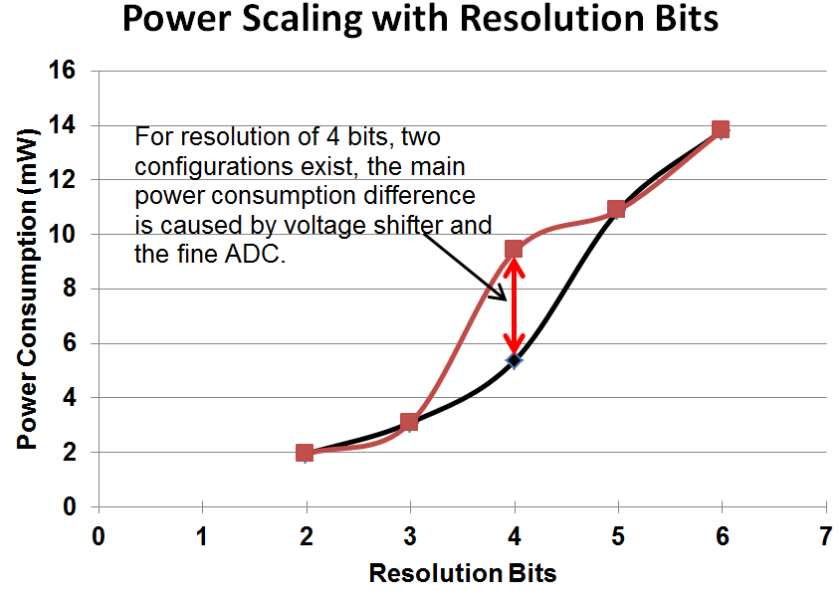


Figure 5.14: Power consumption versus sampling rate with different ADC resolutions.

of two replicated comparator arrays, each of which generates the 16-bit thermal code, form the 32-bit thermal code in total. The 32-bit thermal code is input to a digital pseudo thermal-to-binary translator which is customized design to ensure high speed operation. The amplifier is currently implemented with single-ended output so there still exists mismatch which can cause output common-mode voltage shift. To cope with this problem in current design, the scalability of the bias current of the static amplifier is re-used so that the common-mode of the amplifier can be programmed before receiving RF signals.

As a conclusion, a 5-bit 1-Gsps flash ADC without pipelined structure is selected as a trade-off between speed and circuit complexity after system analysis, and is implemented by comparators with self-generated thresholds and signal amplification. In future implementation, it is preferred to modify the static amplifier with a dynamic counterparts so that power is only consumed during the comparison process [108, 109, 121]. It is also preferred to modify the single-ended output with full-differential output so that mismatch is further depressed.

Figure 5.14 shows the simulated power consumption versus sampling rate with different ADC resolutions (black curve). The comparable results of ADC with folding and pipelined structure is shown in the red curve. The design is power scalable for varied speed and resolution specifications of different communications.

5.4 Summary

This chapter introduces the architecture and design of all-digital polar transmitter and flash ADC for multi-band SDR receiver. By modulating envelop amplitude by pre-generated SDM patterns, the circuit before matching filter of the all-digital transmitter can be realized in digital domain. The circuit is designed by VHDL. System level simulation is carried out for verification. By combining ADC with moderate to wide bandwidth and ADPLL tuning range, the receiver can process multi-band RF signals simultaneously. The architecture of flash ADC is analyzed based on the system specification and the design of comparator with built-in threshold generation and signal amplification in the flash ADC is discussed. Simulation results of power consumption demonstrates its suitability for multi-band SDR receiver.

Chapter 6

Conclusion and Future Works

6.1 Conclusion

This thesis introduces the system and circuit design of interactive RFID for industrial and healthcare IoT applications. Both local and remote display interfaces integrated with RFID tags are studied.

For local display interface or tag-level display interface, one of the flexible EPD technologies, inkjet-printed EC display, is utilized. The electronic performance of EC display is studied to quantize the charging and discharging current and energy for display switching [**Paper I**]. Based on that, a passive UHF RFID tag integrated with inkjet-printed EC display is designed and implemented in 4.5 mm²-sized UMC 180-nm CMOS process. Duty-cycled dual-supply power management scheme and single-pixel display addressing scheme are designed based on the energy sensitivity of EC display. With the two schemes, the switching energy of EC display can be accumulated over multiple cycles of power management unit. The measured sensitivity of UHF RFID tag for display switching is -10.5 dBm at 11.7 sec/cm² update rate [**Paper II**, **Paper VI**].

For remote display interface, UWB transmitter is integrated in the UHF RFID tag and substitutes UHF RFID backscattering circuit. The performance of UWB transmission is studied and compared with other short-ranged communication technologies. It is a most suitable solution for real-time communication of massive number of tags because of its Mbps data rate and tens of μ W active power consumption. For application demonstration, a semi-passive UHF/UWB RFID tag with ECG sensor is designed and implemented in 6 mm²-sized UMC CMOS 180-nm process [**Paper III**, **Paper IV**, **Paper VII**]. The wireless ECG tag is attached to the body of patient and transmits his ECG signals to remote centralized monitor in real time. UWB transmission and ADC sampling of ECG signals are activated in intervals so that the sampled ECG signals during two consecutive UWB transmissions are buffered in tag registers and transmitted in burst mode when transmission is activated. The much higher data rate of UWB transmission over required ECG

sampling rate makes such scheme feasible. Tag operation flow is designed based on this scheme. Additionally, to improve patient comfort, inkjet-printed paper-based ECG electrode is utilized. An analog frontend which filters and amplifies the captured ECG signals by the paper-based ECG electrodes is designed with high input impedance as well as adjustable bandwidth and gain. The optimum number of accessed tags for real time ECG transmission is proved to be 400 tags/second at 1.5 KHz ECG sampling rate with 10 Mbps UWB pulse rate or 40 tags/second at 1.5 KHz ECG sampling rate with 1 Mbps UWB pulse rate. Moreover, tag-level display is also integrated in the UHF/UWB RFID ECG tag to facilitate patient identification. Battery is used to ensure fast display update rate for alert information. And therefore, a battery management unit is also designed to transmit out-of-battery alert when battery is low. For future tag version, printed UHF and UWB antenna are to replace the conventional antenna connection in this tag version, and flip chip interconnection with Anisotropic Conductive Adhesives (ACF) as well as inkjet-printed lines have been verified possible interconnection methods for UHF RFID chip.

Furthermore, a multi-band SDR transceiver for interactive RFID system is studied and designed for different RFID bands and sub-1GHz UWB bands [Paper V]. An all-digital polar transmitter where all the blocks except off-chip matching filter can be designed in digital domain and the digital circuits except Class-D PA can be implemented by VHDL is proposed and discussed. The performance in both time domain and frequency domain are presented. A multi-band receiver with moderate-to-wide IF frequency band based on sliding-IF architecture is proposed. Correspondingly, a flash-ADC with up to 1 Gsps sampling rate is designed and analyzed for the moderate-to-wide IF bandwidth. The simulated power consumption of ADC is scalable for both bandwidth and resolution.

6.2 Future Works

In following of this dissertation and to make the complete proposed interactive RFID system work, the following researches are suggested for future work:

- Heterogeneous integration of the inkjet-printed UHF and UWB antenna with the proposed tag

Printed antenna are the biggest missing part in terms of a fully flexible and complete interactive UHF/UWB RFID display tag. The performances of printed UWB-IR antenna are to be surveyed and the related matching network for the printed antenna and the chip is to be studied before implementing the heterogeneous integration of the printed antenna with the proposed tag.

- UHF/UWB RFID tag with other EPD technologies

EPD technologies are now undergoing fast development, and the performances of driving voltage, response time and power consumption etc. are keeping

changing. With the rising interests in user-interaction systems, it is interesting to research more tags, especially passive tags, with other kinds of EPD technologies based on the design schemes of the proposed wireless display tag.

- SDR reader for the UHF/UWB RFID system

SDR transceiver or reader which receives UWB-IR signals and transmit different bands of RFID signal is still one important role in the proposed UHF/UWB RFID system. For reception of the UWB-IR signals, every narrowband system in the vicinity is a potential interferer and also every other carrierless system. Thus the reader must be improved with relatively complex and sophisticated signal processing techniques to recover the communications data from this noisy environment. Such researches in the SDR design is meaningful.

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