Low-frequency Noise in High-k Gate Stacks with Interfacial Layer Engineering

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Abstract

The rapid progress of complementary-metal-oxide-semiconductor (CMOS) integrated circuit technology became feasible through continuous device scaling. The implementation of high-k/metal gates had a significant contribution to this progress during the last decade. However, there are still challenges regarding the reliability of these devices. One of the main issues is the escalating $1/f$ noise level, which leads to degradation of signal-to-noise ratio (SNR) in electronic circuits.
The focus of this thesis is on low-frequency noise characterization and modeling of various novel CMOS devices. The devices include PtSi Schottky-barriers for source/drain contacts and different high-k gate stacks using HfO_2, $LaLuO_3$ and Tm_2O_3 with different interlayers. These devices vary in the high-k material, high-k thickness, high-k deposition method and interlayer material. Comprehensive electrical characterization and low-frequency noise characterization were performed on various devices at different operating conditions. The noise results were analyzed and models were suggested in order to investigate the origin of $1/f$ noise in these devices. Moreover, the results were compared to state-of-the-art devices.
High constant dielectrics limit the leakage current by offering a higher physical dielectric thickness while keeping the Equivalent Oxide Thickness (EOT) low. Yet, the $1/f$ noise increases due to higher number of traps in the dielectric and also deterioration of the interface with silicon compared to SiO_2. Therefore, in order to improve the interface quality, applying an interfacial layer (IL) between the high-k layer and silicon is inevitable. Very thin, uniform insitu fabricated SiO_2 interlayers with HfO_2 high-k dielectric have been characterized. The required thickness of SiO_2 as IL for further scaling has now reached below 0.5 nm. Thus, one of the main challenges at the current technology node is engineering the interfacial layer in order to achieve both high quality interface and low EOT. High-k ILs are therefore proposed to substitute SiO_x dielectrics to fulfill this need. In this work, we have made the first experiments on low-frequency noise studies on TmSiO as a high-k interlayer with Tm_2O_3 or HfO_2 on top as high-k dielectric. The $TmSiO/Tm_2O_3$ shows a lower level of noise which is suggested to be related to smoother interface between the TmSiO and Tm_2O_3. We have achieved excellent noise performance for $TmSiO/Tm_2O_3$ and $TmSiO/HfO_2$ gate stacks which are comparable to state-of-the-art SiO_2/HfO_2 gate stacks.

Keywords: CMOS, high-k, $1/f$ noise, low-frequency noise, number fluctuations, mobility fluctuations, traps, interfacial layer, TmSiO, Tm_2O_3.

Sammanfattning

Den snabba utvecklingen av integrerade kretsar, baserade på komplementär metall-oxid-halvledare (CMOS) tekniken, blev möjlig genom oavbruten komponent skalning. Införandet av s.k. hög-k/metal-gate var ett viktigt bidrag till dessa framsteg under det senaste decenniet. Emellertid finns det fortfarande problem när det gäller tillförlitligheten hos dessa komponenter. Ett av de viktigaste problemen är den högre $1/f$- eller lågfrekvens-brusnivån, vilket leder till sämre signal-brusförhållande (SNR) i elektroniska kretsar.
Fokus i denna avhandling är på karakterisering och modellering av lågfrekvent brus i denna typ av avancerade komponenter. Avhandlingen utforskar inverkan av olika processteg speciellt Schottky-kontakter för source-drain och olika hög-k stackar såsom HfO_2, $LaLuO_3$ och Tm_2O_3 med olika mellanskikt. De undersökta komponenterna varierar med avseende på hög-k materialet, tjockleken, deponeringstekniken och valet av mellanskiktsmaterial. Omfattande elektrisk och lågfrekvensbrus-karakterisering utfördes på olika komponenter. Brusresultaten analyserades och modeller föreslogs för att undersöka ursprunget till $1/f$-bruset i dessa komponenter. Dessutom jämfördes resultaten med tidigare publicerade studier på state-of-the-art komponenter.
Hög konstants dielektrikum begränsar läckströmmen genom att erbjuda en högre fysisk dielektrisk tjocklek samtidigt som den motsvarande oxidtjocklek(EOT) blir lägre. Ändå ökar $1/f$ bruset på grund av ett ökat antal fällor i det dielektriska lagret och även p.g.a. en försämring av gränsytan eller interfacet mot kisel jämfört med SiO_2. Därför, bör man förbättra gränsytans kvalitet, genom att applicera ett tunt lager eller mellanskikt (IL). Tidigare har SiO_x ofta använts som ett IL eftersom det ger en bra gränsyta med kisel. Mycket tunna, SiO_x lager baserade på ALD med HfO_2 hög k dielektrikum har karakteriserats i denna studie. Denerforderliga tjockleken på SiO_x som IL för ytterligare skalning har nu nått under 0,5 nm. Därför är en av de största utmaningarna på nuvarande tekniknod att hitta en alternativ lösning för detta tunna lager för att uppnå både hög kvalitet och låg EOT. Ett lämpligt dielektrikum med högre k-värde föreslås därför att ersätta SiO_x. I detta arbete har vi gjort de första lågfrekvensbrus-studierna på TmSiO som ett high-k mellanskikt med Tm2O3 eller HfO2 på toppen som hög-k dielektrikum. Jämförelsen av dessa två gatestackar visar att TmSiO /Tm_2O_3 ger en lägre brusnivå, vilket kan förklaras av ett bättre interface mellan TmSiO och Tm_2O_3 jämfört med fallet då man använt ett HfO_2 lager. Vi har demonstrerat utmärkta brusprestanda för TmSiO/Tm_2O_3 och TmSiO/HfO_2 i jämförelse med SiO_2/HfO_2 gatestackar.

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I would like to thank my dear parents for believing in me, encouraging me through all these academic years and for their unconditional love and support.
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List of Symbols and Acronyms

Symbol	Unit	Meaning
$\mathbf{C}$	F(F/cm^2)	Capacitance (capacitance per area)
$\mathbf{C_{ox}}$	F/cm^2	Gate oxide capacitance per unit area
$\mathbf{E}$	J (eV)	Energy
$\mathbf{E_c}$	J (eV)	Conduction band energy
$\mathbf{E_i}$	J (eV)	Intrinsic Fermi level energy
$\mathbf{E_v}$	J (eV)	Valence band energy
$\boldsymbol{f}$	Hz	frequency
$\boldsymbol{f(E)}$		Fermi-Dirac distribution function
$\mathbf{g_m}$	S=A/V	transconductance
$\mathbf{I}$	A	Current
$\mathbf{k}$	J/K	Boltzmann's constant (1.38×10^{-23})
$\mathbf{L}$	µm	Gate length
$\mathbf{m^*}$	kg	Electron effective mass
$\mathbf{N}$		Number of carriers
$\mathbf{N_t}$	cm^{-3}eV^{-1}	Oxide trap density per unit volume
$\mathbf{N_{tIL}}$	cm^{-3}eV^{-1}	Inerfacial layer trap density per unit volume
$\mathbf{N_{tHK}}$	cm^{-3}eV^{-1}	High-k dielectric trap density per unit volume
$\mathbf{n}$	cm^{-3}	Concentration of carriers per unit volume
$\mathbf{q}$	C	Electronic charge (1.602×10^{-19}C)
$\mathbf{Q_i}$	C/cm^2	Inversion charge per unit area
$\mathbf{Q_{ox}}$	C/cm^2	Oxide charge per unit area
$\mathbf{R}$	Ω	Resistance
$\mathbf{S_{ID}}$	A^2/Hz	Power spectral density of the drain current
$\mathbf{S_N}$	1/Hz	Power spectral density of carrier number fluctuations
$\mathbf{S_{VG}}$	V^2/Hz	Power spectral density of the input gate voltage noise
$\mathbf{S_{V\mathit{fb}}}$	V^2/Hz	Power spectral density of the flat-band voltage noise
$\mathbf{S_{Qox}}$	C^2/cm^{4}Hz	Power spectral density of the oxide charge density fluctuations
$\mathbf{T}$	K	Absolute temperature
$\mathbf{T_{IL}}$	nm	Interfacial layer thickness
$\mathbf{T_{HK}}$	nm	High-k dielectric thickness
$\mathbf{t}$	s	time
$\mathbf{t_{ox}}$	nm	Gate oxide thickness
$\mathbf{V}$	V	Voltage
$\mathbf{V_{DS}}$	V	Drain to source voltage
$\mathbf{V_{fb}}$	V	Flat-band voltage
$\mathbf{V_G}$	V	Gate voltage
$\mathbf{W}$	µm	Gate width
$\boldsymbol{\alpha}$	Vs/C	Scattering parameter
$\boldsymbol{\alpha_H}$		Hooge parameter
$\boldsymbol{\xi}$	eV^{-1}	Fitting parameter defining the energy dependence of traps

γ		Frequency exponent
γ_{IL}		Tunneling coefficient for the interfacial layer
γ_{HL}		Tunneling coefficient for the high-k dielectric
η	cm^{-1}	Fitting parameter for the density of traps
λ	cm	Tunneling attenuation length
μ	cm^2/Vs	Carrier mobility
μ_{ac}	cm^2/Vs	Mobility limited by scattering with surface acoustic phonons
μ_b	cm^2/Vs	Mobility limited by scattering with bulk phonons
μ_C	cm^2/Vs	Mobility limited by Coulomb scattering
μ_{eff}	cm^2/Vs	Effective mobility
μ_{sr}	cm^2/Vs	Mobility limited by surface roughness scattering
τ	s	Time constant of GR noise
τ_0	s	Tunneling time constant
ω	rad/s	Angular frequency
Φ_B	J	Energy barrier height

Acronyms	**Meaning**
ALD	Atomic Layer Deposition
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
CV	Capacitance-Voltage
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
FDSOI	Fully Depleted Silicon-on-Insulator
FFT	Fast Fourier Transform
GR	Generation-Recombination
IC	Integrated Circuit
IL	Interfacial Layer
LFN	Low Frequency Noise
MBE	Molecular Beam Epitaxy
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
PDSOI	Partially Depleted Silicon-on-Insulator

PSD	Power Spectral Density
RTA	Rapid Thermal Anneal
RTS	Random Telegraph Signal
SIMOX	Separation by Implantation of Oxygen
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
STL	Sidewall Transfer Lithography
UTB	Ultra-Thin Body
VCO	Voltage Controlled Oscillator
WKB	Wentzel-Kramers-Brillouin

List of Appended Papers

Paper I: B. G. Malm, **M. Olyaei** and M. Östling, “Low-frequency noise in FinFETs with PtSi Schottky barrier source-drain contacts”, International Conference on Noise and Fluctuations (ICNF), Toronto, June 2011.

Paper II: **M. Olyaei**, B. G. Malm, P.-E. Hellström and M. Östling, “Low-frequency noise in high-k $LaLuO_3$/TiN MOSFETs”, Solid State Electronics, vol. 78, pp. 51-55, Dec 2012.

Paper III: **M. Olyaei**, B. G. Malm, E. Dentoni Litta, P.-E. Hellström and M. Östling, “A study of low-frequency noise in high-k/metal gate stacks with insitu SiO_x interfacial layer”, International Conference on Noise and Fluctuations (ICNF), Montpellier, June 2013.

Paper IV: **M. Olyaei**, B. G. Malm, E. Dentoni Litta, P.-E. Hellström and M. Östling, “Improved low-frequency noise for 0.3 nm EOT thulium silicate interfacial layer", European Solid State Device Conference (ESSDERC), Venice, Sep 2014

Paper V: **M. Olyaei**, E. Dentoni Litta, P.-E. Hellström, M. Östling and B. G. Malm, “Low-frequency noise characterization of ultra-low Equivalent-Oxide-Thickness thulium silicate interfacial layer nMOSFETs", accepted for publication in IEEE Electron Device Letters, Oct 2015.

Publications not included in the thesis

Paper 1: **M. Olyaei**, B. G. Malm, P.-E. Hellström and M. Östling, "Low-frequency noise in high-k $LaLuO_3$/TiN MOSFETs ", International Semiconductor Device Research Symposium (ISDRS), College Park MD , Dec 2011

Paper 2: M. Östling, C. Henkel, E. Dentoni Litta, G. B. Malm, P.-E. Hellström, M. Naiini, **M. Olyaei**, S. Vaziri, O. Bethge, E. Bertagnolli and M. C. Lemme, "Atomic layer deposition-based interface engineering for high-k/metal gate stacks", Solid State and Intergrated Circuit Technology (ICSICT), Xian, Nov 2012.

Summary of Appended Papers

Paper I. Low-frequency noise in FinFETs with PtSi Schottky barrier source-drain contacts. This paper reports the effect of dopant segragation in low frequency noise of Schottky barrier MOSFETs. As or B dopant segragation has been used as a method to reduce the Schottky barrier height in FinFETs and Ultra-Thin-Body devices (UTBs). Noise studies have been perfomed on both nMOS and pMOS and n-channel FinFETs. It is shown that the dopant segragation method increases the on-current and decreases the low frequency noise significantly in pMOSFETs. The author has performed 80% of the low-frequency noise characterization and other electrical characterization and, 60% of data analysis and modeling and 50 % writing the manuscript.

Paper II. Low-frequency noise in high-k $LaLuO_3$/TiN MOSFETs. This paper investigates the low frequency noise in different samples with $LaLuO_3$ high-k layer with no interfacial layer and $LaLuO_3$ high-k with SiO_2 interfacial layer. The motivation of this study was to evaluate the quality of $LaLuO_3$ as a high-k dielectric candidate in MOSFETs. This was the first noise study on $LaLuO_3$ MOSFETs. The low-frequency noise studies reports a higher noise for $LaLuO_3$ samples. The extracted trap density is 2×10^{18} for 6 nm and 20 nm high-k samples without an interfacial layer and 2×10^{17} for the sample with a 5 nm SiO_2 interfacial layer. The implementation of a SiO_2 interfacial layer can reduce the noise level significantly. The author has performed 90% of the low frequency noise characterization and other electrical characterization, performed all data analysis and modeling and 90% writing the manuscript.

Paper III. A study of low-frequency noise in high-k/metal gate stacks with insitu SiO_x interfacial layer. In this paper chemical oxide SiO_x interfacial layers fabricated insitu in the Atomic Layer Depostion (ALD) equipment have been studied. All samples have different SiO_x thicknesses deposited in the ALD using different reactants such as O_3 and H_2O and different pulsing schemes and temperatures. This fabrication method provides very uniform and thin layers. Hafnium oxide has been deposited on top in the same ALD. The low frequency noise measurements show higher noise for chemical oxide MOSFETs comparing to the reference exsitu fabricated MOSFET. However the noise level for the H_2O method is lower than other chemical methods reported. The author has performed 100% of the low frequency noise characterization and other electrical characterizations, 100% data analysis and modeling and 90% writing the

manusript. The author presented the paper as a poster at ICNF 2013 in Montpellier, France.

Paper IV. Improved low-frequency noise for 0.3 nm EOT thulium silicate interfacial layer. This paper investigates the low-frequency noise in MOSFETs with Thulium silicate interfacial layer and thulium oxide as high-k dielectric. This is the first study performed on a non-silicon dioxide interfacial layer with ultra-thin EOT (0.3 nm). The comparison of noise results with state-of-the-art SiO_x-HfO_2 benchmark data with thin interlayers shows an improved noise level for nMOSFETs and comparable for pMOSFETs. The author has performed 100% of low-frequency noise characterization and other electrical charactrizations, 100% data analysis and modeling and 90% writing the manuscript. The author gave an oral presentation of the paper at ESSDERC 2014 in Venice, Italy.

Paper V. Low-frequency noise characterization of ultra-low Equivalent-Oxide-Thickness thulium silicate interfacial layer MOSFETs. This paper includes comprehensive low frequency noise characterization on nMOSFETs with ultra -low EOT TmSiO/HfO_2 gate stacks with 0.65 nm total EOT and TmSiO/Tm_2O_3 with 1.2 nm total EOT. This is a novel study on MOSFETs with non-silicon dioxide interlayer and ultra-low EOT. These devices show promising low frequency noise properties and reasonable average oxide trap density values. The comparison between these two gate stacks reports lower noise level for TmSiO/Tm_2O_3 gate stacks which is suggested to be due to the more uniform interface between TmSiO and Tm_2O_3. The author has performed 100% of low-frequency noise characterization and other electrical charactrizations, 100% data analysis and modeling and 90% writing the manuscript.

Chapter 1

Introduction

1.1 Background

Semiconductor technology entered a new era with the introduction of Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) in 1960s. The MOSFET became the key component in nearly all electronic circuits. In 1965, Gordon Moore predicted that the number of transistors in an integrated circuit (IC) doubles every year [1]. Since then, a great progress is observed in Complementary-Metal-Oxide-Semiconductor (CMOS) technology. In order to fit more transistors in a chip, the dimension of devices shrank, followed by reducing the voltage and current which led to power dissipation reduction per transistor. As the oxide thickness became lower, leakage current increased which started limiting the scaling trend. At this point new materials were needed to enable further scaling. High-k dielectrics were implemented in 2007 providing low Equivalent Oxide Thickness (EOT) while the actual physical thickness is higher solving the tunneling problem [2] [3]. The introduction of high-k dielectrics was the greatest change in CMOS technology since the invention of MOSFETs. Different high-k materials have been studied as an oxide choice for CMOS transistors. Among all, hafnium oxide (HfO_2) together with a thin SiO_2 interlayer has been commonly used in different technologies. However as further scaling has become challenging, new materials and techniques are required to keep the scaling trend ongoing [4].
Downscaling also brought some undesired effects such as increased low-frequency noise levels in smaller devices. In electronics, noise refers to a random fluctuation in an electrical signal. It cannot be totally eliminated and it sets a lower limit to the smallest detectable signal. In MOSFETs, the noise in low frequency which is called $1/f$ noise or flicker noise has a power spectral density (PSD) inversely proportional to the frequency [5]. This noise is more significant in lower frequencies but it also affects higher frequencies. In some circuits such as Voltage Controlled Oscillators (VCOs) the $1/f$ noise is up converted to phase noise which limits the system's ability to separate adjacent channels [6]. Therefore, reducing the low-frequency noise is very important. In order to minimize the $1/f$ noise, a deep understanding of the sources of this noise in MOSFETs is required. Low-frequency noise in MOSFETs originates from the traps and defects in the oxide or the fluctuations in

the mobility of carriers in the channel due to lattice vibrations. Investigating the $1/f$ noise helps to get information about the physics of the device.
In this thesis, the main focus is on the study of low frequency noise as a tool to investigate the quality of the dielectrics and the locations of traps. The devices in this work are designed and fabricated in Electrum laboratory at KTH. Most of the devices are double-layer high-k dielectrics with different interlayers and high-k materials. The devices have been characterized and the noise measurement results have been analyzed and suitable noise models have been suggested. The study of low-frequency noise in MOSFETs with novel non-silicon ultra-thin interlayers is presented in this thesis.

1.2 Previous work in low-frequency noise

The state of the art work on low-frequency noise contains a great number of papers on high-k dielectric gate stacks. These gate stacks show increased number of traps comparing to the conventional ones with SiO_2 dielectric, therefore the research is mostly pointed towards finding the reasons behind this excessive amount of noise and proper ways to diminish it.
Imec, as one of the leading groups in the field has performed a lot of research on hafnium based oxides and double layer dielectric gate stacks [7] [8] [9]. They have reported SiO_2/HfO_2 gate stacks with 1 nm total EOT with oxide trap density (N_t) around 5.5×10^{18} cm^{-3} eV^{-1} [10] [11].
Butler *et al* have also published research on noise in high-k gate stacks [12] [13]. They have suggested a modified noise model to include the effect of both layers in double layer gate stacks [14] [15] [16].
Rare earth oxides containing lanthanum, lanthanum lutetium and thulium have been implemented in MOSFETs as high-k dielectric candidates. Research has been performed on low frequency noise in these gate stacks, mostly Lanthanum oxide stacks [17] [18]. Lanthanum lutetium oxide has also been studied by the research group in Julich [19] [20] [21]. Further noise studies on lanthanum lutetium oxide are included in this thesis.
Ghibaudo *et al* have also published papers on low frequency noise in nanoscale MOSFETs and FinFETs [22] [23]. Their results on 28 nm n-channel and p-channel MOSFETs confirmed correlated number and mobility fluctuation for all regions of operation. This led to analytical expression for $1/f$ noise model enabling the prediction of noise in transistors with any dimension. In [23] , low-frequency noise analysis of FinFETs in terms of different channel length and fin width is investigated.
Previously at KTH, low-frequency noise in strained Si and SiGe MOSFETs, SiGe pMOSFETs with Schottky barrier source/drain contacts and MOSFETs with high-k/metal gate stacks had been studied [24].
In this work low-frequency noise in Schottky barrier source/drain UTBs and FinFETs with dopant segregation have been investigated. The $1/f$ noise research on high-k/metal gate stacks is continued with different structure high-k MOSFETs with different interfacial layers.

1.3 Thesis structure

This thesis is organized as follows.
Chapter 2 reviews advanced gate stack MOSFETs and the effect of interfacial layers in these stacks and the quality of the dielectrics by comparing the reported oxide trap densities. In Chapter 3, the fundamental noise sources in electronic devices are described. The emphasis is on the low-frequency part of the spectrum. In Chapter 4, the origin of $1/f$ noise in MOSFETs is explained in detail. It also includes the modeling for both single layer and double layer gate stacks. Chapter 5 gives a comprehensive sample overview including some process details. This is followed by describing the measurement setup. In Chapter 6, the noise properties of the different gate stacks is summarized and discussed. Finally in Chapter 7 a summary of the work together with main conclusions and future perspective is presented.

Chapter 2

Nano-scaled MOSFETs

This chapter gives a summary of the MOSFETs with nano-scale high-k gate stacks previously published. The impact of an interfacial layer (IL) in high-k/metal gate stacks is discussed. Different IL/high-k configurations are compared through their oxide trap density values. The chapter ends with a short introduction of Schottky barrier source/drain contacts and SOI MOSFETs which are also investigated in this thesis.

2.1 High-k metal gate stacks

Since the introduction of metal-oxide-semiconductor-field-effect-transistors (MOSFETs), SiO_2 has been the gate dielectric used in MOS devices for more than 40 years. As semiconductor industry approaches scaling limits, the implementation of high-k dielectrics become necessary to continue the path of Moore's law.
High-k dielectrics, firstly announced by IBM [2] and Intel [3] at 45nm node, enable aggressively scaled EOT, while keeping the leakage current low. This is shown in Fig 2.1 that a thicker high-k dielectric can be used with the EOT corresponding to a very thin SiO_2 layer. Several high-k materials have been under study for a decade, such as Hafnium, Aluminum, Lanthanum and Zirconium base oxides [25] [26] [27]. Most of the high-k dielectrics are unstable on Si [28]. These dielectrics react with Si and form an undesirable interfacial layer which can alter the barrier height. The barrier height or the band offset refers to the alignment of the bands between the Si and oxide. Reducing this barrier height causes emission of carriers leading to gate leakage current. Among all, HfO_2 is the most promising high-k candidate which fulfills the desired properties for CMOS technology. HfO_2 has a relatively high dielectric constant k~17-30, wide band gap and offsets to Si, good thermal stability and compatibility with conventional CMOS technology.
The gate electrode material choice is also of great importance in device performance mainly in order to set the threshold voltage for both n-channel and p-channel devices. The most promising gate materials to combine with high-k dielectrics are metal gates. Although poly silicon gates were successfully implemented with SiO_2 dielectric, the combination of them with high-k dielectrics

is not a suitable alternative. High-k/poly Si gate transistors show high threshold voltage because of Fermi level pinning at poly Si/high-k interface and also channel mobility degradation. Metal gates can screen the phonon scattering in high-k dielectrics resulting in improved channel mobility. Metal gates can also eliminate poly depletion and resistivity effects arising from polysilicon gates. High-k dielectric metal gates are now an enabling technology for MOSFET advanced gate stacks [29].

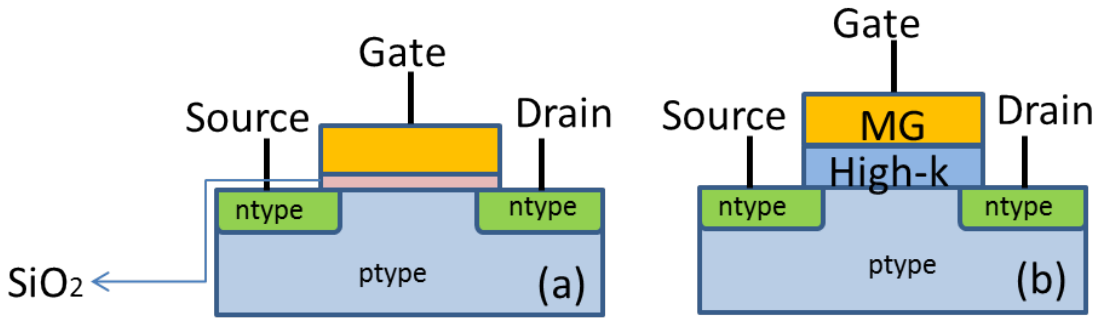


Fig. 2.1. Conventional MOSFET with SiO_2 and poly silicon gate stack (a), High-k/Metal gate stack with a thicker dielectric corresponding to the same EOT or lower(b).

2.1.1 Implementation of an interfacial layer for high-k MOSFETs

By implementing high-k dielectrics directly on silicon, a higher physical thickness is achieved with the same EOT, however, the interface with silicon is deteriorated compared to SiO_2. This poor interface causes mobility and reliability issues. The interface quality is defined by the metric interface state density (D_{it}). D_{it} values of high-k dielectric MOSFETs are reported to be in the range of 6×10^{11} and 5×10^{13} [5] [30]. In order to achieve a better interface with silicon, an interfacial layer (IL) is intentionally deposited between the Si channel and high-k layer for interface improvement. Dual layer dielectric stacks contain a high-k layer and an IL layer which ensure both low EOT through top layer high-k dielectric and good interface quality with silicon by using an appropriate IL [31].
The dielectric constant of this IL is usually lower than the high-k dielectric constant, resulting in a higher EOT of the gate stack. Applying this IL can also reduce the gate current since the dielectric constant and band gap are inversely proportional. Although an IL increases the EOT, the better interface reduces the mobility degradation caused by coulomb or interface scattering. Therefore a suitable IL layer with optimized thickness can provide the satisfactory trade-off between EOT and mobility.
The most commonly used IL is SiO_2, which provides good quality interface with silicon. SiO_x together with a high-k dielectric offers low EOT gate oxide, with good mobility and interface. In order to follow the scaling trend, the thickness of the IL needs to be lower than 0.5 nm. Achieving thinner SiO_x is challenging and several techniques have been surveyed in this direction among which IL scavenging is mainly under focus.

IL scavenging was first introduced by Kim *et al.* through applying a Ti over-layer on HfO_2 or ZrO_2 gate dielectrics [32]. Although the technique was modified a lot since then by changing the scavenging elements, process temperature and location of scavenging element, it is still challenging to achieve a thin SiO_x IL without deteriorating the mobility and the interface.
Alternative materials with higher-k dielectric are thus researched to be substituted as an IL layer by SiO_x. The most promising high-k IL materials are silicates which provide scaled EOT and reasonable interface state quality and mobility. Lanthanum silicate which has been vastly studied is formed as an IL layer by applying a La_2O_3 cap on Hf-based high-k layer MOSFETs [33]. The La elements diffuse through the high-k layer after high temperature annealing, forming the silicate layer. This new IL has a higher dielectric constant compared to SiO_2, contributing to desired lower EOT. Another good candidate among silicates is thulium silicate (TmSiO) which has been recently reported as an IL with reasonably high dielectric constant and promising reliability results. A process flow compatible with gate-last CMOS technology has also been developed for TmSiO IL [34] [35]. This is a great advantage as compatibility to CMOS technology is a major issue in implementing new higher-k ILs. Strontium oxide (SrO) is also a new potential high-k IL which can be deposited before HfO_2 high-k dielectric [36]. In Table 2.1 possible IL alternatives with their respective reported EOTs have been summarized.

Table 2.1. Alternative ILs with respective EOTs.

IL material	IL EOT (nm)
SiO_x/HfO_2	0.4-2 [8] [9]
SiON/HfSiON	0.8-1.8 [14]
$LaSiO/HfO_2$	0.58-0.62 [33]
$TmSiO/Tm_2O_3$	0.3 [Paper IV and V]
SrO/HfO_2	0.5-0.6 [36]

2.1.2 Oxide trap density in high-k MOSFETs

In Table 2.2 trap density values of dielectric layers with different compositions and thicknesses has been reported. The oxide trap density is the number of traps which exist per unit volume. This metric is used to define the quality of the oxide and it is used vastly in this thesis (Chapter 6). Oxide trap densities are extracted through low-frequency noise measurements. Charge pumping is also a possible method to extract the trap densities; but using this method only the traps close the interface (D_{it}) can be extracted [37]. Low-frequency noise measurements are required in order to monitor deep in the oxide [38].
All high-k dielectrics in Table 2.2 are Hf based. The data is taken from published studies in the past 10 years. The samples in this study are not included in this table but discussed in Chapter 6. The results show that oxide trap density is sensitive to the type and thickness of the interfacial layer and the Hf content of the high-k layer. HfO_2 high-k dielectrics shows higher trap density values compared to SiO_2 alternatives. As for dual layers, bringing the HfO_2 layer closer to the Si-SiO_2

increases the trap density. According to the table, for very thin IL layers (IL< 1nm) higher trap density values is observed. This is further discussed in the dual layer modeling Section 4.4. The results also suggest that adding elements such as ZrO_2 to HfO_2 reduces the oxide trap density value.

Table 2.2. Oxide trap density values of different gate dielectrics.

Dielectric material	IL thickness (nm)	High-k thickness (nm)	Trap density (eV^{-1} cm^{-3})
SiO_2-HfO_2 [9]	0.8 4.5	5 5	$5.7x10^{19}$ $1.1x10^{18}$
SiON-HfSiON [14]	0.8 1.8	3 3	$1.82x10^{19}$ $2.12x10^{18}$
SiO_2-HfO_2 [30]	1	4.5	$1x10^{20}$
SiO_2-ZrO_2 added HfO_2 [39]	1	1.6	$8.9x10^{18}$-$5.1x10^{19}$
Chemical SiO_2-HfO_2 Native SiO_2-HfO_2-$HfSiO_x$ Thermal SiO_2-HfO_2 [40]	1 3 4.5	5 1.5 5	$9x10^{19}$ $2x10^{20}$ $7.7x10^{17}$
HfO_2 La_2O_3-HfO_2 (e beam) La_2O_3-HfO_2 (e beam) [17]	0 1 0.5	3 3 3	$5x10^{20}$ $8x10^{19}$ $2x10^{20}$
SiO_2-HfO_2 [10]	0.7	2	$1.3x10^{19}$

2.2 Schottky barrier source/drain contacts

A Schottky barrier is formed when a metal and a semiconductor come into contact. Schottky barrier MOSFETs were introduced as an alternative for low series resistance. These MOSFETs are different from the conventional MOSFETs as the source and drain region are metal silicide contacts with a barrier. This barrier might result in higher noise [41]. Barrier height tuning for both electrons and holes is investigated in Paper I. The fabrication is simpler since there is no need for very high thermal steps and source-drain implantation which makes the process more cost efficient. The process is also fully compatible with CMOS technology [42].

2.3 Silicon-on-Insulator (SOI) MOSFETs

Silicon-on-Insulator (SOI) is the technology of using an insulator layer between two layers of silicon instead of the conventional silicon substrate in MOSFETs. This design provides a reduction in parasitic capacitances resulting in better device performance. The parasitic capacitances reduce due to isolation from the bulk substrate. Fully depleted (FD) SOI technology is a promising candidate for CMOS technology [43] [44] [45]. In an FDSOI device, the silicon region on top of the buried oxide is so thin that the whole region becomes depleted. In our work the Schottky barrier MOSFETs use SOI substrate and FinFETs are fabricated at the same time. The fin height is determined by the silicon body. These devices are also investigated from a noise perspective in Paper I. In Fig 2.2 Ultra-thin body (UTB) and FinFET is shown which is based on an SOI wafer.

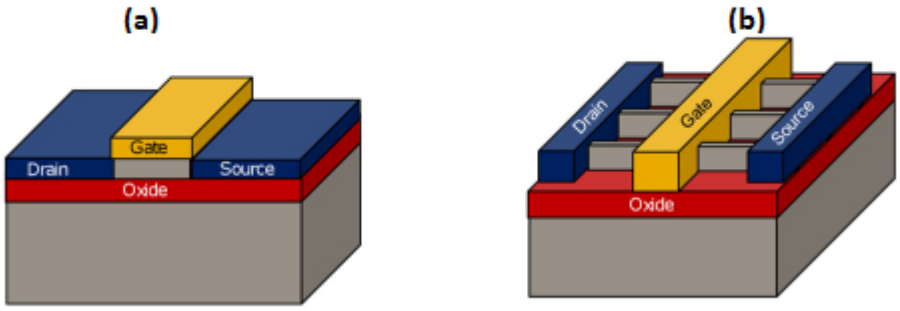


Fig. 2.2. (a) ultra-thin body (b) FinFET-Trigate (adapted from [46]).

Chapter 3

Fundamentals of noise in electronic devices

This chapter gives an overview of the fundamental noise sources in electronic devices. Different noise sources such as thermal noise, shot noise, generation-recombination (GR) noise, random-telegraph (RTS) noise and flicker (1/*f*) noise are described.

3.1 Background

Noise in electronic circuits is defined as random fluctuations in currents and voltages originating in the physics of devices. This noise is different from other disturbances which are due to external sources, such as 50 Hz wall sockets, light and interferences due to other electrical circuits. External noise can often be identified and eliminated by shielding and filtering. While internal sources of noise cannot be totally removed but can be reduced. This is possible by studying the noise in order to get essential information about the device physics and origin of the noise and find methods to reduce the noise.
The signal to noise (SNR) ratio is an important quantity in electronics which represents the ratio of signal strength to the background noise. Achieving a higher SNR ratio is desirable in electronic circuits. However with downscaling, the supply voltage becomes lower and the internal noise of devices becomes higher leading to a lower SNR.
Noise is a stochastic or random signal. Stochastic signals are not predictable and their future values cannot be accurately calculated. These random signals should be analyzed using probability and statistics. Since the average value of current or voltage over time is zero, the best quantity to define noise is a square quantity which is the power spectral density (PSD) denoted by S(f), or equivalently the Fourier transform of autocorrelation function. The unit of S(f) is A^2/Hz and V^2/Hz for PSD of the current noise and voltage noise respectively (equation 3.1).

3.2 Thermal noise

Thermal noise which is also called Johnson or Nyquist noise, is the noise due to thermal random motion of carriers in a material. Thermal noise is uniformly distributed across the frequency spectrum and is referred to white noise. Therefore the PSD of this noise is independent of frequency. Considering a piece of material with R resistance and T temperature, the PSD of thermal noise is written as:

$$S_{\mathrm{I}} = 4kT/R \text{ or } S_{\mathrm{v}} = 4kTR \tag{3.1}$$

Where k is the Boltzmann's constant. According to the equation, the PSD of thermal noise is proportional to the absolute temperature and it equals to zero at T=0 [47].

3.3 Shot noise

Shot noise results from the fact that electron charge is discrete and the motion of these charges are random and independent of frequency. This type of noise is mostly visible in potential barriers. The spectral density of shot noise is proportional to the average current and unlike the thermal noise, it cannot be reduced by lowering the temperature. The PSD of shot noise is shown as:

$$S_I = 2qI \tag{3.2}$$

where q is the electron charge. The shot noise should be distinguished from the device thermal noise which is always present.

3.4 Generation-Recombination noise

Generation-recombination (GR) noise arises due to traps which capture and emit carriers. These traps have energy levels located in the forbidden band-gap. Capture and emission of carriers through these traps causes fluctuations in the number of free carriers. The trapped charge can also cause fluctuations in the mobility, electric field and barrier height. The noise spectral density of generation-recombination noise is a lorentzian. The PSD of GR noise is written as:

$$S_N(f) = 4\Delta N^2 \frac{\tau}{1+(2\pi f)^2\tau^2} \tag{3.3}$$

Where τ is the time constant, ΔN is the fluctuations in the number of carriers and f is the frequency. The generation-recombination noise appears when the Fermi level is within a few kT compared to the trap level [48].

3.5 Random-telegraph noise

Random-Telegraph-Signal (RTS) noise is a special type of generation-recombination noise which occurs when there are one or a few number of traps which contribute to capture and emission of carriers. Transitions between two or more discrete levels are visible in the current or voltage level over time.
RTS noise is mostly reported in very scaled devices since the performance of these devices are highly affected by even a few numbers of traps. The PSD of RTS noise is also a lorentzian [49]. GR noise is the sum of RTS noise from different trap levels.

3.6 1/*f* noise

Low-frequency noise is also called $1/f$ noise or flicker and is referred to fluctuations in the current or voltage of electronic devices which has a PSD proportional to $1/f^{\gamma}$ with γ close to 1. These fluctuations are mostly significant in lower frequencies. The PSD of flicker noise is given as:

$$S_I = \frac{KI^{\beta}}{f^{\gamma}} \tag{3.4}$$

Where K is a constant and β is a current exponent.
Considering the conductivity equation:

$$\sigma = nq\mu \tag{3.5}$$

Where μ is the mobility and n is the concentration of carriers.
The fluctuations leading to $1/f$ noise originates from two sources. There are fluctuations in the number of carriers (ΔN) which is related to GR noise or fluctuations in the mobility of carriers (Δμ) [50] [51]. The sum of several lorentzians from different traps which are independent makes a $1/f$ spectrum. In Fig. 3.1 the superposition of four independent GR noise is shown which gives a total $1/f$ noise spectrum. In Chapter 4, the formal derivation of $1/f$ noise using the trap time constants is found.

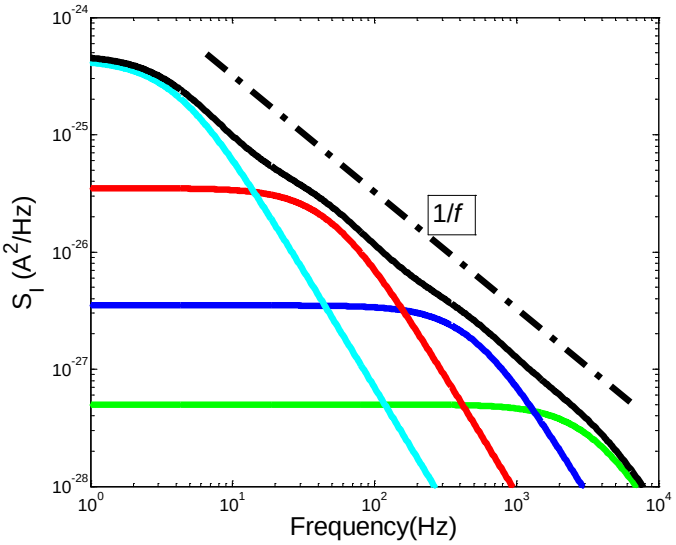


Fig. 3.1. Superposition of four lorentzians resulting in $1/f$ noise.

In summary, fundamental noise sources, their spectral density and current/voltage dependence have been presented in this chapter. In the following chapters, the focus is mainly on $1/f$ noise on MOSFETs. Chapter 4 gives a detailed description of $1/f$ noise sources in MOSFETs followed by noise modeling. In Chapter 5, the sample overview and low-frequency noise measurement set up is explained. Chapter 6 contains the results of noise measurements. GR noise is also investigated in more detail.

Chapter 4

1/*f* noise in MOSFETs

This chapter addresses the $1/f$ noise mechanisms in the drain and gate currents in MOSFETs and the models used for these noise sources.
As discussed in Chapter 3, $1/f$ noise in MOSFETs refers to fluctuations in the low-frequency region with a $1/f$ spectrum. Low-frequency noise in MOSFETs has been studied for a long time in order to discover the origin of these fluctuations. Two different theories were introduced which discussed the $1/f$ noise in MOSFETs. The first theory is based on the fluctuations in the number of carriers in the channel. Since the current in MOSFETs flows through a very narrow region, it is sensitive to the traps located at the interface and in the oxide. The other noise theory is based on fluctuations in the mobility of carriers due to different scattering mechanisms. The correlated number and mobility fluctuation theory assumes that the fluctuations in the number of carriers due to traps affect the mobility of carriers in the channel.

4.1 Number Fluctuations

The number fluctuation noise theory was originally proposed by McWorther [52] in 1957. This theory is based on fluctuations due to trapping and de-trapping of carriers into and out of the traps of the oxide. This will cause fluctuations in the surface potential and inversion charge density leading to drain current noise. Fig. 4.1 illustrates this theory in schematics. It shows that a trap in the oxide can be filled by the carriers in the channel or a filled trap can be emptied and the charge moves to the channel therefore fluctuations occur in the drain current.
Since the number fluctuations are due to trapping and de-trapping of carriers, the equation for GR noise (equation 3.3) can be used:

$$S_{Q_{ox}} = S_{V_{fb}} C_{ox}^2 = \frac{q^2}{W^2 L^2} 4\overline{\Delta N_{ox}^2} \frac{\tau}{1 + (2\pi f \tau)^2} \tag{4.1}$$

where S_{Qox} is the power spectral density of the oxide charge fluctuations, S_{vfb} is the power spectral density of the flat band voltage, C_{ox} is the oxide capacitance, q is

the electron charge, W is the width of the gate, L is the length of the gate, τ is the time constant, *f* is the frequency, and N_{ox} is the number of oxide charges.

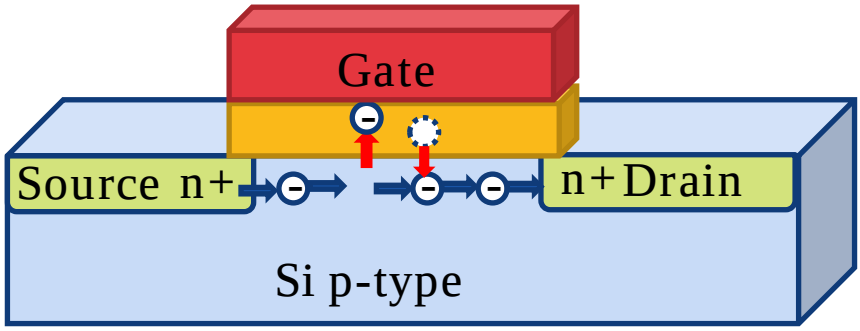


Fig. 4.1. Schematic of trapping and de-trapping of electrons into and out of the traps which causes fluctuations in the drain current.

Taking into account all traps in the gate oxide [53], the power spectral density will be:

$$S_{Q_{ox}} = \frac{q^2}{W^2 L^2} \int_{E_C}^{E_V} \int_0^W \int_0^L \int_0^{t_{ox}} 4N_t f(E)(1-f(E)) \frac{\tau}{1+(2\pi f\tau)^2} dxdydzdE \qquad (4.2)$$

The probability that the traps are occupied is calculated according to the Fermi-Dirac distribution function:

$$f(E) = \left[1 + e^{(E-E_{F,n(p)})/KT}\right]^{-1} \qquad (4.3)$$

Assuming that only traps around the quasi-Fermi level contribute to fluctuations: f(E)(1-f(E))= -kTdf(E)/dE and N_t is the density of traps at the quasi-Fermi level. The power spectral density turns into:

$$S_{Q_{ox}} = \frac{q^2 kT}{WL} \int_0^{t_{ox}} 4N_t \frac{\tau}{1+(2\pi f\tau)^2} dz \qquad (4.4)$$

The trapping time constant through tunneling is calculated as shown below:

$$\tau = \tau_0(E).e^{z/\lambda} \qquad (4.5)$$

where λ is the tunneling attenuation length calculated through the Wentzel-Kramers-Brillouin (WKB) theory:

$$\lambda = \left[\frac{4\pi}{h}\sqrt{2m^*\varphi_B}\right]^{-1} \qquad (4.6)$$

where h is the plank constant, m^* is the carrier effective mass and φ_B is the barrier height for tunneling in the gate stack material. In this thesis different gate stack materials have been investigated. Tunneling attenuation length has been estimated for $TmSiO/Tm_2O_3$ gate stack. This estimation is based on the barrier height of Tm_2O_3 and average of effective masses of SiO_2 and HfO_2 which is discussed in Section 6.3.
Applying the trapping time constant equation into the power spectral density of the flat-band voltage gives:

$$S_{V_{fb}} = \frac{q^2 kT\lambda N_t}{f^{\gamma} WLC_{ox}^2} \tag{4.7}$$

where γ is the frequency exponent. If γ=1, the number fluctuation model will show $1/f$ slope which means that the trap density is uniform in depth. Non-uniform trap density results in deviations in γ [54].

4.2 Mobility Fluctuations

The drain current noise can also be a result of fluctuations in the mobility of carriers which was first suggested by Hooge [55] through the following equation:

$$\frac{S_I}{I^2} = \frac{\alpha_H}{fN} \tag{4.8}$$

$$\frac{S_I}{I^2} = \frac{q\alpha_H}{fWLQ_i} \tag{4.9}$$

Where Q_i is the carrier density and α_H is the Hooge parameter.
Considering different scattering mechanisms that are present in the MOSFET such as bulk phonon mobility (μ_b), mobility limited by surface acoustic phonon (μ_{ac}), mobility limited by surface roughness scattering (μ_{sr}) and mobility limited by Coulomb scattering (μ_C) according to Matthiessen's rule the effective mobility will be :

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_C} \tag{4.10}$$

The α_H does not depend only on material quality but each scattering parameter has an influence on the Hooge parameter. If each scattering parameter has the mobility μ_j and the Hooge parameter $\alpha_{H,j}$, the total α_H will be:

$$\alpha_H = \sum_j \frac{\mu_{eff}^2}{\mu_j^2} \alpha_{H,j} \tag{4.11}$$

If carrier density is not uniform along the channel the noise equation will be:

$$\frac{S_I}{I^2} = \frac{q\alpha_H}{fWL} \int_0^L \frac{dx}{Q_i(x)} = \frac{q\alpha_H}{fL^2} \int_0^{V_{DS}} \frac{\mu_{eff}}{I_D} dV = \frac{q\alpha_H \mu_{eff} V_{DS}}{fL^2 I_D} \tag{4.12}$$

where I_D is the drain current and V_{DS} is the source-drain voltage. Pure mobility noise fluctuations have previously been reported in pMOSFETs [56] [57]. However as devices shrink, number fluctuation dominates and mobility fluctuations mostly contribute as correlated to number fluctuations which is discussed in the next section. In the devices studied in this thesis, number fluctuations and correlated number and mobility fluctuations are reported.

4.3 Correlated number and mobility fluctuations

The number fluctuation noise model has been commonly used specially for nMOSFETs and shows excellent agreements with the results. The $1/f$ noise in pMOSFETs is mostly explained by mobility fluctuations. However in some MOSFETs neither of the models shows complete agreement and deviations are observed. Therefore, a new theory was introduced to explain the fluctuations in these devices. This theory referred to correlated number and mobility fluctuation theory was suggested by Hung *et al* [58] [59] as the unified model and assumes that the fluctuations that occur due to trapping and detrapping of carriers can also affect the mobility of carriers in the channel. The drain current fluctuations can be evaluated as [60] [61]:

$$\delta I_D = \frac{\partial I_D}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{4.13}$$

$$\delta I_D = -g_m \, \delta V_{fb} + \frac{I_D}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{4.14}$$

$$\alpha = \frac{1}{\mu_{eff}^2} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \tag{4.15}$$

where g_m is the transconductance and α is defined as the mobility parameter. Applying α in the equation:

$$\delta I_D = -g_m \, \delta V_{fb} \pm \alpha I_D \mu_{eff} C_{ox} \delta V_{fb} \tag{4.16}$$

$$S_{I_D} = S_{V_{fb}} \left(1 \pm \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m}\right)^2 g_m^2 \tag{4.17}$$

The correlated number and mobility fluctuation current noise power spectral density contains two terms which the first one is related to the number fluctuation and the second term is the mobility fluctuation correlated to the number fluctuation. The positive sign is used for nMOSFETs and the negative sign is used for pMOSFETs. Different α values are reported for the correlated model [12] [61] [62]. In this thesis α values between 0.4×10^4 Vs/C [Paper V] to 1×10^4 Vs/C [Paper II] have been extracted.

4.4 1/*f* noise in high-k MOSFETs

Increased low-frequency noise is one of the substantial issues in aggressively scaled MOSFETs with high-k gate dielectric. Studies have shown that measurement of this type of noise is one of the viable tools to investigate properties of the oxide.

High-k dielectrics show higher $1/f$ noise compared to conventional SiO_2 which is mostly caused by the traps located in the high-k layer or at the high-k dielectric and channel interface.

Applying an IL of SiO_x has been shown to be inevitable in order to achieve a better oxide interface quality and better thermal stability. In these dual layer gate MOSFETs, the contribution of both layers to the LFN should be considered. LFN measurements in these devices show traps in the IL and the high-k dielectric. The thickness of this IL influences the level of $1/f$ noise remarkably. As the IL reaches very low thicknesses, the contribution of noise originated from the high-k dielectric becomes so significant that the noise from IL traps can be negligible compared to high-k dielectric traps. It is shown that there is a tradeoff between achieving very thin EOT and having a good quality interface and consequently low LFN.

The unified $1/f$ noise model was commonly used for high-k gate stacks. This model is considered for single layer gate oxides and traps that are uniformly distributed in the energy gap of the gate dielectric. However since high-k dielectrics are mostly used in multi layers, the unified model is modified to include the effect of different gate stack layers.

For a multilayer gate stack consisting of a high-k layer and an interfacial layer, traps are in both layers so the tunneling distance, the trapping time constant and the trap density should be different. If we assume equation 4.17 for the correlated number and fluctuation model, and split N_t and γ into two parts referring to the high-k and IL layer due to independent fluctuations, the new S_{Id} is:

$$S_{Id} = \frac{kTI_d^2}{fWL}\left(\frac{1}{N_{inv}} + \alpha\mu_{eff}\right)^2 \times \left[\frac{N_{tIL}(E_{fn})}{\gamma_{IL}} A + \frac{N_{tHK}(E_{fn})}{\gamma_{HK}} B\right] \tag{4.18}$$

where N_{inv} is the inversion carrier density, N_{tIL} and N_{tHK} are the oxide trap densities in the IL and high-k dielectric, γ_{IL} and γ_{HK} are the tunneling coefficients, $A=(2/\pi)\,tan^{-1}(\omega\tau_0\exp(\gamma_{IL}T_{IL}))$ and $B=(2/\pi)\,[tan^{-1}(\omega\tau_0\exp(\gamma_{HK}(T_{HK+}T_{IL}))-tan^{-1}(\omega\tau_0\exp(\gamma_{HK}T_{IL}))]$, T_{IL} and T_{HK} are the thickness of interfacial layer and high-k layer and τ_{IL} and τ_{HK} are the corresponding time constants

If the IL is thick enough, T_{IL}>~4-4.5 nm, the second term which is regarding the high-k layer becomes negligible and the equation will turn into the unified model equation with the N_t and γ of IL layer.

If the IL is very thin, T_{IL}<1 nm, then the first term which is related to the IL part becomes negligible and the equation will be the unified model for high-k.

This model is suitable for all kinds of double layer MOSFETs considering same energy levels for the traps. It was proposed by Min et al, on HfSiON nMOSFETs with SiON interfacial layer [14].

In equation 4.18 the effect of electric field on the trapping time constant is not accounted which means that the traps are considered to be uniformly distributed in energy. In order to take this into account, a more complicated model is needed. In the new model, the non-uniform trap density profile in the dielectric layers is shown by an exponentially varying function with respect to band energy and distance into the gate dielectric [16] [63]:

$$N_t(E,z) = N_{t0}exp\left[\xi(E-E_i) + q\lambda\left(\frac{V_g - V_x}{T_{ox}}\right)z + \eta z\right] \tag{4.19}$$

where

ξ: fitting parameter that defines the energy dependence of traps (eV^{-1})

E_i: intrinsic Fermi level at Si/IL (eV)

η: fitting parameter for the density of traps (cm^{-1})

V_g: applied gate potential (V)

V(x): channel potential due to horizontal field at a distance x from the source varying from 0 to V_d (drain to source bias)

Equation 4.19 should be considered for high-k and IL separately.

The modified models related to double layer high-k MOSFETs are all derived with the assumption that each trap is independent of the transactions in the other traps. Although these models are quite complicated, they can be simplified for very thin or very thick interlayers. For a double layer gate stack with 2 nm SiO_2 and 3 nm HfO_2, Nt_{IL} and Nt_{HK} have been extracted to be 1×10^{17} eV^{-1} cm^{-3} and 3.8×10^{19} eV^{-1} cm^{-3} [15].

Double layer MOSFETs have been vastly studied in this thesis [Paper II-V]. However since the interlayers are very thin ($T_{IL}\leq1$ nm), the noise is mostly from the high-k layer and IL layer can be ignored; Therefore the simple noise model have been used [Paper III-V]. In Paper II, the SiO_2 interlayer is nearly 5 nm which is too thick and it almost blocks all the noise form the high-k by preventing tunneling of carriers into the oxide. This makes the simple model still the preferred modeling choice. In order to apply the double layer models, samples are needed with an interfacial layer which is between 1 nm and 5 nm.

4.5 Gate current noise

LFN measurements usually refer to low-frequency drain-current noise measurements which is very useful in validating the gate stack quality. Moreover, it is shown that low-frequency gate-current noise measurement is also useful for investigation of the quality of gate stack in MOSFETs in terms of extracting the oxide trap density. Gate-current noise is caused by the tunneling of charges from the channel to the oxide layer and vice versa. These measurements are especially very suitable when the accuracy of the traditional techniques become questionable due to large gate tunneling current.
It is reported that thinner ILs lead to higher gate current noise. This thickness reduction of IL has also the same effect on drain current noise. IL thicknesses reported for gate current noise are below 1 nm [64] [65]. Gate current noise is more sensitive to traps close to the gate side since they can influence the carrier tunneling while these traps which are located far from the channel interface have a small effect on drain current noise. Therefore, performing gate current noise measurements together with drain current noise measurements provides complementary information about the gate stack quality. In this thesis for reliable noise measurements, the drain current is selected carefully so that the gate current is at least one order of magnitude lower in order to eliminate the effect of gate current noise. Gate current noise studies were also conducted on the devices under study, but it were severely limited by oxide reliability issues.

Chapter 5

Process details and experimental set-up

The first aim of this chapter is to give a comprehensive overview of the investigated samples. Wafers were fabricated in-house at KTH and different technologies were used, including UTB SOI devices (short channel and FinFETs) and also bulk devices with a so-called gate last flow and longer channels. The gate last flow was suitable for studies of novel Atomic Layer Deposition (ALD) schemes. The samples include reference wafers, with high quality thermal SiO_2 gates on both UTB SOI and bulk. Other samples are double layer high-k dielectrics on bulk with different high-k and IL materials and thicknesses.
The second part refers to the experimental setup for low-frequency noise measurements and on-wafer IV/CV characterization and describes the details of different measurements. The choice of suitable low-noise amplifiers for MOSFET $1/f$ noise measurements is discussed. The bias conditions, influence of gate current, fitting of spectra to $1/f$ and GR etc are exemplified and motivated.

5.1 Device Fabrication

5.2.1 UTB SOI Technology

The samples that were studied in Papers I and II were fabricated using UTB SOI technology. This allowed short channel devices, FinFETs and double layer high-k dielectrics. Two different types of studies were conducted, the first looked at influence of SB source/drain on $1/f$ noise and the other investigated the integration of $LaluO_3$ as a possible high-k dielectric for CMOS technology.
Schottky barrier FINFETs and Ultra-Thin-Body (UTB) devices were fabricated with different Ar or B dopant segregation. In Fig. 5.1, the SEM top view of the fin channel and gate is shown. The fins were formed by sidewall transfer lithography (STL) with fin dimensions, 30 nm wide and 24 nm high. The fabrication process is shown in summary in Fig. 5.2. Details of the process are described in Paper I and [66].

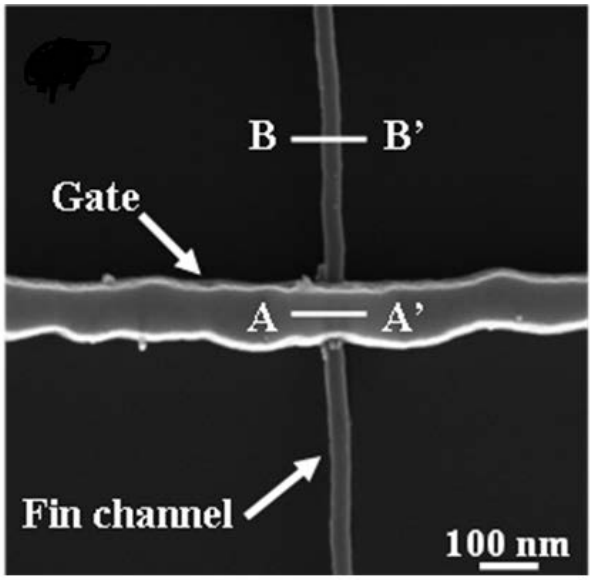


Fig. 5.1 Top view SEM of the device after defining the gate on the Fin channel [66].

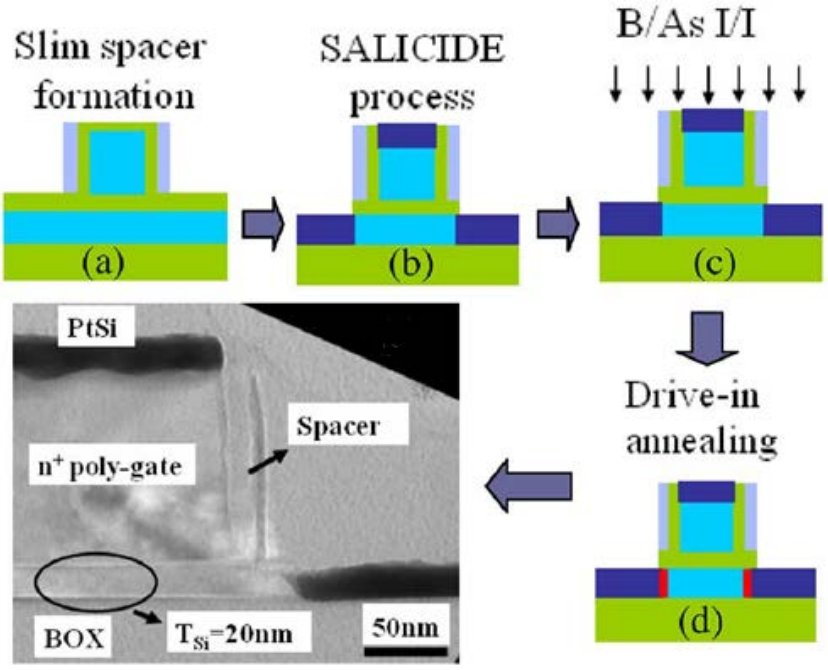


Fig. 5.2 Fabrication process of Schottky barrier [67].

The Fabrication of $LaLuO_3$ samples is similar to UTB SOI process mentioned in the previous section, the main difference lies in the gate stack formation. There are four wafers with different gate stack compositions. High-k dielectrics were deposited by Molecular Beam Epitaxy (MBE). The first wafer referred to the reference wafer has a 5 nm SiO_2 dielectric and no high-k. In the other wafer, high-k1, a 6 nm $LaLuO_3$ is deposited on top of the SiO_2. The next two wafers,

high-k2 and high-k3 have only a high-k $LaLuO_3$ dielectric with 6 nm and 20 nm thicknesses respectively with no interfacial layer. The cross section of these gate stacks is shown in Fig. 5.3.
The samples are designed with different thicknesses which is very interesting from a low-frequency noise point of view. This is investigated in Chapter 6 showing the influence of the interfacial layer and different thicknesses of high-k material in the resulting low-frequency noise.
TiN metal gates were deposited by sputtering on all the samples. Further fabrication details are explained in Paper II.

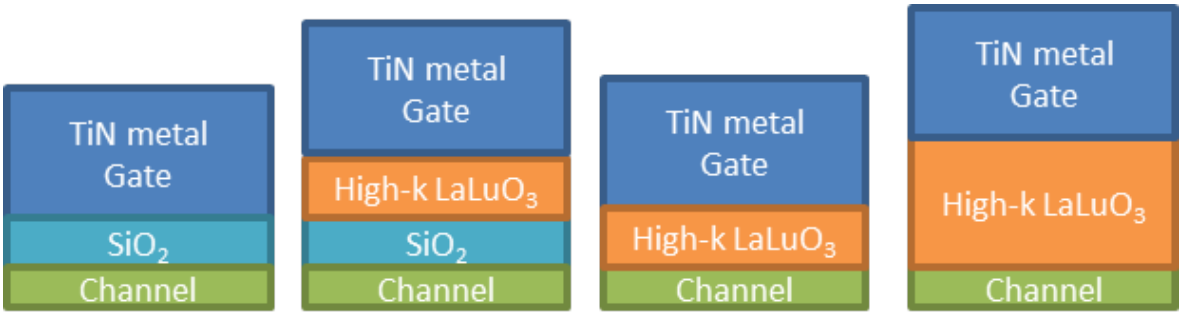


Fig. 5.3 Gate stack schematic of Reference, high-k1, high-k2 and high-k3 (not to scale).

5.2.2 Bulk Si gate last technology

The remaining samples studied in this thesis (Papers III, IV and V) were bulk silicon wafers. The fabrication method was changed from gate first to gate last. The gate last process is beneficial in providing better quality high-k gate stacks by limiting the thermal budget. The main drawback is that only rather long channel devices (~3 µm) could be fabricated.
The first group is double layer gate dielectrics with chemical SiO_x interlayer with an HfO_2 high-k dielectric. In these devices the IL layers were fabricated in situ in the ALD using different oxidizing agents. Ozone and water have been used as oxidizing agents in first and second wafer. In the other wafer a pulsed sequence is applied with Argon purge. Depositing the IL in the ALD can provide very thin and uniform layers. Since the high-k deposition is performed in the same ALD, the wafer would not be exposed to air and will get less contaminated. A Reference wafer with an exsitu SiO_2 IL was also used for comparison.
These samples all differ in the IL thickness. A 3.5 nm HfO_2 high-k was deposited on all wafers. The fabrication process in detail is described in [68]. A cross section of these gate stacks is shown in Fig. 5.4. The samples are studied from low-frequency noise point of view in Chapter 6.

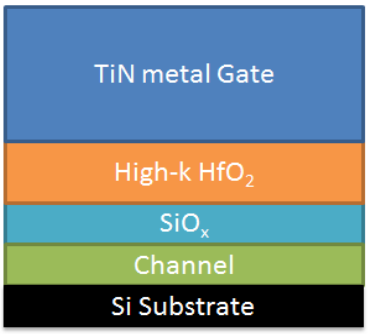


Fig. 5.4. Gate stack schematic. 3.5 nm HfO_2 layer, different SiO_x IL from 0.4 nm to 1 nm.

In the last two Papers, TmSiO as a new interlayer was introduced as a candidate to replace the conventional SiO_2. This novel non-silicon dioxide dielectric is fabricated through RTA of Tm_2O_3 that was deposited in ALD. The annealing process forms a TmSiO layer. The thickness of this layer depends on the degree and duration of annealing. In the samples under study the thickness of TmSiO was 0.9nm which corresponds to an EOT of 0.3 nm. This has been achieved through RTA at 550 °C in N_2. The unreacted 3.5 nm (0.9 nm EOT) Tm_2O_3 is used as a high-k dielectric. For the other set of samples, the Tm_2O_3 layer was selectively etched in H_2SO_4 and 2 nm HfO_2 deposited in ALD. The fabrication process is described in detail in [34] [35] [69] [70]. The total EOT was 1.2 nm for $TmSiO/Tm_2O_3$ gate stack and 0.65 nm for $TmSiO/HfO_2$ gate stack. The gate stack cross sections are shown in Fig. 5. 5.

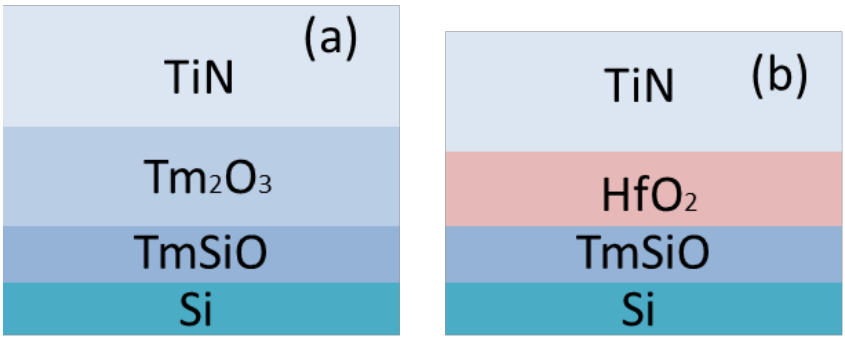


Fig 5.5 Gate stack schematic of $TmSiO/Tm_2O_3$ (a) and $TmSiO/HfO_2$ (b).

An overview of all double layer high-k samples is found in Table 5.2, containing the high-k and IL materials and thicknesses, IL and total EOTs, the substrate material and fabrication methods used. The thinnest IL EOT is 0.3 nm (Physical thickness: 0.9 nm) which refers to TmSiO interlayer. The thinnest total EOT is around 0.65 nm in the gate stack using the same TmSiO interlayer with HfO_2 as high-k dielectric. The high-k 2 wafer with $LaLuO_3$ high-k and no interfacial layer corresponds to a total EOT 0f 0.8 nm which is the next lowest total EOT. The equivalent EOT is calculated through equation 5.1. Other thin interlayers (T_{IL}<0.5 nm) are silicon-dioxide layers fabricated insitu in the ALD equipment.

$$EOT = t_{high-k}\left(\frac{K_{SiO_2}}{K_{high-k}}\right) \quad (5.1)$$

Table 5.2. Overview of all double layer high-k samples in this thesis.

samples	High-k material	High-k thickness (nm)	IL material	IL thickness (nm)	Total EOT (nm)	Fabrication method	Substrate material
High-k 1	$LaLuO_3$	6	SiO_2	5	5.8	Gate first	SOI
High-k 2	$LaLuO_3$	6	-	-	0.8	Gate first	SOI
High-k 3	$LaLuO_3$	20	-	-	2.6	Gate first	SOI
Etch back	HfO_2	3.5	SiO_x	1	1.7	Gate Last	Bulk Si
H_2O	HfO_2	3.5	SiO_x	0.5	1.2	Gate last	Bulk Si
Pulsed	HfO_2	3.5	SiO_x	0.45	1.15	Gate last	Bulk Si
O_3	HfO_2	3.5	SiO_x	0.4	1.1	Gate last	Bulk Si
$TmSiO/Tm_2O_3$	Tm_2O_3	3	TmSiO	0.9 (0.3 EOT)	1.2	Gate last	Bulk Si
$TmSiO/HfO_2$	HfO_2	2.5	TmSiO	0.9 (0.3 EOT)	0.65	Gate last	Bulk Si

5.2 Measurement set-up

5.2.1 IV measurements

For a proper noise measurement, in the first step, an IV measurement is required in order to evaluate the device performance. Through IV measurements, the threshold voltage (V_t), transconductance ($g_m=\partial I_D/\partial V_{GS}$), subthreshold slope and the leakage current will be obtained. It should be noted that leakage current refers to the gate current that is expected to be quite high since we are dealing with very low EOTs. It is very important that the devices which are selected for noise measurements have low enough leakage current so that the drain current noise is monitored during measurements. The selected devices all have a leakage current which is at least 10^3 times lower than the drain current. The IV measurements were carried out with a cascade microtech probe station with shielded

microchamber and temperature controlled chuck connected to a Keithley parameter analyzer. A typical IV plot is shown in fig. 5.6 for both nMOSFETs and pMOSFETs on $TmSiO/Tm_2O_3$ samples. The plot shows symmetric drain currents and source currents. The gate current is low enough in this gate voltage range in order to measure $1/f$ noise. The subthreshold slope is around 70 mV/dec.

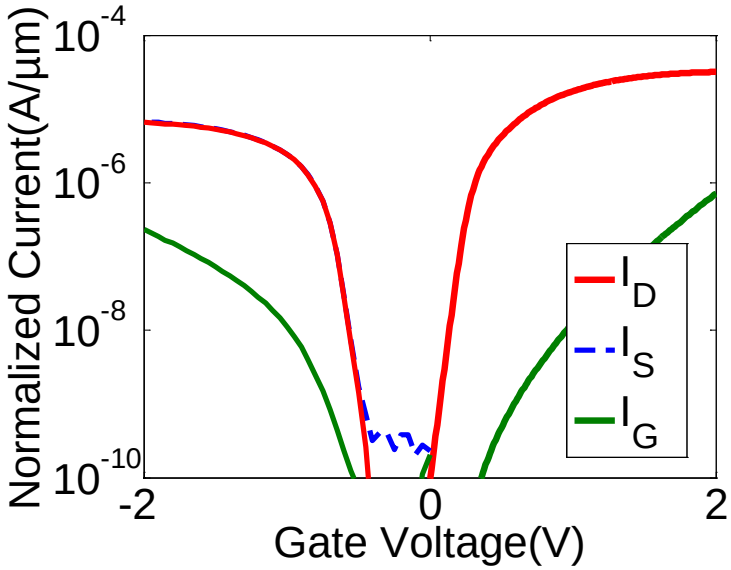


Fig 5.6. Normalized current versus gate voltage for nMOSFETs and pMOSFETs W×L=10×3 μm²

5.2.2 CV measurements

CV measurements were also performed on devices under study. By measuring the oxide capacitance, the thickness of the oxide dielectric was extracted. This capacitance is the gate-bulk capacitance ($C_{gb)}$ which was measured with an HP 4284A CV meter. By performing this measurement the EOT can be extracted through fitting the measured gate-to-bulk CV curves using the CVC fitting tool [71]. The gate-channel capacitance (C_{gc}) which is also shown in Fig. 5.7 is used to find inversion charge in the mobility extractions.

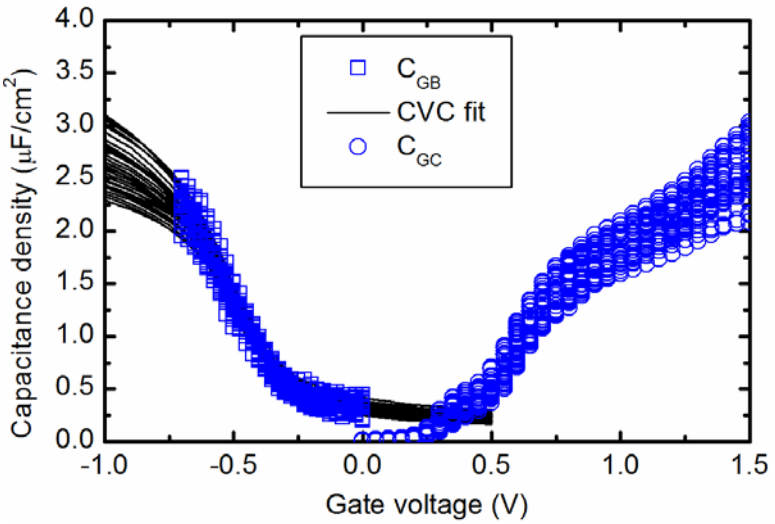


Fig. 5.7. C_{GB} and C_{GC} curves for nMOSFETs and CVC fitting of the C_{GB} data [69].

5.2.3 Noise measurements

The measurement of low-frequency noise is very sensitive, since the measured noise power is low. These measurements could be affected by the undesired disturbances from other electronic devices in the lab, the light and RF/microwave signals. Therefore the set-up should be designed carefully and proper shielding should also be used.
The measurements were performed by placing the wafer in a shielded cascade probe station connected by Triax/BNC cables to a low noise amplifier with biasing voltage. This low noise amplifier is needed in order to amplify the device noise. This amplifier is connected to the spectrum analyzer to measure the power spectral density. The amplifier and spectrum analyzer add noise to the measurements. This noise sets a limit to the measurable device noise. Therefore amplifiers with ultra-low input noise should be selected. The collected noise data is then transferred to a PC for further analysis.
Two amplifiers were used for measurements in this thesis. The first set up includes a Femto DLCPA-200 low-noise current (transimpedence) amplifier which is biased with a battery powered network used in Paper I. The other setup contains a programmable biasing amplifier (PBA) and a low-noise power supply by Synerigie concept used for measurements in Papers II to V. The noise set-up for the second amplifier is shown in Fig 5.8.
The gain of the amplifiers can be adjusted for each measurement. For devices with lower noise level a higher gain setting is used so that the noise level will be distinguished from the noise floor. The noise floor refers to the level of background noise in the system which is always present even if the device is not biased. In order to select the proper gain, different gain settings were examined. For the devices under study, amplifier gains of 10^{-4} to 10^{-6} (A/V) have been used. The performance depending on gain setting taken from the data sheet of both amplifiers is shown in Table 5.3. The equivalent input noise current defines the limit of the lowest current noise that can be measured reliably. The requirements for a proper amplifier for this type of measurements are variable gain, ultra-low input noise and sufficient frequency range (up to 10^5 Hz is used in these measurements).

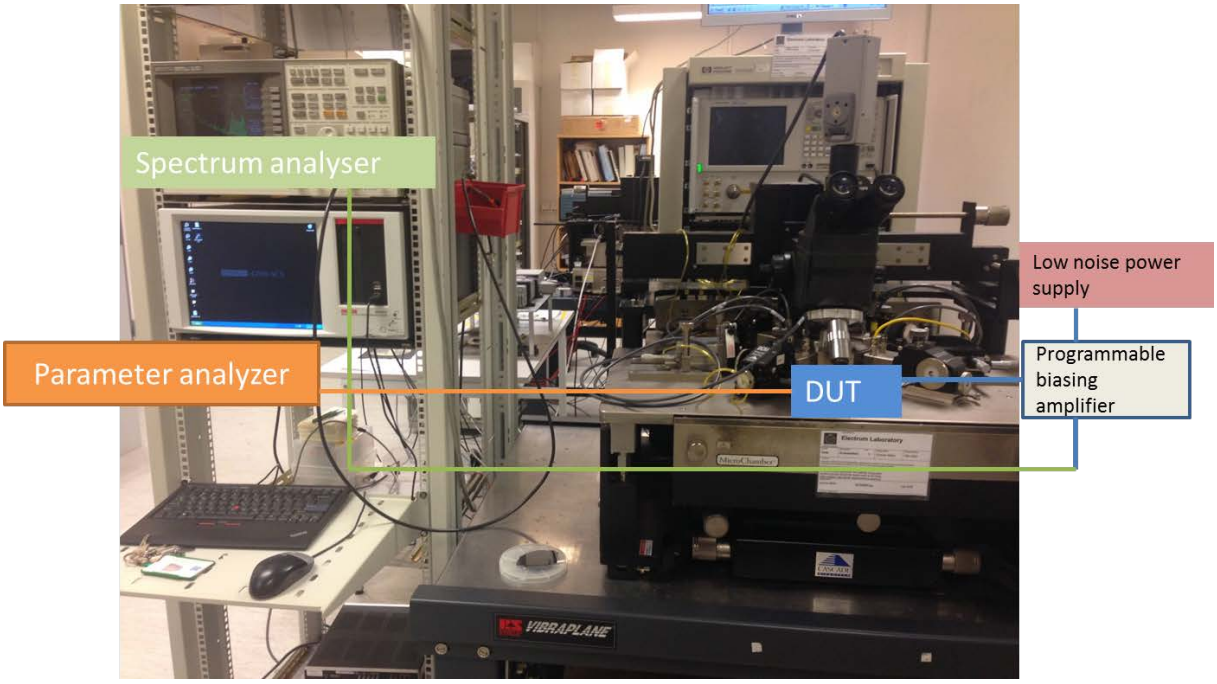


Fig. 5.8. Noise measurement set-up.

Table 5.3. Performance depending on gain setting derived from Femto DLCPA-200 and PBA2 data sheets.

Gain (V/A)	10^3		10^4		10^5		10^6		10^7	
Amplifier	Femto	PBA	Femto	PBA	Femto	PBA	Femto	PBA	Femto	PBA
Equivalent input noise current (/$Hz^{1/2}$)	20 pA	200 pA	2.3 pA	98.2 pA	460 fA	10.1 pA	130 fA	1.1 pA	43 fA	168 fA
Upper cut-off frequency	500 kHz	500 kHz	500 kHz	480 kHz	400 kHz	510 kHz	200 kHz	290 kHz	45 kHz	138 kHz
Max biasing current	10 mA	10 mA	1 mA	10 mA	0.1 mA	1 mA	10 µA	100 µA	1 µA	10 µA

Using the power supply, the MOSFETs can be measured at different gate and drain bias voltages. Most of the measurements are performed in the linear region of operation with low drain-source voltage. Some measurements have also been carried out in the saturation region at V_{DS}=1 V. In Fig 5.9, the programmable biasing amplifier is shown together with the power supply. The connections to the device are also indicated with arrows to the drain, gate and the spectrum analyzer. A software program comes together with the PBA and power supply called NoisysSimple which sets the gain of the amplifier and the drain and gate bias.

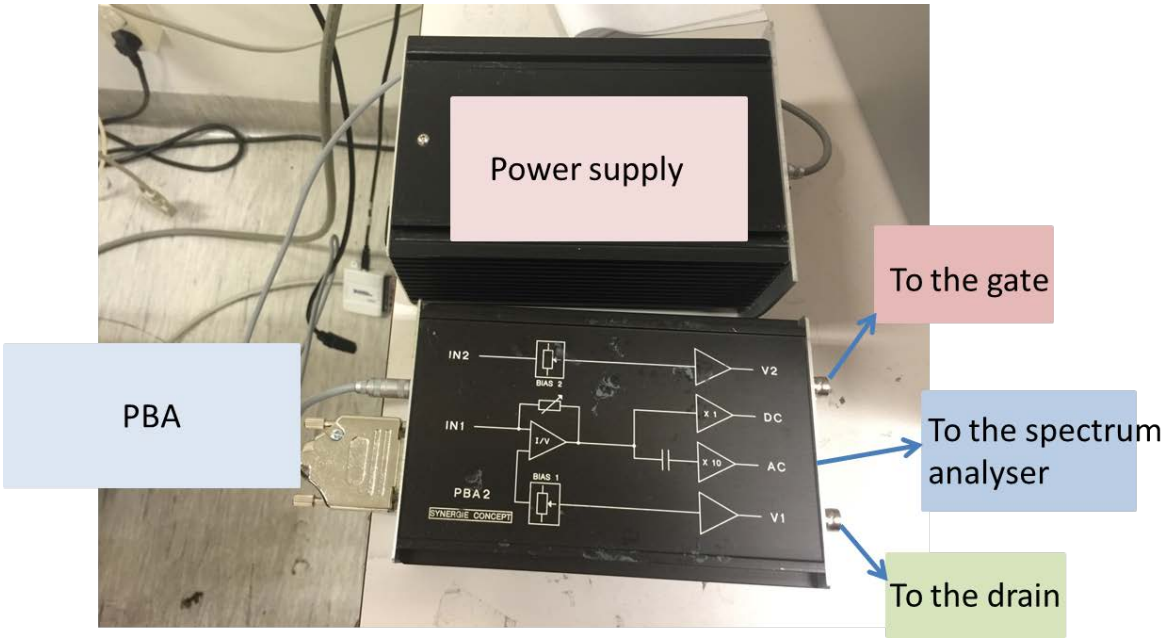


Fig. 5.9. Programmable biasing amplifier (PBA) and power supply.

The spectrum analyzer is controlled through a LabVIEW program where the user can specify the settings of the spectrum analyzer such as frequency span, range and number of averages taken. The spectrum analyzer takes averages to perform these measurements. Therefore noise measurements are usually slow and each measurement takes around 1-2 minutes depending on the number of averages taken and the gate bias range. During noise measurements, the device was normally biased for few minutes to measure a larger frequency range. In some devices this caused degradation in the gate oxide leading to device damage. Therefore IV measurements were performed both before and after measurements to monitor the gate current. The damaged devices were excluded from the study. For other devices included in the study, a small shift in the threshold voltage was observed normally. The shift could even appear after simple IV measurements. Therefore the noise level can slightly vary with each measurement.

In order to increase the resolution, the frequency regions are split into small regions of one/two decades of frequency. The final power spectral density is shown for a typical device in Fig 5.10. The depicted power spectral density by the spectrum analyzer is in dBm which shows the noise of the device including the amplifier gain. To calculate the noise of the device itself, that power is converted to Watt and divided by the square of gain. This figure is shown for different gate voltage overdrives at a constant drain voltage of 50 mV. It is shown that the noise level depends on the gate bias and increases with increasing the gate voltage. The 50 Hz peak is also visible in the plot together with the harmonics. For each bias point (gate voltage setting), a line with the form of $1/f$ is fitted to the measurement curve. Then the data is taken at f=10 Hz for further analysis and comparisons. For some devices showing GR noise, this noise is also fitted. The fitting have been performed manually with a few trials. For devices showing GR noise, equation 3.3 was fitted on top of $1/f$ noise. Using this fitting, the corner frequency has also been calculated. Corner frequency refers to the frequency peak which is used for the time constant extraction. Using the fitting line, the problem of 50 Hz peak and its

harmonics can be solved. An example of fitting is depicted in Fig 5.11 for $1/f$ noise and white noise and in Fig 5.12 for GR noise, $1/f$ noise and white noise. In Fig. 5.12, the quantity of the y-axis represents f*S_{id} which is plotted over the frequency. The peak of the curve represents the corner frequency.

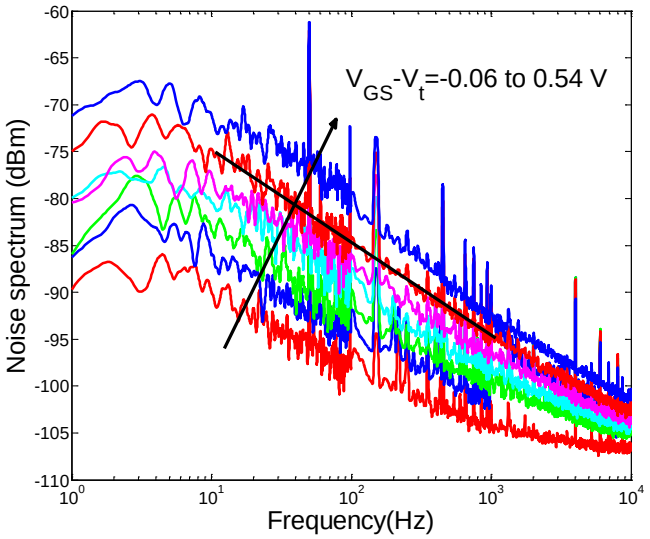


Fig 5.10. Typical drain current noise power spectral density (PSD) for nMOSFET with W×L=10×3 µm².[Paper III]

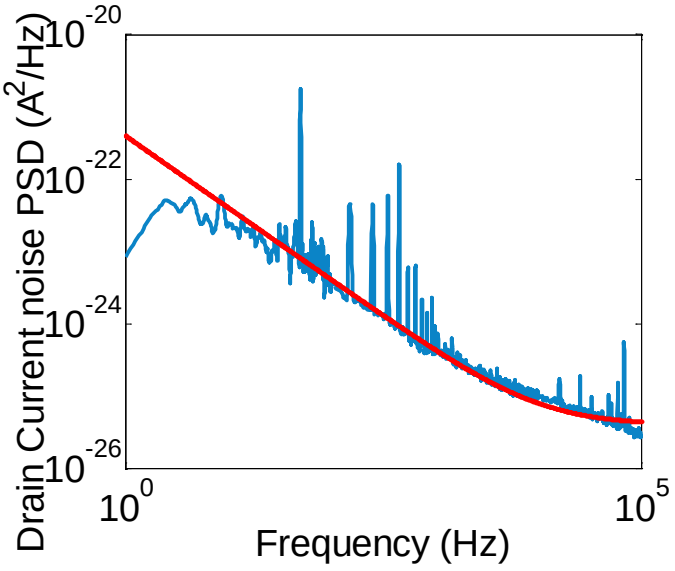


Fig 5.11. Fitting $1/f$ and white noise to a typical measurement plot.

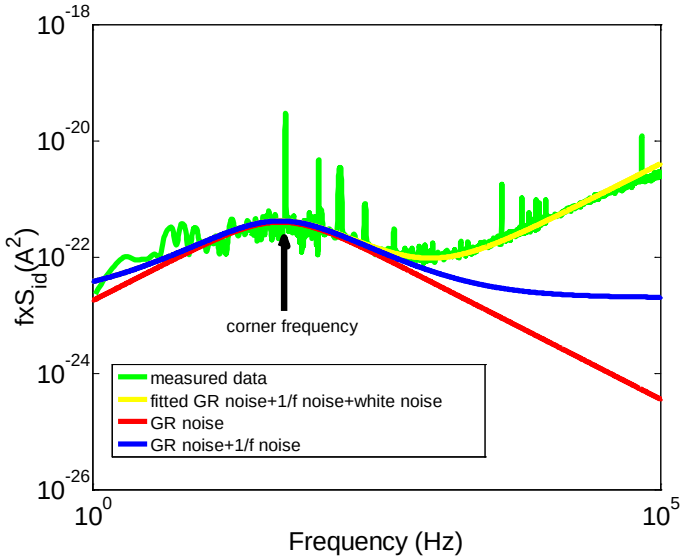


Fig 5.12. Fitting GR, $1/f$ and white noise to a typical measurement plot.

Chapter 6

Noise results and discussion

In this chapter, the low-frequency noise performance of different MOSFETs is summarized. The first group of devices is Schottky barrier nMOSFETs and pMOSFETs and n-type FinFETs. The major part of the devices is double layer high-k MOSFETs with different IL and high-k dielectrics. These devices include novel MOSFETs with high-k IL (TmSiO) with ultra-low EOT, very thin chemical SiO_2 IL and $LaLuO_3$ MOSFETs with no IL. The chapter contains the measurement results, modeling of the noise measurements followed by analysis of the results and discussion. The oxide trap density is an important metric that gives information in this study. The actual slope of $1/f$ noise spectrum and normalized current noise values taken at specific frequencies are also other important metrics. For each noise spectrum $1/f^{\gamma}$ was carefully calculated through curve-fitting at low frequency. In most devices γ was between 0.8 to 1.2, in few devices γ was found to be between 1.5 and 2 which shows the occurrence of GR noise. This is studied in detail in Section 6.3. Several devices have been measured on each sample so it was possible to calculate an average of measurements which was typically based on 5-6 devices.

6.1 Short channel device Schottky barriers (Paper I)

Schottky barrier source/drain is a promising solution for low-resistive contacts in CMOS technology. However, more noise is generated in SB MOSFETs compared to conventional MOSFETs due to formation of the metallic source-drain. The barrier height has a significant effect on IV characteristics and measured low frequency noise. Previous studies on SB MOSFETs reported high NiSi and PtSi electron barriers [72] [73]. Dopant segregation can be used as an effective method to reduce the barrier height [74]. PtSi Schottky barrier MOSFETs were implanted with As or B in order to lower the barrier height. The study includes nMOS and pMOS and nMOS FinFETs. In Table 6.1, it is shown that the barrier height has been lowered with dopant segregation [66]. Comparing this PtSi Schottky barrier with other Schottky barriers such as NiSi shows that the barrier height for holes is

lower for PtSi which gets even lower after dopant segregation. The barrier height for electrons has been shown to be high for both NiSi and PtSi Schottky barriers from previous studies [41] [72]. This has been reduced significantly for PtSi samples with dopant segregation.

Table 6.1 Barrier heights with and without dopant segragation.

	p-type barrier height φ_{Bp} (eV)	n-type barrier height φ_{Bn} (eV)
Before dopant segragation	0.2	0.88
After dopant segragation	0.1	0.2
NiSi [72]		0.64
PtSi [72]		0.93
NiSi SB [41]	0.45	

Noise measurements were carried out on both UTB and FinFETs. N-channel devices with high barrier were difficult to measure due to very low drain current. P-channel UTB devices with Boron implantation were compared to UTB devices with no dopant segregation. The IV measurements in Fig 6.1 show that the on-current is limited by the Schottky-barrier. The measurements were performed in both forward and reverse direction. A slight asymmetry can be observed in the forward and reverse on-current which is related to the position of PtSi to the channel interface.

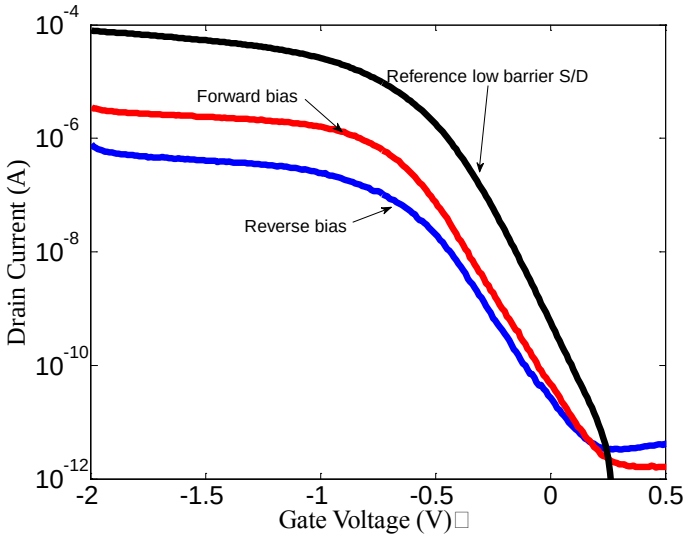


Fig. 6.1. IV characteristics of p-channel UTB devices with W=25 µm and L=90 nm with dopant segregation at forward and reverse bias shown with circles. P-channel UTBs with W=6 µm and L=90 nm with B implantation shown with square symbols [Paper I].

Low-frequency noise measurements were performed on UTBs with W=6 µm and L=90 nm. The measurements show a $1/f^{\gamma}$ slope with γ close to 1. The normalized drain current noise versus the drain current is shown in Fig. 6.2. The plot shows that the noise level is reduced for low barrier device with dopant segregation for

both n-type and p-type devices. The increased noise at higher drain currents for the pmos low barrier is a result of high series resistance or additional gate current noise in low EOT devices. A slight variation is seen in the normalized noise of the forward and the reverse configuration in a p-channel UTB FET.
Low-frequency noise has also been measured on n-type SB FinFETs. Previous work has been published on SB FinFETs [75] [76] but no noise study was reported to the best of author's knowledge. The measurements show a higher noise level for FinFETs compared to UTBs which is related to the special gate structure of these devices. The small gate area and traps in the sidewall gate oxide were found to be the main noise source in FinFETs [77].
In future work this can be improved by optimizing the interface composition. Further work on Schottky-barriers can include improvements in SB contacts in order to reduce the difference between reverse and forward bias. Temperature noise measurements can also be a possible future work. The high barrier devices with very low current can be measured at elevated temperatures since it will lower the barrier and increase the current. Finally, NiPtSi Schottky barriers have shown extremely low contact resistance and therefore low barrier [78]. A comprehensive low-frequency noise analysis on such devices could give useful information about the quality of these barriers.

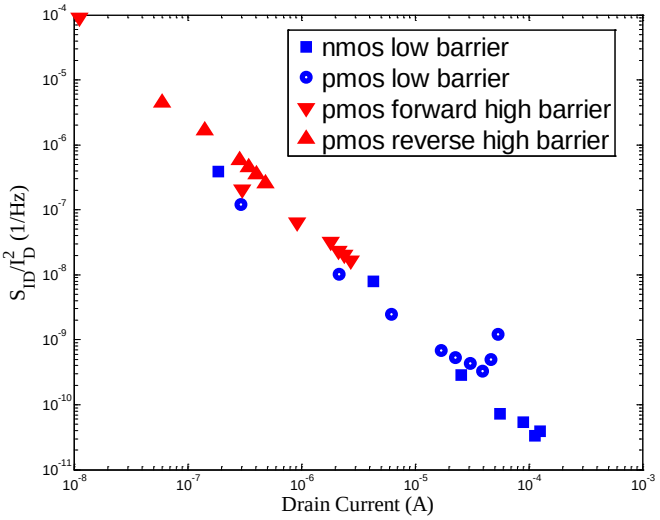


Fig. 6.2. Normalized low-frequency noise versus current for low barrier n-channel UTB FET with L= 0.5 µm and W=10 µm (shown with square symbols) and p-channel UTB FETs with L= 90 nm and W=25 µm at forward and reverse bias (shown with triangle symbols) and low barrier p-channel with L=90 nm and W=6 µm (shown with circles) at V_{DS}= 50 mV and f=10 Hz.

6.2 Double layer high-k gate stacks

The MOSFETs under study in this part are advanced gate stacks which mostly contain double layer dielectrics with a high-k and an interfacial layer. $LaLuO_3$ is introduced as a new high-k dielectric. This dielectric is implemented with no interfacial layer on silicon. In the next section chemically fabricated silicon dioxide interlayers are studied. These oxides are fabricated layer by layer in the ALD

which result in very thin and uniform interlayers. TmSiO as a novel high-k interlayer is implemented allowing low EOT with higher physical thickness. This IL is used together with Tm_2O_3 and HfO_2 high-k dielectrics. Different IV, CV and noise measurements have been performed on these devices which are summarized below.

6.2.1 $LaLuO_3$ high-k MOSFETs (Paper II)

Hafnium based MOSFETs with an SiO_2 interfacial layer have been commonly used in CMOS technology. However since further scaling became challenging, the possibility of integrating new high-k materials or high-k dielectrics with no interfacial layer has been investigated. Previously it has been shown that La-alminate has been directly fabricated on Si with no IL [79]. In this study a new high-k dielectric ($LaLuO_3$) with no IL is studied. $LaLuO_3$ with an optical bandgap of 5.2 eV and symmetrical 2.1 eV conduction and valence band offset to Si is implemented as a higher-k dielectric with k~30. The high-k value of this dielectric together with no IL leads to very scaled EOT of 0.8 nm. The thermodynamic stability is reported to be around 1000°C which can be an advantage in the gate-first process [80] [81].
In this study low-frequency noise analysis has been carried out in order to examine the quality of this promising oxide. Different gate stack configurations with $LaLuO_3$ as high-k and SiO_2 as interfacial layer and samples with no interfacial layer have been investigated which have been described in detail in section 5.2.2. A reference wafer is also used with only SiO_2 as dielectric which is very useful for comparisons. These devices follow the same SOI technology with SB as used in Paper I.
Channel mobility is measured through drain conductance method and N_{inv} is obtained from the split-CV measurements. Large area devices (W=50 µm and L=3 µm) were selected for mobility measurements. The extracted mobility versus inversion charge density is shown in Fig 6.3. As shown in the figure, when the $LaLuO_3$ layer is placed on top of the Si, the mobility degrades for high-k 2 and high-k 3 due to increased number of traps and further Coulomb scattering in the high-k dielectric. The mobility measurement on different devices on high-k 1 shows some variation in the effective mobility.

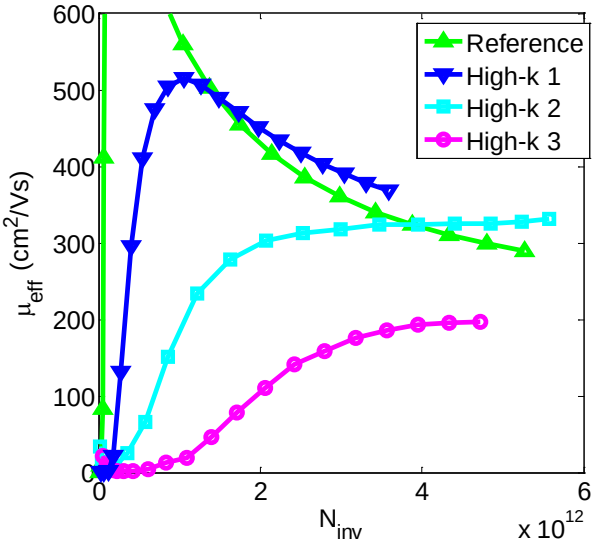


Fig 6.3. mobility versus inversion charge density.

The low-frequency noise measurements were performed using a programmable biasing amplifier (PBA) with an external low noise power supply shown in section 5.2.3. The measured devices have 0.35 µm, 0.5 µm and 1 µm gate lengths and 10 µm and 50 µm gate widths. The transistors were measured at different gate voltages from subthreshold to strong inversion and two different drain voltages (V_{DS}=50 mV and V_{DS}=1 V). The power spectral density of a typical nMOSFET measured at three different gate voltage overdrives in the frequency range between 1 Hz and 100 Hz is shown in fig 6.4. The plot shows that the drain current noise increases with increasing gate voltage. The low frequency noise at each gate voltage overdrive level shows a slope of $1/f$.

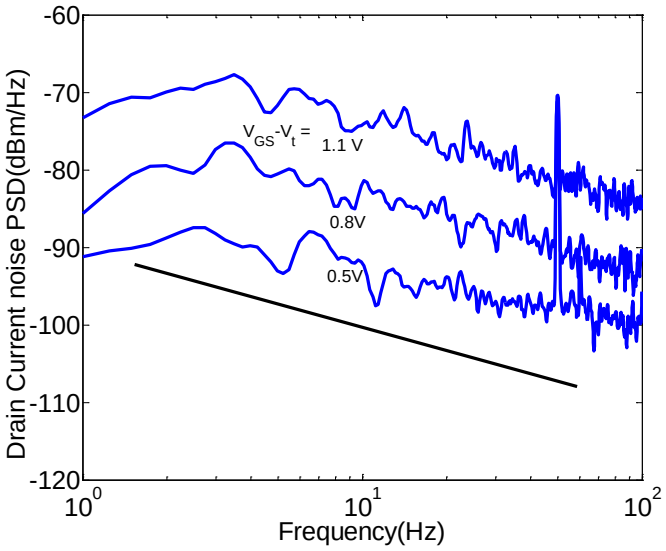


Fig 6.4. Drain current noise PSD for nMOSFET W=10 µm and L=0.5 µm for three different gate voltages.

Different devices with the same geometries have been measured on all four samples to confirm the reproducibility of the measurements. The noise level for different geometries has also been investigated. This is shown in Fig. 6.5 representing different area devices on the highk-1 sample. The legend of the figure refers to the width and length of the devices respectively. Both W and L were varied to obtain different geometries. The figure shows higher noise level for smaller gate area devices measured at lower V_{DS} which is confirmed by the noise equation 6.1.

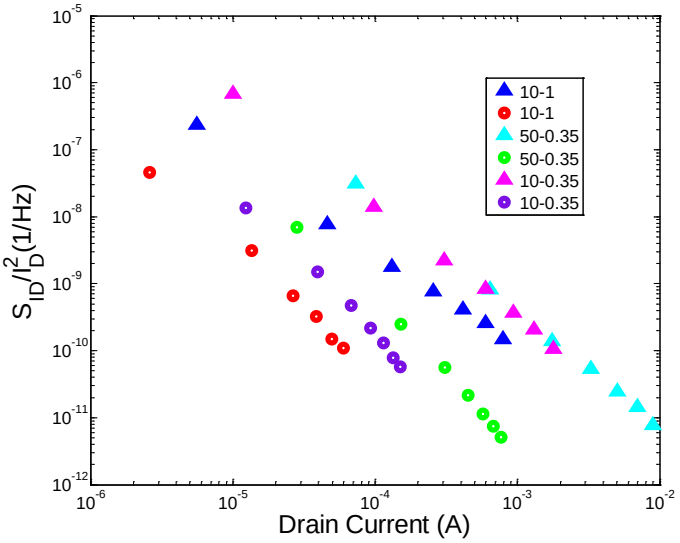


Fig 6.5. Normalized drain current noise versus drain current for different gate dimension on high-k 1 wafer taken at V_{DS}= 50 mV(circle symbols) and V_{DS}= 1V (triangle symbols) and *f*=10 Hz.

The normalized drain current noise versus drain current plots for all three samples were compared to $(g_m/I_D)^2$ and $1/I_D$ to fit a proper model to the measurements. The close agreement between the results and $(g_m/I_D)^2$ suggests the correlated number and mobility fluctuation model for these samples. In this model it is assumed that the charged traps cause fluctuations in the mobility. N_t and α were extracted for these four samples according to equation 6.1.

$$\frac{S_{ID}}{I_D^2} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f^{\gamma}} \frac{g_m^2}{I_D^2} \left(1 + \frac{\alpha\mu_{eff} C_{ox} I_D}{g_m}\right)^2 \qquad (6.1)$$

The calculated N_t is 1×10^{17}, 2×10^{17}, 2×10^{18} and 2×10^{18} eV^{-1} cm^{-3} for the reference, high-k 1, high-k 2 and high-k 3 respectively. The extracted mobility parameter α is 1×10^4 Vs/C. As expected the effective trap density is higher for the high-k wafers which is related to higher number of traps in the high-k dielectric. However it should be noted that in these samples the high-k is implemented without any interfacial layer. Previous studies on implementation of new high-k dielectrics such as ZrO_2 added HfO_2 and La_2O_3-HfO_2 MOSFETs has reported N_t values of $8.9x10^{18}$ to $2x10^{20}$ [17] [39]. In high-k 1, the high-k dielectric is separated from the silicon substrate with an interfacial layer of 5 nm SiO_2. This interfacial layer has effectively blocked the noise from the high-k and N_t has been reduced an order of magnitude. Since these samples have the same Schottky barrier technology as

Paper I, the oxide trap density results confirm that the Schottky barrier does not add any extra noise to the MOSFET.

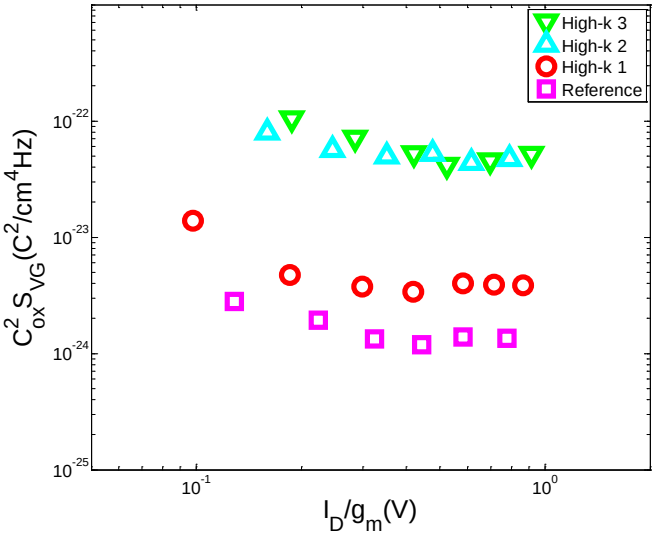


Fig 6.6. Normalized input gate voltage noise versus I_D/g_m taken from nMOSFETs with W=10 µm, L=1 µm from all four samples.

In Fig 6.6, the input referred gate voltage noise which is normalized to the oxide capacitance is depicted versus I_D/g_m.
The reference wafer without any high-k shows lower noise. High-k 2 and high-k 3 show the highest noise resulted from the traps in the high-k. For high-k 1, the SiO_2 interfacial layer has blocked the noise from the high-k layer and decreased the noise level significantly. However the SiO_2 IL used is rather thick to be used and results in high total EOT. For a proper comparison to state-of-the-art hafnium-based gate stacks, samples with $LaLuO_3$ high-k dielectric are needed with a thin enough SiO_2 interlayer. Yet the noise level of the high-k 2 and high-k 3 samples are shown to be an order of magnitude higher. This is comparable to HfO_2 samples, showing that this higher-k dielectric can be a possible candidate for future CMOS technology.
In order to complete the study, samples with different IL thicknesses are needed, such as samples with IL< 1 nm and 1 nm<IL<2 nm. Studies on these samples according to the modeling discussion in section 4.4, will give information on noise contribution from both the IL and high-k layer.

6.2.2 Chemical oxide SiO_x (Paper III)

In advanced gate stacks with a high-k layer, the implementation of an interfacial layer is necessary for a better interface quality. The thickness of this IL has a significant effect on the low-frequency noise level. SiO_2 have been widely used as an IL layer. This oxide can be fabricated both using thermal and chemical

methods. In an exsitu thermal method, the oxide layer is grown thermally and etched back to the desired thickness. This method was commonly used for fabrication of IL SiO_2. However in order to achieve a thin SiO_2 layer, this method can no longer be used and chemical methods are needed. SiO_2 interlayers which were fabricated using ozone based chemical methods have been reported previously [9] [10] . In this study, the IL is fabricated insitu, in the same Atomic Layer Deposition (ALD) as the high-k layer. Deposition at low temperature in ALD allows thin and uniform IL layers. Since the deposition of high-k is performed in the same ALD, the wafer will not be exposed to air leading to less contamination compared to exsitu methods.

In this study, four wafers are investigated with high-k HfO_2 layer and SiO_x interfacial layer with different thicknesses. The details are explained in section 5.2.3.

The low-frequency noise measurements were performed on nMOSFETs with L=3 µm, L=10 µm and W=10 µm. The gate voltage is ranged from 0.6 V to 1.2 V at a fixed drain voltage V_{DS}= 50 mV.

DC measurements using parameter analyzer defines DC properties such as gate leakage, transconductance (g_m) and threshold voltage (V_t) as shown in Chapter 5. Reasonable I_D-V_G curves were obtained for all samples. Even though the insitu samples have higher gate current, the gate voltage was limited for noise measurements to include the drain current regions which are an order of magnitude higher than the gate current. In Fig. 6.7, the gate current density versus gate voltage is depicted for all four samples. The insitu samples show higher gate current leakage which is a result of their very thin SiO_x interlayer.

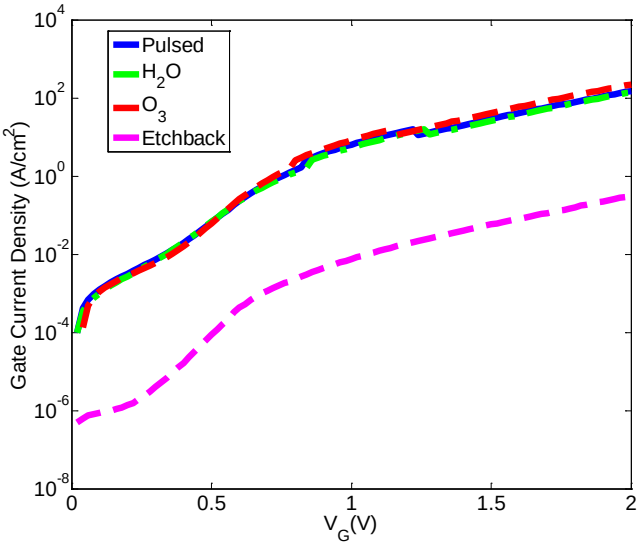


Fig 6.7. Gate current density versus gate voltage on nMOSFETs with W×L=10×3 µm² and V_{DS}=50 mV.

Noise measurements on these devices show $1/f^{\gamma}$ dependence for all samples with γ close to 1. The noise spectrum of an nMOSFET on pulsed wafer with W=10 µm and L=3 µm in the linear region has been shown in Chapter 5, Fig 5.8.

To compare the four samples, the effective density of traps has been extracted using the following equation which is derived from equation 4.7:

$$N_t = \frac{S_{id}(V_{GS} - V_t)^2 \lambda C_{EOT}^2 WLf}{q^2 kTI_D^2} \quad (6.2)$$

In this equation, g_m is assumed to be $I_D/ (V_{GS}-V_t)$ and $\lambda=0.5\times10^8$ cm^{-1} for HfO_2. This equation is different from equation 6.1, as it contains only the number fluctuation part.
The trap density increases as the interfacial layer decreases. The extracted N_t values are 7×10^{18}, 1×10^{19}, 2×10^{19} and 4.8×10^{19} eV^{-1} cm^{-3} for etchback, H_2O, pulsed and O_3 wafers respectively. Insitu wafers show higher N_t values due to thinner IL or likely different quality HfO_2. However the extracted N_t values are lower than other ozone based chemical method exsitu fabricated interfacial layers [9] [82]. This is shown in Fig 6.8 which shows N_t versus the inverse of IL which compares the trap density values for different interfacial layer thicknesses. The data shown with a square refers to an ozone based exsitu fabricated SiO_2 with 0.8 nm thickness which is taken from a similar study at IMEC. The comparison shows that N_t values of devices with even thinner insitu SiO_x are lower than the chemical exsitu N_t. It is worth noting that using this insitu method, very thin and uniform interlayers can be fabricated which is very challenging to achieve using exsitu methods.

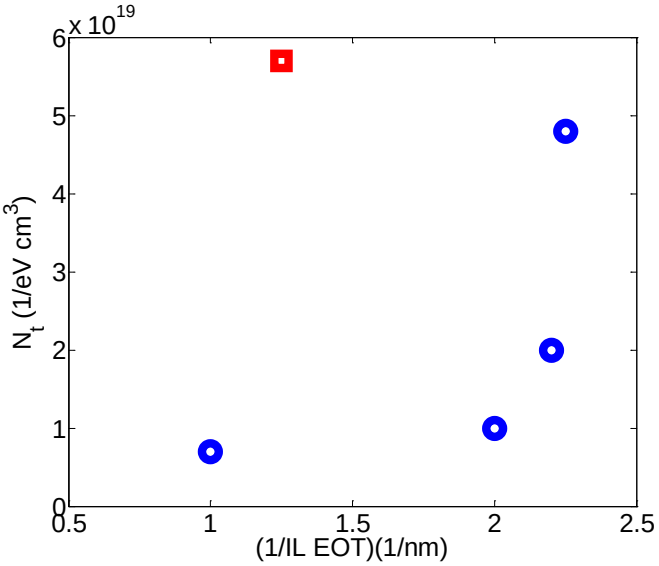


Fig 6.8. Effective trap density extracted at *f*=10 Hz versus the inverse of IL thickness for the samples under study (circle symbols) and the exsitu chemical oxide [9] (square symbol).

6.2.3 Thulium silicate high-k interfacial layer (Paper VI & V)

The implementation of interfacial layer in high-k gate stacks provides good quality interface. However, according to scaling trends the IL should be scaled below 0.5

nm which is challenging. Therefore, high-k ILs such as silicates are introduced to enable scaled EOT. Previously lanthamun silicate had been studied as an interlayer with La_2O_3 high-k dielectric [33] [83]. These devices showed low EOT and low interface state density. Yet the process is challenging since La_2O_3 seems to react with Si and H_2O. Therefore the process should be controlled strictly by using special annealing conditions to achieve scaled EOT. Due to these limitations the lanthamun silicate interlayer is applicable only in La-based dielectrics.
Thulium silicate has been studied in this thesis as an interfacial layer with ultra-low EOT of 0.3 nm. Thulium oxide and hafnuim oxide are the high-k dielectrics used. These gate stacks have previously shown promising mobility, stability and reliability. In the next step a complete noise performance study would be useful to reveal information about the quality of this new gate stack.
Extraction of DC properties showed well-behaved IV characteristic for both nMOSFETs and pMOSFETs with W=10 µm and L=3 µm on $TmSiO/Tm_2O_3$ gate stack.
Noise measurements were performed on nMOSFETs and pMOSFETs with L=3 µm and L=10 µm and W=10 µm at $|V_{DS}|$= 100 mV and $|V_{GS}-V_t|$ from 0 V to 0.3 V using the noise set-up shown in Chapter 5. The gate voltage was always selected in a region that the drain current was at least an order of magnitude higher than the gate current. Most of the devices under study show a typical noise spectrum with $1/f^{\gamma}$ slope with γ close to 1. This slope does not vary much with frequency or gate voltage. The noise PSD is shown for typical nMOSFETs with W=10 µm, L=3 µm at $V_{GS}-V_t$=0.3 V for both $TmSiO/Tm_2O_3$ and $TmSiO/HfO_2$ gate stacks in Fig. 6.9. It is shown that for the same gate voltage overdrive the sample with HfO_2 shows a higher noise level.

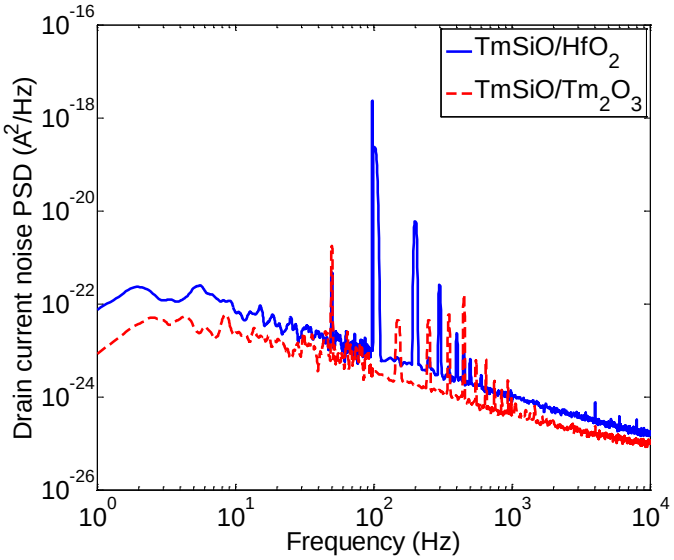


Fig. 6.9. Current noise spectrum versus frequency for nMOSFETs WxL=10x3 µm² taken at V_{DS}= 50 mV and $V_{GS}-V_t$= 0.3 V on $TmSiO/Tm_2O_3$ (dotted line) and $TmSiO/HfO_2$ (solid line) samples.

The noise data were normalized to the drain current for further analysis. This is shown for five different devices with W=10 µm and L=3 µm on $TmSiO/HfO_2$ gate stack. The devices show very uniform results which is depicted in Fig. 6.10. The normalized noise data in both gate stacks were compared to $(g_m/I_d)^2$ in order to fit

a proper model. The results suggest a correlated number and mobility fluctuation model. According to the equation 6.1, the N_t and α values were extracted for both gate stacks.

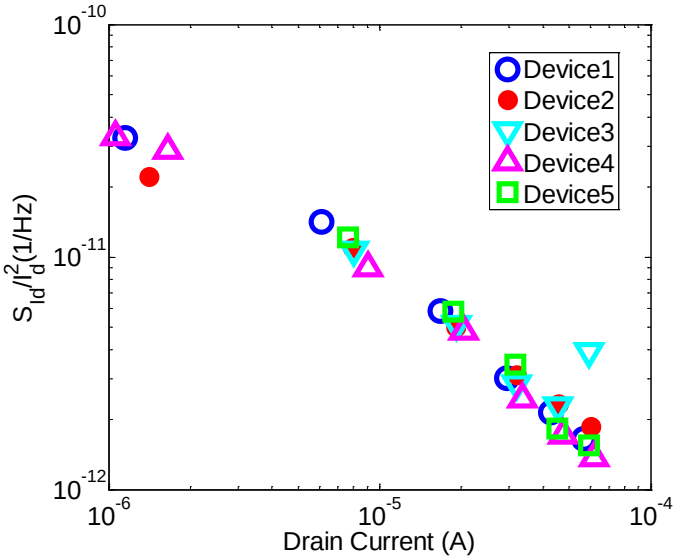


Fig. 6.10. Normalized current noise versus drain current for nMOSFETs with WxL=10x3 μm², V_{DS}= 100 mV, f=10 Hz on TmSiO/HfO_2 gate stack.

For extractions, the tunneling attenuation length is assumed to be 10^{-8} which is normally used for SiO_2/HfO_2 gate stacks. The extracted effective oxide trap density values are 1.5×10^{17} $eV^{-1}cm^{-3}$ and 2.5×10^{17} $eV^{-1}cm^{-3}$ for TmSiO/Tm_2O_3 and TmSiO/HfO_2 samples respectively. The N_t values for these gate stacks show good oxide quality for both gate stacks and lower effective N_t for TmSiO/Tm_2O_3.
For further comparison the input gate voltage noise ($S_{vg}=S_{id}/g_m$) is plotted over (I_d/g_m) for different devices on both wafers in Fig. 6.11. This plot also shows lower noise level for TmSiO/Tm_2O_3 wafer which was also shown in Fig. 6.9. Since these two gate stacks are composed of the same interlayer, the difference should be originated from the high-k layers. It can be either the fewer traps in Tm_2O_3 layer comparing to HfO_2, or smoother interface in TmSiO/Tm_2O_3 due to gradual transformation of Tm_2O_3 to TmSiO.
For a complete comparison, this promising gate stack (TmSiO/Tm_2O_3) is compared to state-of-the-art wafer with SiO_x/HfO_2 gate stack with comparable IL thickness (0.4 nm) which is chosen as benchmark data. These devices have the same width and different lengths. Therefore the noise data is normalized to the length for comparison. The normalized data of TmSiO/Tm_2O_3 gate stacks and the benchmark data were plotted over the gate overdrive which is depicted in Fig 6.12. This is shown for three nMOSFETs and three pMOSFETs shown with different symbols. Although some variation is observed in the data, the overall results look promising. The plot suggests an improved level of noise for nMOSFETs and comparable noise level for pMOSFETs.

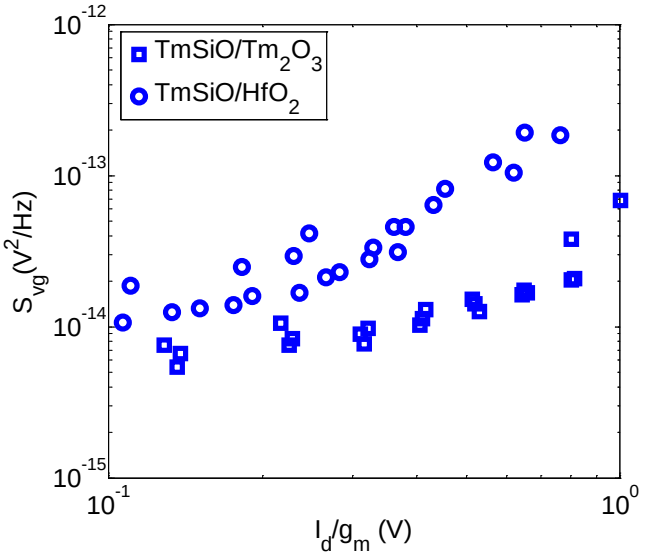
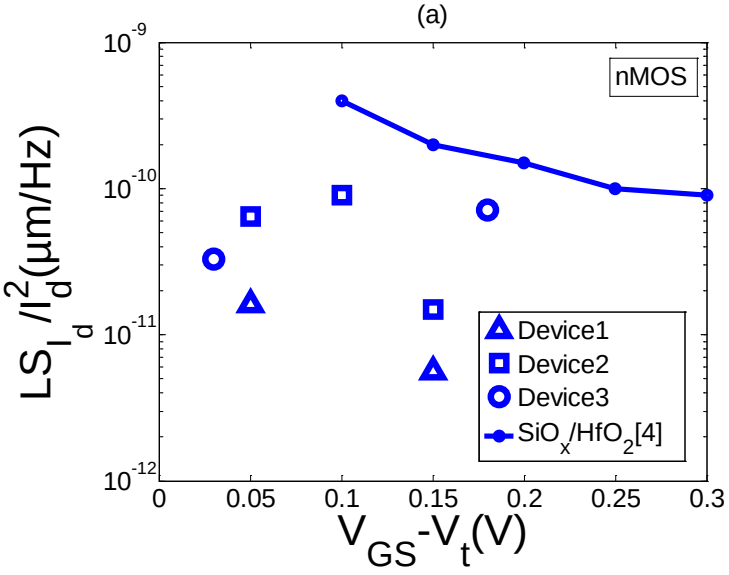


Fig. 6.11. Input gate voltage noise versus I_d/g_m for nMOSFETs on $TmSiO/Tm_2O_3$ (squares) and $TmSiO/HfO_2$ (circles) with W=50 µm, L=3 µm measured at *f*=10 Hz and V_{DS}= 50 mV.



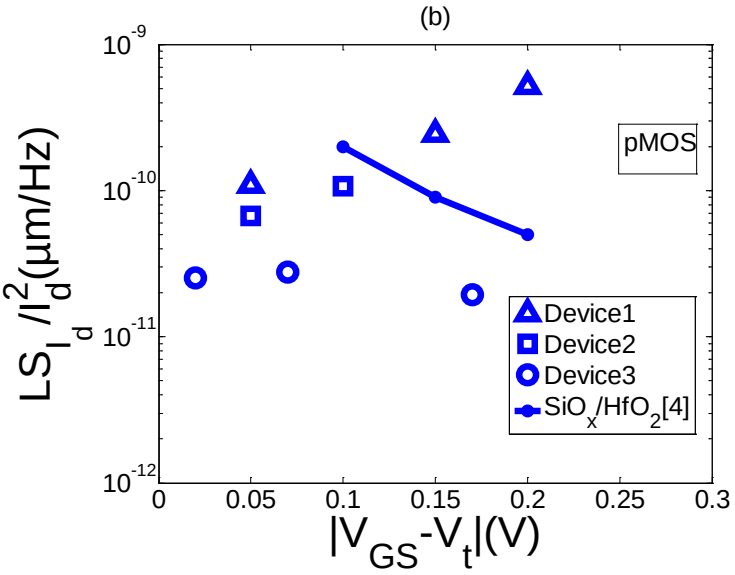


Fig. 6.12. Normalized drain current spectral density (marked with circle, square and triangle symbols) versus gate voltage overdrive at f=10Hz for $TmSiO/Tm_2O_3$ nMOSFETs with W×L=10×10 μm² (a) and pMOSFETs with W×L=10×3μm² (b) and reference SiO_x/HfO_2 with W×L=10×1 μm² (ref).

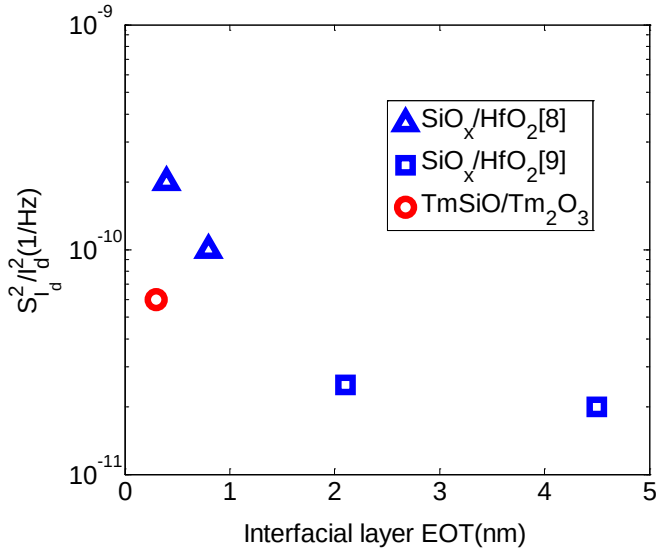


Fig. 6.13. Normalized drain current noise spectral density versus interfacial layer EOT for $TmSiO/Tm_2O_3$ nMOSFET (circle symbol) and SiO_x/HfO_2 reference nMOSFETs (square symbols) at f=10 Hz.

In Fig. 6.13, the normalized drain current spectral density is shown versus the interfacial layer EOT for different benchmark data with SiO_x/HfO_2 gate stacks and $TmSiO/Tm_2O_3$ sample. It is shown that the normalized noise decreases with increasing IL thickness. The decreasing slope is sharper for lower EOTs and it gets less sharp above 2 nm interlayer thickness. According to the double layer modeling [14], when the IL reaches the critical thickness (IL> 4.5-5 nm), the contribution of high-k traps to the total noise will be minor. The lowest EOT SiO_x

IL is around 0.4 nm which shows the highest noise level. The 0.3 nm EOT TmSiO IL depicted with a circle symbol shows lower noise even though the IL EOT is lower. Since TmSiO is a high-k interlayer, the actual physical thickness corresponding to 0.3 nm is 0.9 nm which is the reason for achieving lower noise. This is the thinnest interlayer which has been studied from a low frequency noise point of view.

6.3 Trap location in $TmSiO/Tm_2O_3$ dual layer stack

Among all measured devices, a few number of pMOSFETs showed different PSD representing Generation-Recombination (GR) noise which can be related to trap levels in high-k layer or interfacial layer. This kind of PSD was not observed in the nMOSFETs under study. The noise spectrum which represents GR noise shows a $1/f^2$ slope. In fig. 6.14, the current noise PSD of different devices with $TmSiO/Tm_2O_3$ gate stack is shown. The data is taken from 10 different devices with same area at V_{DS}=100 mV and gate voltage overdrive from 0 V to 0.4 V. It is visible that the slope varies from $1/f$ to $1/f^2$ which refers to devices showing pure $1/f$ noise or $1/f^\gamma$ with $1<\gamma<2$ related to devices with GR noise.

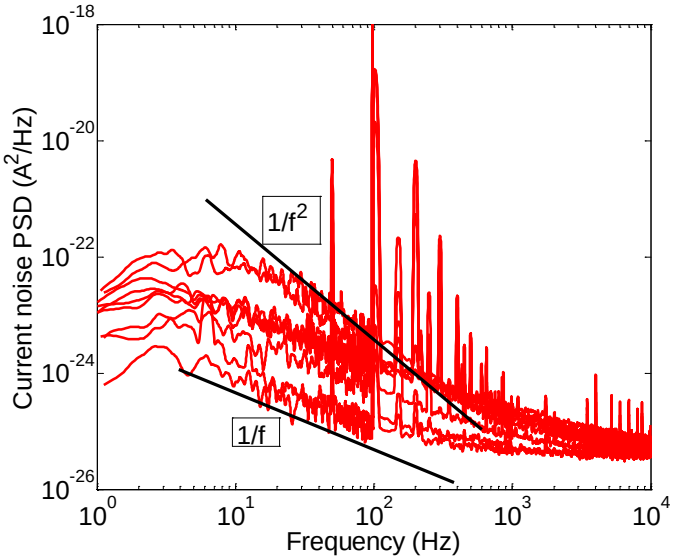


Fig. 6.14. Variablity in current noise PSD of $TmSiO/Tm_2O_3$ samples.

Further noise measurements at higher temperatures were performed to investigate the trap energy level. The selected temperatures started from room temperature then increased with small ΔT. The maximum measured temperature was around 90 °C and the temperature was not increased further in order to protect the oxide.

Fig. 6.15 shows the noise PSD of a pMOSFET at a fixed drain voltage for gate voltage overdrive from 0 V to 0.4 V at room temperature. According to the plot, lorentzian spectrum is observed at higher gate voltage overdrives which confirms generation-recombination (GR) noise.

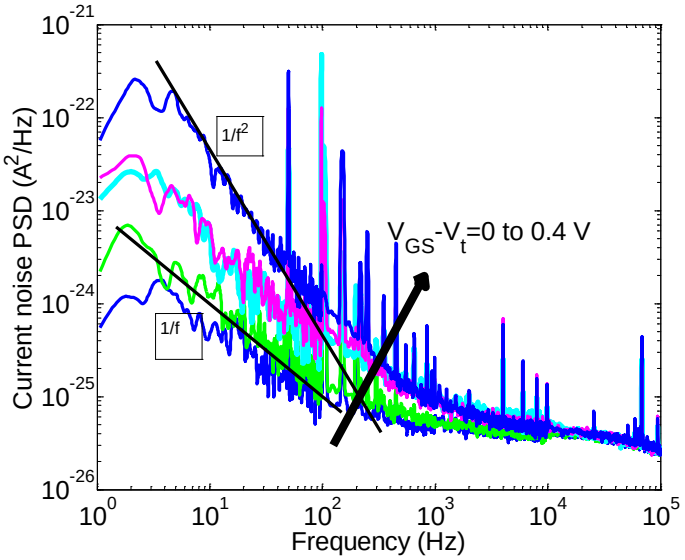


Fig. 6.15. Current noise spectrum versus frequency for pMOSFET WxL=10x3 µm², V_{DS}= -50 mV.

In order to detect the corner frequency, the drain current spectral density (S_{id}) is multiplied by the frequency. In Fig. 6.16, f×S_{id} of the previous device is depicted. The plot shows how the corner frequency shifts with increasing the temperature. In addition, the trap tunneling depth can be calculated through the corner frequency.

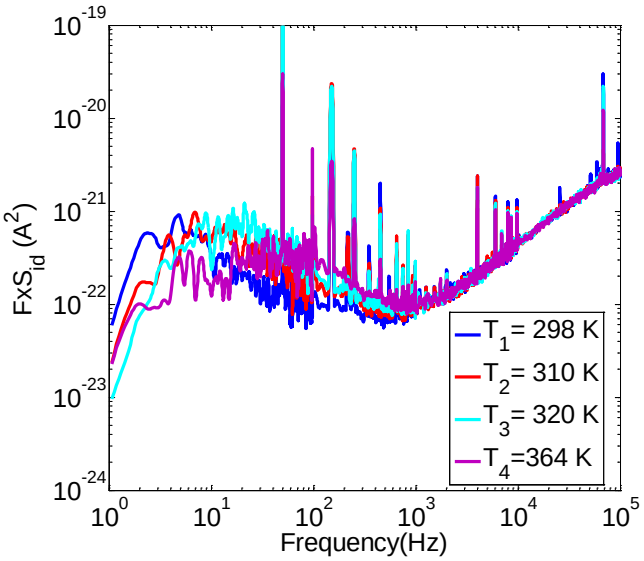


Fig. 6.16. f×S_{id} versus frequency for pMOSFET WxL=10x3 µm², V_{GS}-V_t=-50 mV, V_{DS}= -50 mV, amplifier gain =10^{-5} (A/V).

Assuming that trapping occurs by elastic tunneling, the tunneling depth can be calculated through equation 4.5.
The attenuation coefficient of the electron wave function for tunneling into the oxide is shown with γ and is calculated through equation 4.6.
The barrier height for holes for Tm_2O_3 is taken 3.1 eV according to [84] . Since the barrier height value for TmSiO is not available and silicate formation does not influence the barrier height a lot, the Tm_2O_3 barrier height is used for this

calculation. The hole effective mass of TmSiO is also unknown; therefore the tunneling depth is calculated for available hole effective masses of oxides such as SiO_2 and HfO_2. The effective masses of these two oxides vary between $0.3m_0$ to $0.58m_0$ [85][86][87].
The calculated values are summarized in Table. 6.2.

Table 6.2. Tunneling depth(γ) values calculated for different effective masses at different corner frequencies.

	Tunneling depth (γ) nm			
Temperature(T) K	298	310	320	364
Corner Frequency (f_c) Hz	4	10	20	60
SiO_2 effective mass (kg) $0.58m_0$	1.27	1.2	1.15	1.1
HfO_2 effective mass (kg) $0.3m_0$	1.77	1.67	1.6	1.49

According to the tunneling depth values for different corner frequencies, the suggested tunneling depth is around 1.5 nm. Since the physical thickness of the TmSiO layer is around 0.9 nm, the traps which are in a tunneling depth of 1.5 nm should be located in the Tm_2O_3 layer.

6.4 Discussion

In this work double layer MOSFETs with different dielectric materials and interlayers have been studied with the focus on low frequency noise. The oxide trap density has been used as a figure of merit for $1/f$ noise performance. The extracted values for all the samples are compared in fig. 6.17. The trap density values vary from 1×10^{17} $eV^{-1}cm^{-3}$ to 4.8×10^{19} $eV^{-1}cm^{-3}$ from the reference wafer with SiO_2 as gate dielectric to O_3 based SiO_x/HfO_2 gate stack with 0.4 nm IL.
Since the traps are mainly located in the high-k layer, and the trapping and de-trapping occurs due to tunneling into the oxide, a thick enough IL layer can block the noise from the high-k layer. However very thin interlayers are desirable for achieving low EOT gate oxides. Therefore there is always a trade-off between lower EOT and higher low-frequency noise.
The gate stacks with ultra-low EOT TmSiO IL (0.3 nm) shows promising N_t values although the IL EOT and total EOT is very low in these gate stacks. The reason behind this is that the ultra-low 0.3 nm IL EOT corresponds to an actual physical thickness of 0.9 nm which is more effective in blocking the noise from the high-k dielectric due to limiting the tunneling of carriers. Moreover, the interface between TmSiO and Tm_2O_3 is a gradual transmission of Tm_2O_3 to TmSiO resulting in a smoother interface. The oxide trap density of $TmSiO/Tm_2O_3$ is actually comparable to the reference wafer with pure SiO_2 dielectric. Among all, chemical oxide SiO_x/HfO_2 gate stacks show the highest noise. Although the IL is very thin in these samples, the quality of the HfO_2 seems to be the main reason causing this noise. It is worth noting that the quality of HfO_2 has been improved for the latter samples.
Devices with $LaLuO_3$ high-k dielectric and no interlayer show a higher N_t comparing to the reference wafer with pure SiO_2. Yet the N_t values are comparable

to other modified high-k dielectrics. Since there is no interlayer in these devices, very low EOT is achieved. However the interface state density should be measured for future work. There might be a need for a very thin IL for better interface; TmSiO can then be used as a possible high-k interlayer.

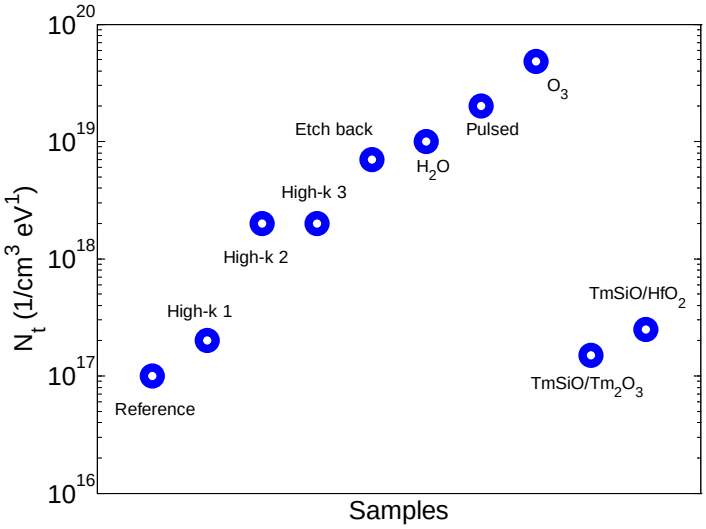


Fig. 6.17. Effective trap densities for different samples in this study.

All the noise measurement results of samples in this work have been fitted to proper noise models. The number fluctuation model and the correlated mobility and number fluctuation model are found to be suitable models for these devices. For samples with correlated mobility and number fluctuation model, the mobility parameter α, has been extracted which is also a figure of merit for 1/*f* noise performance. The extracted values are summarized in Table 6.3.

Table 6.3. mobility parameter (α) values for samples under study.

Sample	α (Vs/C)
$LaLuO_3$ samples	1×10^4
$TmSiO/Tm_2O_3$	0.4×10^4
$TmSiO/HfO_2$	0.5×10^4

Chapter 7

Summary and future outlook

This thesis contains a comprehensive study of low-frequency noise in advanced gate stacks for nano-scaled MOSFETs or similar. The low-frequency noise has been used as a tool to investigate the quality of the gate oxide. MOSFETs with different high-k dielectric and interfacial layer materials fabricated in house at KTH have been studied. The devices have been characterized electrically followed by low-frequency noise measurements. Different physical parameters have been extracted through these measurements.

The main results of this work are summarized below.

Schottky barrier FinFETs and ultra thin body SOI MOSFETs have been characterized and it is shown that dopant segregation is an effective method in reducing the barrier height and achieving higher on-current and lower low-frequency noise in pMOSFETs. The noise level of FinFETs is shown to be higher than for UTB MOSFETs.

In future work, this elevated noise level can be decreased by improving the interface of the FinFETs. The devices with Schottky barriers feature a significant variability in the current and noise. This variability is illustrated by measuring the same device in forward and reverse direction by changing the source and drain. Ideally Schottky barriers with less variability are aimed.

High-k dielectrics are implemented in CMOS technology together with an interfacial layer to provide good quality interface.

$LaLuO_3$ has been studied as a high-k candidate in CMOS technology. Samples with different $LaLuO_3$ thicknesses deposited through MBE with no interfacial layer and samples with an SiO_2 interfacial layer have been studied. Low-frequency noise characterization reports an order of magnitude higher noise level for $LaLuO_3$ gate stacks compared to reference SiO_2 stack which is comparable to HfO_2 MOSFETs. The implementation of the interfacial layer has reduced the noise level significantly. Since the IL in these samples is thick, for future studies, a thinner IL is needed in order to achieve low enough EOT and good interface quality at the same time. The non-silicon TmSiO interlayer can be suggested as a possible low EOT IL.

Chemical oxide SiO_x MOSFETs fabricated insitu in the ALD have been studied. Very thin uniform layer SiO_x has been formed through this insitu method using O_3 and H_2O as oxidizing agents and different pulsing schemes using Ar gas. An HfO_2 high-k layer has been deposited on top in the same ALD. The low-frequency noise is increased for very thin chemical oxide SiO_x MOSFETs comparing to exsitu

fabricated SiO_x but comparable to other chemical oxide SiO_x MOSFETs. The sample fabricated with H_2O shows the best noise performance.

In this work, thulium silicate as a novel non-silicon interlayer is introduced and characterized for the first time as low-frequency noise point of view. This interlayer is the thinnest interlayer (0.3 nm EOT) reported to best of author's knowledge for low-frequency noise measurements. Tm_2O_3 and HfO_2 have been implemented as high-k materials. These two gate stacks show excellent noise properties and reasonable effective oxide trap density values such as 2.5×10^{17} and 1.5×10^{17} for $TmSiO/HfO_2$ and $TmSiO/Tm_2O_3$ respectively. This is comparable to or even better than the values reported for the state of the art SiO_2/HfO_2 based stacks. Lower noise level is observed in $TmSiO/Tm_2O_3$ gate stack. Since the interlayers are the same in both stack, this can be related to fewer number of traps in Tm_2O_3 dielectric or a better interface with TmSiO layer leading to lower $1/f$ noise. The latter can be the most probable conclusion since there is no sharp interface only a gradual transition from TmSiO to Tm_2O_3.

For a more accurate noise study on gate stacks with TmSiO interlayer, gate stacks with different interlayer thicknesses can be fabricated. This can help to find out the effective interlayer thickness that can block the noise from the high-k layer while providing reasonable EOT.

In summary, a detailed study of the quality of double layer high-k gate stacks has been performed. There are some issues regarding each study that need to be addressed in future work which were discussed in Chapter 6 and earlier in this chapter. In the following paragraph a suggestion is given for further low-frequency noise studies for all samples.

The devices under study in this thesis were all long channel devices. RTS noise referring to single traps can be observed in short channel devices. Studying RTS noise can find the relation between the traps in short devices and $1/f$ noise in larger devices. Therefore short channel devices are needed for a complete noise study.

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