Modeling of stresses and deformation in thin film and interconnect line structures

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Preface

The research presented in this thesis was carried out between May 1997 and June 2001 at the Department of Solid Mechanics, Royal Institute of Technology in Stockholm, Sweden. The background for this project is as follows. In 1997 professor Subra Suresh, MIT, USA spent half a year at the department as a guest professor. As part of the collaboration work between Subra Suresh and the department, professor Peter Gudmundson initiated a Masters thesis project directed into mechanical properties of microelectronic circuits. At that time, I was looking for an interesting Masters thesis topic. Peter contacted me and asked if I was interested in working with this project. When Peter, who eventually became my advisor, explained what the project was all about, and that it was likely to be extended to a doctoral project which was going to be performed in close cooperation with professor Suresh, I decided to go for it. I have truly enjoyed research and I want to express my sincere gratitude to my advisor Peter Gudmundson for excellent guidance and cooperation during the course of the work. We have had many discussions on various aspects of solid mechanics, sometimes quite unconnected to the research. Peter has always taken time to discuss and seriously consider my sometimes unconventional ideas. I much appreciate his enthusiasm and deep insight in solid mechanics problems. I would also like to sincerely thank Subra Suresh. He has been a great source of inspiration and his advice and vast knowledge have been of great value for the research presented in this thesis. I have also really enjoyed the visits at MIT.

Finally, I would like to thank everybody at the department for creating an excellent research atmosphere as well as Dr. Andrew Gouldstone and M.Sc. Tae-Soon Park at MIT for valuable discussions.

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Bastuträsk in August 2001

Adam Wikström
Dissertation

This dissertation contains a summary and the following appended papers.

Paper A


Paper B


Paper C


Paper D


Paper E

Division of work between co-authors.

**Paper A**

Wikström performed the analysis and most of the writing. Gudmundson developed the foundation of the analytical formulations as well as provided guidance and advice in the work. Suresh wrote the introduction and provided guidance in the work.

**Paper B**

Wikström performed the analyses and most of the writing. Gudmundson provided guidance and advice in the work. Suresh wrote the section with comparisons to experiments and the part regarding electromigration and provided guidance in the work.

**Paper C**

Wikström performed the analyses and writing. Gudmundson provided guidance in the work.

**Paper D**

Wikström performed the analyses and writing. Gudmundson developed the boundary layer solution for large initial curvatures and provided guidance in the work.

**Paper E**

Wikström performed the analyses and writing. Nygårds provided the code for the generation of plane periodic Voronoi cells.
Abstract

This thesis contains five papers concerned with temperature induced stress evolution in thin films, unpassivated and passivated interconnect lines. In the first two papers, analytical expressions for the average stresses in unpassivated and passivated interconnect line structures are presented. For unpassivated lines, the analytical solution is valid for any line aspect ratio (thickness to width ratio) and pitch of the elastic lines. For passivated lines, a solution is presented for the limiting cases of vanishing line aspect ratio and very large line aspect ratio. It is shown that the result for very large line aspect ratio represents a reasonable approximation for a wide range of relevant geometries. The results for unpassivated as well as passivated lines compare favorably with finite element simulations as well as experimental results from the literature. In the third and fourth paper, the possibility to extract material properties from curvature measurements is explored. The determination of stresses based on curvature measurements of passivated line structures is investigated in paper three. A method that allow the measured averaged stress in the entire layer to be divided into line and passivation stresses is presented. In paper four, the possibility to extract relevant material properties from curvature measurements on initially curved substrates is investigated. It is shown that material properties can be extracted by a theoretical simulation of curvature measurements in combination with the solution to an elastic boundary value problem. Analytical solutions are presented for a substrate with spherical initial curvature. In paper five, the effect of elastic anisotropy on the stress state of a polycrystalline copper film with columnar grain structure is investigated theoretically. In order to model the grain structure, a Voronoi algorithm is employed. The average texture of the copper film is taken from experiments reported in the literature. A three-dimensional finite element model is applied. The effect of loading as well as the cyclic behavior was explicitly investigated. Finally, a direction dependent hardening law that is based on the elastic anisotropy is proposed.

Keywords: Thin films, thermal stress, theory and modeling, interconnect lines, finite element, texture, copper, unpassivated lines, passivated lines
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### Appended papers

**Paper A**  
Thermoelastic analysis of periodic thin lines deposited on a substrate

**Paper B**  
Analysis of average thermal stresses in passivated metal interconnects

**Paper C**  
Stresses in passivated lines from curvature measurements

**Paper D**  
Thermal deformation of initially curved substrates coated by thin inhomogeneous layers

**Paper E**  
Anisotropy and texture in thin copper films - an elasto-plastic analysis
1. Introduction

An integrated circuit is composed of millions of electronic devices deposited in several layers. These devices are connected by a very complex pattern of metallic interconnects. Common interconnect materials are aluminum, copper and tungsten. The devices and interconnects are embedded in an electrically insulating passivation material such as silicon oxide. Figure 1 shows a close-up of an IBM PowerPC 750 chip where the electrically insulating passivation material has been etched away. It is observed from Figure 1 that the geometry is extremely complex and the width of individual interconnects may be significantly smaller than 1 µm. As a comparison, the thickness of a human hair is normally about 50 µm.

The reliability of microelectronic devices is strongly influenced by internal stresses that develop in the interconnect structures. These stresses may cause chip failure through mechanisms such as cracking of the passivation or interconnect lines, void growth that occurs either through a high mechanical load or through interaction with electric fields. Sources of such stresses include: (a) thermal expansion mismatch between dissimilar materials such as the substrate, interconnects and passivation layers, caused by temperature changes introduced during processing, manufacture and service, (b) the passage of electric current in the interconnects which introduce non-uniform atomic transport, so called electromigration, (c) non-equilibrium conditions during film deposition, (d) various processes used to create geometrical and topological changes during etching and patterning of interconnect lines and during planarization, (e) diffusion and chemical reactions which occur at and across interfaces during temperature changes, (f) the absorption of substances such as water vapor.

Figure 1. CMOS 7S with 6 layers of copper and one layer of tungsten interconnects. The electrically insulating passivation material has been etched away. Courtesy of International Business Machines Corporation. Unauthorized use not permitted.
The research presented in this thesis is mainly focused on the determination of stresses originating from thermal expansion mismatch between dissimilar materials. Even so, the determination of internal stresses require that reliable material properties are known. This is something that presents great difficulties when inelastic deformations occur.

It is obvious that a theoretical prediction of the internal stresses in an entire circuit presents enormous difficulties. Therefore, simplified but technically relevant experimental or theoretical setups are normally used to obtain design rules and qualitative predictions of the material with respect to mechanical properties, electromigration behavior, electrical properties and so on.

The objective of this thesis is to enhance the understanding of thermal stress evolution and mechanical behavior of the most commonly used theoretical and experimental model systems. Particular emphasis has been placed on the development of analytical solutions. The results are believed to be of great value for investigations of parameter dependences, evaluation of experimental data and for estimates of the stress state in real components.

2. Manufacturing and interconnect performance

The manufacturing of microelectronic devices is based on several processing steps. The starting point is generally a silicon wafer with a thickness of about 0.5 mm and a diameter of 200-300 mm. Often the substrates are first thermally oxidized in steam to produce blanket SiO₂ films at process temperatures that are of the order of 1000 °C.

From this point, there are mainly two types of fabrication techniques. (a) the traditional technique and (b) the Damascene technique.

![Figure 2: A schematic of the difference between the traditional and damascene techniques in microelectronic manufacturing.](image-url)
The traditional technique

Here, the metal film, which normally consists of aluminum or aluminum with a small fraction of copper (typically 0.5%) to enhance the resistance to electromigration, is first deposited. There are several film deposition techniques, two of the most common ones are chemical vapor deposition (CVD) and sputter deposition. The process temperature for CVD is normally in the range of 400-500 °C. Sputter deposition may be performed in a variety of ways with process temperatures ranging from room temperature and up to about 500 °C. For the Al(Cu) based interconnect layers, processing temperatures below 450 °C are required, since the metal degrades rapidly above this temperature, forming voids and hillocks [1]. The metal film is then patterned into the desired interconnect line structure through etching. An electrically insulating material such as silicon dioxide or doped silicate glasses is then deposited such that the interconnect line structure becomes completely embedded in the passivation material. The insulator deposition is normally followed by some type of planarization process such as chemical mechanical polishing. The entire process is repeated until the desired number of layers is obtained.

Copper deposition and the Damascene process

Copper has quite recently emerged as an interconnect material in the microelectronic industry. Two advantages with copper as an interconnect material is that it is quite insensitive to electromigration and that its electric conductivity is about 70% higher than that of aluminum. The main drawbacks are that copper require a diffusion barrier to prevent contamination of silicon and that it is difficult to etch copper. Due to the difficulties to etch copper, it is instead advantageous to etch on the insulating material and to deposit the copper by means of electroplating. Electroplating requires a seed layer whose function is to conduct the current from a contact at the substrate edge to all points on the substrate where a deposit is desired. Various methods exist to manufacture interconnects through electroplating. Two common techniques are referred to as Through-mask plating and the Damascene process [2,3]. When Through-mask plating is used, the seed layer is first deposited. A masking material is then used on top of the seed layer. Electroplating occurs only on those areas of the seed layer that are not covered by the mask. The masking material and the surrounding seed layer are finally removed. The idea with the Damascene process is to first deposit an oxide layer on the substrate, then to dry-etch trenches that conform to the geometry of the interconnect lines in the oxide layer. Thin barrier and seed layers are then deposited over the patterned material. The trenches are then filled with copper by recourse to electroplating. The extra copper above the trenches are subsequently removed by chemical mechanical polishing. The entire process is repeated until the desired number of layers is obtained.
Figure 3: Cross section of one layer of parallel passivated interconnect lines. The aspect ratio is defined as the thickness to width ratio of the lines.

**Issues regarding interconnect performance**

As microprocessor clock frequencies increase, interconnect (RC) delay becomes a larger fraction of the total clock delay. Interconnect delay on a long interconnect line can approach 30% of the clock cycle for a 0.25 \( \mu \text{m} \) technology generation 400 MHz microprocessor [4]. There are several geometrical and material issues that affect interconnect delay.

The interconnect delay turns out to be sensitive to interconnect pitch, see Figure 3. Studies show that a 0.7x reduction in pitch gives a 2x increase in interconnect delay for a constant aspect ratio and two different line lengths of 1 mm and 10 mm respectively [4]. Hence, interconnect delay can be decreased by allowing for wider pitch. This is the main reason why the manufacturers keep adding more and more metal layers to the circuit. Historical trends suggest that about one new layer per generation is added. The thickness of the metal layers and the pitch generally increase from the lower to the upper layers.

The metal aspect ratio (thickness/width) also affects the interconnect delay. Traditionally, the pitch has reduced by 0.77x per generation while the average metal thickness has remained constant [5]. At the same time the average metal aspect ratio has increased from 0.4 to 1.7. Theoretical studies by show that increases of aspect ratio up to ~ 2 provide improved interconnect delay characteristics for a constant pitch [5]. The average aspect ratio for the Intel 0.25 \( \mu \text{m} \) process is 1.7. Increases in aspect ratio have traditionally been limited by the ability to pattern and etch metal spaces and the ability to fill them with dielectric.

Interconnect delay is also reduced by decreasing the metal resistance (i.e by using Cu instead of Al as an interconnect material) and/or by reducing the interconnect capacitance through use of low dielectric constant materials with high resistivity.
3. Size effects

The determination of stresses and strains requires access to reliable material properties. In order to study this in some more detail, the concept of averaging must be discussed. Since a material property is a measured quantity, it will always represent a relation between stresses and strains that is averaged over some volume (the test sample). The smallest volume required to experimentally obtain a repeatable and stable material behavior is called a representative material volume (RVE). Geometrical features that are significantly larger than the smallest possible RVE may then be included in a geometrical description and predicted by modeling and computations. For example, elastic behavior takes place on the atomic scale. Hence, the RVE that is required to represent elastic behavior within a grain is very small as compared to the grain size. A RVE that represents elasto-plastic behavior require a sufficiently large number of dislocations to average over. It is therefore clear that elasto-plastic material behavior requires a much larger RVE as compared to purely elastic behavior. This effect has recently been observed very clearly in indentation experiments [6].

Figure 4. (a) Top-view TEM image of the flat as-deposited Al film, of 0.4 µm thickness, on Si substrate. (b) Cross-sectional TEM image showing the columnar grain structure and a thin layer of amorphous SiO₂ between the Al film and Si substrate. Reprinted from Gouldstone et al. (2000) with permission.
Thin films represent a fundamental building block in the manufacturing of microelectronic circuits. It is therefore not surprising that much experimental and theoretical work on thin films exists in the literature [8-9]. The film thickness of metal films or passivation layers is typically in the micron or sub-micron range while diffusion barriers and may be significantly thinner. Thin metal films often exhibit a columnar grain structure with a grain size that is of the order of the film thickness. Figure 4(a) show a top-view TEM image of an as-deposited Al film with a thickness of 0.4 µm indicating the grain structure. In Figure 4(b), a cross-sectional TEM view of the same film as shown in Figure 4(a) is presented. The columnar grain structure of the Al film is clearly observed. A metal film that has been patterned into lines is shown in Figure 5. Note that the width of the lines is of the same order of magnitude as the film thickness and grain size. Experimental investigations [6,8] have indicated that plastic and creep properties depend on the geometrical dimensions of the film or interconnects. It is generally concluded that smaller is stronger. This is normally rationalized by noting that plasticity is controlled by dislocation (or defect) motion. When the dimensions of the structure decrease, the possibility for the defects to move become severely restricted. For bulk materials the Hall-Petch relation states that the yield stress is inversely proportional to the square root of the average grain size. For thin films, the yield strength appears to be inversely proportional to the film thickness raised to a number somewhere between one half and one. This size dependence has triggered an intense research on so called non-local or gradient plasticity, see Wikström [7] for a literature survey. Hence, as the physical dimensions of microelectronic devices continue to decrease, the relevance of models based on elastic behavior becomes of increasing importance. The size dependence implies that mechanical properties must be measured on realistic geometries.

Figure 5: Top view of an array of unpassivated interconnect Al lines. The thickness of the lines is 1 µm, the width 4 µm and the pitch 8 µm. Reprinted with permission from Y. -J. Choi.
4. Common model geometries

Since the geometry of an entire circuit is extremely complex, it may be wise to study idealized geometries experimentally as well as theoretically. These geometries may be used to (a) obtain more or less precise values of various material properties or to (b) rank different materials or geometries with respect to yield behavior, creep behavior, resistance to electromigration, interconnect delay or various other properties. It is then hoped that this information should result in increased understanding which ultimately could be translated into design rules that may be used during the design of integrated circuits. Some common model geometries are shown in Figure 6. Idealized models of the kind that is shown in Figure 6 may be subjected to various loads such as thermal cycling, electric currents, moisture, mechanical loading and so on. Many theoretical as well as experimental investigations of these idealized geometries exist in the literature. A very nice presentation of the electromigration phenomenon where theoretical as well as experimental aspect are treated have been written by Thompson and Lloyd [9]. The yield stress of thin metal films have been studied experimentally and theoretically by many researchers [6, 8, 10-13]. Theoretical studies of the yield strength of thin metal films are often based on a model of one threading dislocation that originally was proposed by Freund [10]. Theoretical models for the yield strength in unpassivated or passivated lines are often based on modifications of the film model. However, creep or plastic yielding is always preceded by elastic deformation. It is therefore convenient to have access to reliable and easy-to-use elastic models with which the stress evolution in the most common model geometries can be computed. Some theoretical and experimental models for stress evaluation will be discussed below.
Theoretical models

When the material properties, residual stresses and external loads are known, the stress and strain fields may be obtained by making use of numerical methods such as the finite element method. It is in fact the only reasonable method when a complex material behavior is included in the model. However, when purely elastic materials are considered it is sometimes possible to compute stresses by approximate easy-to-use formulas which clearly show parameter dependencies. The biaxial stress state in a continuous elastic and isotropic thin film deposited on a substrate subjected to thermal loading is well known and may be expressed as

\[
\sigma_{\text{film}} = \frac{\alpha_s - \alpha_f}{1 - \nu_f} E_f \Delta T
\]

where \(\alpha_s\) and \(\alpha_f\) represent the coefficients of thermal expansion of the substrate and film respectively. Young’s modulus and Poisson’s ratio of the film are denoted by \(E_f\) and \(\nu_f\) respectively. A temperature change from a stress free state is denoted by \(\Delta T\). In practice, the stress free temperature is normally assumed to be the temperature at which the film deposition is performed. In paper A, approximate expressions for the average stresses in patterned unpassivated lines are presented. The model which is based on elastic material behavior provides a very easy-to-use tool to describe the average stresses in the patterned lines. The only relevant geometrical parameter is described by the line aspect ratio. Since the behavior of most passivation materials is close to linear elastic, this model may be of particular interest for modeling of the Damascene process. In paper B, expressions for the stress state in passivated lines are presented for the limits of vanishing and very large line aspect ratio. It is shown that the expression that is valid for very large line aspect ratios provide a good approximation for aspect ratios that are larger than \(\sim 2\). Note that the average aspect ratio, which for the Intel 0.25 \(\mu\)m process is 1.7, traditionally have increased for each technology generation.

The effect of elastic anisotropy on polycrystalline copper films

As observed in Figure 4, a real metal film is built up by grains which may be defined as material pieces in which the metal atoms are arranged in well defined crystallographic planes. Since many metals have a cubic crystal structure, the stiffness of a single grain is dependent upon the loading direction. This stiffness direction dependence is for example very strong in copper, not as strong in aluminum and non-existent in tungsten. However, when a cubic material is heated the expansion is uniform and direction independent. Hence, when a polycrystalline copper film is heated, a highly non-uniform stress field results. The average stress that results can be captured through eq. (1) if the Young’s modulus and Poisson’s ratio are interpreted as average values for the entire film. In paper E the effect of non-uniform stresses due to elastic anisotropy has been
studied with respect to loading directions, texture, yield behavior and cyclic yield behavior. One conclusion is that care has to be taken when experimental data based on different kinds of loading are compared.

**Experimental methods**

There are mainly three experimental methods that are commonly used to measure material properties in thin films and interconnect lines. (a) indentation methods, (b) X-ray techniques and (c) curvature measurements. Micro- and nano-indentation mainly provide information about local elastic and plastic properties [6]. When X-ray measurements are utilized, mechanical or thermal loading is applied to either a free-standing film or a film/substrate system [11]. The X-ray measurements provide elastic strains that are averaged over a large number of grains. Furthermore, X-ray measurements can provide information about the average elastic strains in different texture components of the film. In order to convert the measured average elastic strains into average stresses, the elastic stiffness tensor of the film must be known.

**Curvature measurements**

Curvature measurements can be used when the film is attached to a flat elastic substrate. The film/substrate system is normally subjected to thermal loading which due to thermal mismatch between the film and substrate gives rise to a curvature change of the initially flat substrate [12]. Mechanical loading can also be applied under certain circumstances [13]. The advantage with curvature measurements is that no information about the material properties of the film is required. The drawback is that the applied strain is controlled by the applied temperature, a fact that prevents these quantities from being prescribed independently. An illustration of curvature measurements is shown in Figure 7.

![Figure 7: Illustration of curvature evolution due to a temperature change.](image-url)
The resulting curvature change is normally evaluated from (a) slope measurements where the angle between an incident and reflected laser beam is evaluated or by (b) displacement measurements by a surface profilometer. The measurements are generally performed on a back-polished substrate. Since a constant curvature theoretically results when the substrate is initially flat, the measured slopes or displacements are fitted through a least squares procedure to a deflected shape that has a constant curvature.

The method of curvature measurements provides information about stress changes averaged over the entire coating of thickness $t$, see Figure 6. The in-plane average stress changes ($\langle \sigma_x \rangle$, $\langle \sigma_y \rangle$) are obtained through mechanical equilibrium and measured curvature changes which results in a generalized Stoney formula [14].

$$
\begin{bmatrix}
\langle \sigma_x \rangle \\
\langle \sigma_y \rangle 
\end{bmatrix} = -\frac{E_s}{6(1-\nu_s^2)} \frac{h^2}{t} \begin{bmatrix}
1 & \nu_s \\
\nu_s & 1
\end{bmatrix} \begin{bmatrix}
\Delta \kappa_x \\
\Delta \kappa_y
\end{bmatrix}
$$

In eq. (2), $h$ denotes the thickness of the substrate, $E_s$ Young’s modulus of the substrate and $\nu_s$ Poisson’s ratio of the substrate. The curvature change along and across the lines on the initially flat substrate is denoted by $\Delta \kappa_x$ and $\Delta \kappa_y$ respectively. Note that equation (2) does not require any information about the material properties of the thin film, only the material properties of the substrate and geometry are needed. The reason for this is that since the film is thin as compared to the substrate, the whole film/substrate system will behave predominantly elastic. For a homogeneous film, $\Delta \kappa_x = \Delta \kappa_y$ and a biaxial state of stress results. When unpassivated or passivated lines are considered, the curvatures and corresponding average stresses generally differ along and across the line direction. In situations where the thin layer of thickness $t$ consists of unpassivated patterned lines, the average stress along and across the patterned lines are easily obtained by multiplying the average stresses in the entire layer (eq. 2) by the pitch to width ratio [15]. For passivated lines a more complicated situation arises. Even though the stresses in the combined line/passivation layer are known through eq. (2) it is generally not trivial to separate the stresses in the line and passivation respectively. In paper C, a method to separate the stresses in the lines and passivation without knowledge of the solution to the complete boundary value problem is demonstrated. In order to accomplish this it is assumed that (a) the lines are very long, (b) the line/passivation layer is planarized and (c) that linear thermoelasticity remains valid for the substrate, line and passivation. One possible application of this method would be to analyze creep experiments [16]. In this case a substrate with passivated lines is heated and kept at a certain temperature while the curvature changes are monitored. After some time, the curvature stabilizes at a certain value. A small temperature change is then suddenly applied. The stress that results from the temperature change may then be computed by means of the formula presented in paper C. These stresses represent the internal stress buildup that gradually relax due to creep effects.
For an initially flat substrate with a homogeneous thin film deposit subjected to thermal loading, the resulting curvature will theoretically be uniform over the substrate. For an initially non-flat substrate however, a non-uniform curvature results. When curvature measurements are performed, the curvature change that enters eq. (2) is averaged in a sense. Two basic questions then emerges: (a) Is it meaningful to obtain thin film material properties from curvature measurements performed on initially non-flat substrates, i.e is the state of stress in the film theoretically homogeneous even if the resulting curvatures vary over the substrate? (b) How can an eventual initial curvature be accounted for? As observed from eq. (1), the stress build-up in a thin film on a thick substrate due to thermal loading is primarily caused by substrate in-plane strains. Curvatures play a secondary role and may be viewed as an effect rather than a cause of stress build-up in the film. Hence, a homogeneous state of stress results in a homogeneous film of constant thickness that is deposited on a non-planar thick substrate. It is therefore meaningful to interpret curvature measurements also for situations when the curvatures vary over the substrate. Since the behavior of the entire thin film/thick substrate system behaves predominantly elastic, the effect of the possibly inelastic film may be treated as a loading parameter only. Hence, it is possible to derive a modified Stoney formula by a simulation of curvature measurements in combination with the solution to an elastic boundary value problem that considers the initially curved substrate. This problem has been treated in paper D. An analytical solution that is based on slope measurements is presented for substrates with spherical initial curvature.

5. Summary of appended papers

Paper A

This paper considers a periodic pattern of thermoelastic unpassivated lines deposited on a substrate and subjected to a temperature change. Approximate expressions for the curvatures and volume average stresses in the lines have been derived. The predictions compare favorably with finite element simulations for Si substrates with Al, Cu or SiO₂ lines. Comparisons have also been made to prior experimental measurements along and normal to patterned SiO₂ lines on Si substrates. The model presented here thus provides a very simple analytical tool for the extraction of curvatures and volume averaged stresses for any width, thickness and spacing of the lines.

Paper B

In this paper, a periodic pattern of passivated lines deposited on a Si substrate is considered. Analytical expressions for volume averaged thermal stresses have been derived for situations where the thickness to width ratio of the interconnect lines is
small or large. The expressions are derived for the most general case of elastic and thermal anisotropy in the line, passivation and substrate. It is shown that the theoretical predictions, particularly those for the hydrostatic stresses, are in excellent agreement with detailed finite element calculations for a wide range of practically relevant geometries and material combinations. Plastic yielding in the interconnect lines is briefly addressed. The theoretical predictions also show reasonable agreement with experimental results from the literature based on x-ray diffraction measurements.

**Paper C**

The possibility to determine three-dimensional averaged stresses in lines and passivation solely from information about changes in curvatures is studied. An exact expression which is valid for arbitrary in-plane shapes and volume fractions of lines is presented. Unlike the determination of average stresses in a thin continuous film, this method requires knowledge of the material properties of the line and passivation. In order to establish the existence of a unique solution, some requirements regarding the differences between elastic constants in the line and passivation must be fulfilled. The sensitivity of the method to uncertainties in curvature data has been investigated for a typical line/passivation geometry.

**Paper D**

Mechanical elastic and inelastic properties of thin films are often studied by means of the curvature measurement technique in combination with the Stoney formula. It is then implicitly assumed that the elastic substrate is initially flat which implies that the curvatures theoretically remain constant over the substrate. However, for a substrate that is initially non-flat the resulting curvature change will be non-uniform over the substrate. A method for the extraction of mechanical properties from curvature measurements on initially non-flat substrates is proposed. The method is based on a simulation of curvature measurements in combination with the solution to an elastic boundary value problem (BVP). The elastic BVP appears because the film is very thin as compared to the substrate, a fact that cause the combined film/substrate system to behave elastically were the influence of the film enters as a load parameter only. An analytical solution is presented for a film/substrate system with a spherical initial curvature.

**Paper E**

A polycrystalline thin copper film with columnar grain structure has been modeled within a three-dimensional continuum framework. The film which is deposited on a thick substrate exhibits a fiber texture with (111), (001) and randomly oriented grains. The effect of elastic anisotropy on stress inhomogeneity and effective behavior has been analyzed. Mainly two load cases have been considered. Biaxial/thermal loading of a film deposited on a silicon substrate and tensile loading of a film deposited on a
polyimide substrate. The stress distributions are generally found to be very sensitive to the imposed type of loading. For small grain aspect ratios, analytical expressions for the stress distribution in a polycrystalline film with a (001) fiber texture are presented. When plastic behavior is considered, a structural hardening effect that has the appearance of a non-linear kinematic hardening is observed. A new orientation dependent hardening law which cause the hardening to scale with elastic anisotropy is proposed. The proposed hardening law is demonstrated on a film with small grain aspect ratio.

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6. References

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