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Tailoring the interface between dielectric and 4H-SiC by ion implantation

Sethu Saveda Suvanam^a*, David. M. Martin^b, Carl-Mikael Zetterling^c
and Anders Hallén^d

KTH Royal Institute of Technology School of Information and Communication technology, SE 164
40 Stockholm-Kista, Sweden.

^asuvanam@kth.se, ^bdavidmar@kth.se, ^cbellman@kth.se, ^dahallen@kth.se

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Abstract. In this paper, the effect of carbon (C), silicon (Si) and nitrogen (N) implantation on the interface properties of 4H-SiC/SiO₂ and the implications for 4H-SiC bipolar junction transistors (BJT) passivation are discussed. 4H-SiC epi-layer have been implanted with ¹²C, ¹⁴N and ²⁸Si ion at three different doses with energies of 3, 3.5 and 6 keV, respectively, resulting in a projected range of 8 nm for the three ions. Then metal oxide semiconductor (MOS) structures with SiO₂ as dielectric have been fabricated. Capacitance voltage measurements show an increase in the negative fixed charges for all the implanted samples as a function of implantation induced damage. Similarly, in the case of C and Si, the surface roughness increases as a function of dose and the mass of the ions. No reduction of D_{it}s due to the implantations is seen for any of the ions. Furthermore, TCAD device simulations of npn bipolar junction transistors (BJT), using the interface and fixed charges extracted from CV measurements, show a way to further optimize current gain and breakdown properties for the BJT.

Introduction

Previous studies on the effects of various surface passivation for bipolar devices have shown that plasma enhanced chemical vapour deposition (PECVD) oxide with N₂O annealing give the best current gain of BJTs due to a reduction of the density of interface states (D_{it}). However, these devices suffer from lower breakdown voltage due to the presences of fixed oxide charges, which strongly affects the design of the high-voltage junction termination extension (JTE) [1]. Various methods have been used to reduce the presences of high density of surface states at the interface of SiO₂/4H-SiC [2, 3], for instance the use of N implantation at the interface of thermally grown SiO₂/4H-SiC. F. Ciobanu et al. [3] have shown an improvement in D_{it} by three orders of magnitude with values ranging from 10¹⁰ cm⁻² eV⁻¹, besides introducing a dose dependent high amount of positive fixed charges. No such studies exist on PECVD-deposited SiO₂, but selectively tailoring the fixed charges of PECVD SiO₂ using ion implantation at the JTE could also result in an improvement of the breakdown voltage without compromising on the forward current gain (β). Here we have used low energy C, Si and N ions to tailor the interface of SiO₂/4H-SiC prior to the dielectric deposition to study the influence of chemical and structural effects on electrical device data.

Fabrication

The MOS structures are fabricated on 4° off-axis 4H-SiC wafers with a nitrogen doped n-type epi-layer of 14 μm thickness and doping concentration of 8×10¹⁵ cm⁻³. First, a standard (7 up + IMEC) cleaning procedure was used to clean the samples. Then 150 nm thick nickel contact was evaporated for back contact and annealed by rapid thermal annealing (RTA) at 950 °C for 1 minute. As shown in the Table 1, the samples were implanted with three ion species ¹²C, ¹⁴N and ²⁸Si with

energies 3, 3.5 and 6 keV, respectively, at the Ion Technology Centre, Uppsala. The energies were selected to give the same projected range in SiC [7]. Silicon and carbon were implanted with the fluence of $1 \times 10^{12} \text{ cm}^{-2}$ (low), $1 \times 10^{13} \text{ cm}^{-2}$ (medium) and $1 \times 10^{14} \text{ cm}^{-2}$ (high), whereas nitrogen was implanted with only one fluence of $1 \times 10^{13} \text{ cm}^{-2}$. Prior to the oxide deposition all the samples were cleaned using weak RCA-1 (100 ml NH_4 : 2 l DI H_2O : 400 ml H_2O_2 solution at 60 °C) and finally dipped in HF solution to remove the native oxide. SiO_2 was deposited at 300 °C using plasma enhanced chemical vapour deposition (PECVD) in two steps: in the first step, 15 nm SiO_2 was deposited with high rate followed by rapid thermal annealing (RTA) in N_2O for 5 minutes at a temperature of 1150 °C. Then, in a second step, 27 nm of SiO_2 was deposited at 300 °C with low rate and annealed in RTA for 30 sec. at a temperature of 1100 °C in N_2O to obtain a high quality SiO_2 layer. Finally, a 150 nm thick aluminium layer was deposited and patterned as circular top contacts with diameters of 100, 150 and 200 μm . The samples were characterized by capacitance voltage (CV) measurements and atomic force microscopy (AFM).

Results and Discussions

Fig. 1. CV measurements of MOS structures consisting of reference and implanted samples with ^{12}C , ^{14}N and ^{28}Si at different doses. The arrow indicates the increase in negative charges due to ion implantation.

Figure 1 show the CV curves of the un-implanted reference sample and samples implanted with ^{12}C , ^{14}N and ^{28}Si at different doses and the extracted flatband voltage (V_{fb}) and D_{it} are shown in Table 1. The flatband voltage shifts towards a positive voltage as a function of dose for all the implanted samples in comparison to reference sample B_0 . This shift in V_{fb} signifies an increase in the negative charges. These charges could exist either in the near interface oxide, or in the top-most SiC region created by the implantation damage, or a combination of both. The sign is opposite to the previously described positive charge introduction in grown oxides by N implantation [3]. The V_{fb} increase scales as a function of the atomic mass in

case of ^{12}C and ^{28}Si , i.e., sample B_1 having the lowest V_{fb} shift (doubled) and sample B_6 having the highest V_{fb} , about 10 times higher. In contrast, the lowest V_{fb} for the medium dose was recorded for B_7 using N implantation. It is known that during post oxide annealing (POA), implanted N atoms at the interface diffuse into the oxide and it may be the presence of this N in the oxide bulk that reduces the effective fixed charges, thus reducing the V_{fb} [4, 5]. Surface roughness, which can be

Table 1. Samples and implantation parameters (Column 1-5). Flatband voltage and density interface states extracted from Fig. 1 for different implantations (Column 6-7). Surface roughness of SiO_2 deposited on the implanted samples extracted from AFM measurements (Column 8).

Sample #	Fluence (cm^{-2})	Implanted Ion	Implantation Energy (keV)	Projected range in SiC (nm)	Flatband Voltage (V)	Density interface states (cm^{-2})	Surface Roughness (nm)
B_0	--	--	--	--	0.78	4×10^{11}	2.9
B_1	1×10^{12}	Carbon	3	7.7	1.6	6.5×10^{11}	1.6
B_2	1×10^{13}				4.2	1.7×10^{12}	3.1
B_3	1×10^{14}				>30	No data	6.5
B_4	1×10^{12}	Silicon	6	7.6	3.2	1.3×10^{12}	3.4
B_5	1×10^{13}				8.8	2.5×10^{12}	7
B_6	1×10^{14}				>30	No data	12
B_7	1×10^{13}	Nitrogen	3.5	7.7	3.4	2.2×10^{12}	7.3

seen in Table 1 as measured by atomic force microscope (AFM), scales with the ion induced damage, i.e. ion dose and mass, for both ^{12}C and ^{28}Si implanted samples. Figures 2a and b shows the density of interface states extracted from the CV measurements and surface roughness extracted from AFM, as a function of the total number of vacancies produced in the SiC calculated by SRIM [7], respectively. The solid and dashed lines show the trend for carbon and silicon implanted structures, respectively. A point for nitrogen, medium dose (B_7) is also included. It could be observed that the variations in both electrical and surface topography are scaled in accordance with the damage produced. Furthermore, when plotted as a function of damage the previously reported positive effect of nitrogen is not seen in this investigation. In fact, it seems that it is the carbon implanted samples that sticks out, both in terms of lower D_{it} and smoother surfaces.

Fig. 2. a) Density interface states b) surface roughness as a function of total number of vacancies per unit area produced in the 4H-SiC for various implantations. Solid and dashed lines show the change in both surface roughness and D_{it} s for various doses of carbon and silicon implanted structures, respectively.

Simulation

In order to understand the effects of tailored SiO_2 surface passivation on the performance of the npn transistors, 2D-TCAD device simulation [8] have been utilized. A cross section of the device used for this simulation is shown in Fig. 3a. The physical models used in the simulations are described in Ref. [1]. The concentration of the interface traps and negative charges have been added in the models using the values extracted from the CV measurements. The values have been implemented for both the JTEs in Dielectric Region 2 (see Fig. 3a) and the breakdown voltage (V_{BD}) is then extracted at the point where the ionization integral equals 1. Since Dielectric Region 1 has a direct influence on the transistor current gain, β , it is crucial to have a dielectric with low D_{it} , i.e., passivation with no implantation (B_0).

Simulated breakdown voltage, V_{BD} , shows an improvement of 4% (3404 V) and 11% (3611 V) for C-low and C-medium dose, respectively, with respect to the reference sample (3266 V). In contrast to the ^{12}C implantation, ^{28}Si implanted samples showed an increase in V_{BD} by 6.3% (3473 V) for the low dose, whereas for the medium dose V_{BD} decreased by 17% (2714 V) with respect to B_0 . Finally, the ^{14}N implanted sample show an increase of 5.6% (3450 V) as compared to B_0 . An understanding in the variation of V_{BD} can be comprehended from the electric field distribution in the JTEs. Figure 3b shows the TCAD simulated electric field distribution along the line LL' in Fig. 3a for various samples at a reverse voltage of 2.875 kV. The increase in negative charges by the implantation shifts the peak of the electric field distribution from JTE 1 to JTE 2, resulting in an improvement of V_{BD} in comparison to an unimplanted reference. For too large amount of negative charge the field reduction at JTE 1 is, however, compensated by a field increase at JTE 2, which results in an earlier breakdown, as is seen in the Si low and medium case.

Fig. 3. a) Cross section of the BJT used for the TCAD device simulation [1]. b) Electric field distribution in the device along the line LL' at reverse voltage of 2.875 kV for various carbon and silicon implanted structures.

Conclusion

In summary, we have presented investigations on the effects of low energy ion implantation prior to oxide deposition on the 4 H-SiC/SiO₂ interfaces. CV measurements have shown an increase in negative charges in the oxide, or near oxide region due to ion implantation which scales as a function of the ion induced damage. When comparing C, N, and Si, as a function of induced damage, it appears that carbon ions gives the best properties, not nitrogen as previously reported by several authors. Computer simulations, using the data extracted from the CV measurements, indicate a possibility to tailor the interface charge and thereby improving the blocking properties of 4H-SiC BJT's without compromising the current gain.

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