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This is the accepted version of a paper published in *Materials Science Forum*. This paper has been peer-reviewed but does not include the final publisher proof-corrections or journal pagination.

Citation for the original published paper (version of record):

Lanni, L., Malm, B G., Östling, M., Zetterling, C-M. (2015)

ECL-based SiC logic circuits for extreme temperatures.

Materials Science Forum, 821-823: 910-913

<http://dx.doi.org/10.4028/www.scientific.net/MSF.821-823.910>

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<http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-183141>

ECL-based SiC logic circuits for extreme temperatures

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Keywords: High-temperature ICs, silicon carbide (SiC), bipolar junction transistor (BJT), ECL.

Abstract. Integrated digital circuits, fabricated in a bipolar SiC technology, have been successfully tested up to 600 °C. Operated with -15 V supply voltage from 27 up to 600 °C OR-NOR gates exhibit stable noise margins of about 1 or 1.5 V depending on the gate design, and increasing delay-power consumption product in the range 100 - 200 nJ. In the same temperature range an oscillation frequency of about 1 MHz is also reported for an 11-stage ring oscillator.

Introduction

Silicon carbide (SiC) devices can operate at extreme temperatures well beyond the limits of the traditional Si or SOI technology thanks to a much lower intrinsic carrier concentration. For this reason several integrated circuits (ICs) based on different SiC technologies have reported operating temperatures approaching 600 °C. JFET-based logic gates and analog circuits have been demonstrated up to 550 [1] and 600 °C [2], respectively. Bipolar ICs have shown similar operating temperatures. Specifically, OR-NOR gates [3] and a monolithic operational amplifier [4] fabricated in the same bipolar SiC technology have reported stable operation up to 500 °C. Using a standard aluminum-based metallization system, the increasing current gain reported for such technology above 300 or 400 °C shows promise for operation beyond 500 °C.

The aim of this work is to push the operating temperature of such bipolar technology to the metallization temperature limit. Operation of emitter coupled logic (ECL) based OR-NOR gates and 11-stage ring oscillators has been successfully verified from room temperature up to 600 °C.

Design and fabrication

Two different versions of an ECL-based OR-NOR gate, referred to as v1 and v2, were considered for this study. The gate design reported in [3], referred to as v1 in the following, was modified in order to enlarge the gate noise margins (NMs) from about 1 to 1.5 V leading to a similar design, referred to

as v2. The two designs, whose schematic diagram is shown in Fig 1 (a), consist of 10 BJTs and 11 integrated resistors and differ only in the resistance value of some resistors. Based on v2 an inverter was designed and used as fundamental stage for an 11-stage ring oscillator. As shown in Fig. 1 (b), it consists of a 2-input NOR gate, which acting as control stage allows enabling the oscillation of the entire circuit, and 10 inverting stages connected in a chain. A further inverting stage is used as output buffer. All integrated resistors were realized in the high-doped collector layer (see Fig. 2).

Figure 1 (a) OR-NOR gate schematic. (b) 11-stage ring oscillator block diagram.

Figure 2 Fabricated device cross-sectional view.

Discrete devices and integrated circuits were fabricated on 100 mm 4H-SiC wafers. The designed epitaxial structure, shown in Fig. 2, allows topside collector contact and isolation between different devices without ion implantation. Emitter, base and collector mesas were defined by means of reactive ion etching. After a dry sacrificial oxidation, surface passivation was performed by annealing 50 nm of deposited SiO₂ in N₂O. Ohmic contacts to n- and p-type SiC were formed with Ni and a triple layer of Ni/Ti/Al, respectively. Over-layer metallization for device contact and interconnects were realized based on a stack of Ti/TiW/Al. This metallization system imposes important limitations to the maximum operating temperature of both devices and circuits due to the use of Al as main metal, because of its relatively low melting point (about 660 °C), and of TiW as metal diffusion barrier. The TiW layer allows prolonged operation up to 500 °C avoiding intermixing of Al and Ni silicide at 400 °C and, hence, degradation of ohmic contacts to n-type SiC [5], but it is no longer stable above 500 °C [6].

Results and discussion

All measurements were performed by direct wafer probing on a temperature-controlled stage. All devices and circuits presented in this study belong to 3 pieces cut out from two 100 mm wafers.

Sheet resistance and specific contact resistance of emitter, base and high doped collector layer were estimated by means of transfer length measurements in the range 27-500 °C. The sheet resistance of all three layers exhibits a non-monotonous temperature dependence with a minimum around 200 °C for emitter and collector layer and between 300 and 400 °C for base layer. In the same temperature range the specific contact resistance of all layers slightly decreases for increasing temperature, remaining approximately equal to 10⁻⁶, 10⁻⁴ and 10⁻⁵ Ω·cm² for emitter, base and collector layer respectively. After a short exposure at 600 °C the room temperature specific contact resistance increased by approximately 5 and 8 times for emitter and collector layer, respectively. While no significant variation was observed for the base layer.

Figure 3 Current gain temperature dependence.

Device performance. In the range 27 - 600 °C the transistor current gain shows a non-monotonous behavior with a minimum around 400 °C (fig. 3), similarly to what has been previously reported for this technology [3] and predicted by simulation [7]. In the same temperature range the collector resistance, following the variations of the collector layer sheet resistance, exhibits a minimum at ~200 °C similarly to [3].

OR-NOR gates. The static behavior of the OR-NOR gates was tested by applying an input signal, swept between -10 and 0 V, at one input (A or B) leaving the other one open, with a supply voltage (V_{EE}) of -15 V. Voltage transfer characteristics (VTCs) measured up to 600

°C for OR and NOR output are shown in Fig. 4 (a)-(b) and (d)-(e) for v1 and v2, respectively; while related noise margins are given in Fig. 4 (c) and (f). As already reported in [3] for v1 the logic threshold and both OR and NOR output voltage levels move towards positive voltages when the temperature rises, resulting in stable NMs about 1 V from 27 up to 600 °C (see Fig. 4 (c)). Except for the low output voltage levels, similar temperature behaviors can be also observed for v2. Specifically, no significant changes occur above 100 °C for the OR output low logic level, while for the NOR output it increases only when the temperature rises from 500 to 600 °C. Nevertheless, stable NMs of about 1.5 V can be observed for v2 from 27 to 600 °C thanks to larger output voltage swings at each temperature (see Fig. 4(f)). Switching measurements were performed for both v1 and v2 up to 600 °C with V_{EE} = -15 V and an input signal having frequency of about 100 kHz and logic levels similar to those of the tested gate at the selected temperature (see Figs. 5 (a) and (b)).

Figure 4 Measured static characteristics at different temperatures for v1 (a)-(b) and v2 (d)-(f). Temperature dependence of related low (NM_L) and high (NM_H) noise margins for v1 (c) and v2 (f).

The frequency of the input signal was set at 100 kHz since this value is consistently lower than the maximum frequency at which the gates can operate. As will be shown in the next section, an 11-stage ring oscillator fabricated on the same wafer oscillates with a frequency of approximately 1 MHz. At each temperature OR and NOR outputs of both v1 and v2 exhibit asymmetric propagation delays, with low-to-high transitions faster than the high-to-low ones and increasing propagation delays above 100 or 200 °C (see Fig. 5 (c)). The temperature dependence of both propagation delay and total current consumption is mainly determined by changes in bias currents throughout the circuits [3], which tracking the temperature variations of resistor resistance depend on changes in the collector layer sheet resistance. An unexpected increase in total current consumption occurred at 600 °C, likely due to degradation of the metallization system and/or n-type ohmic contact. For both gates the delay-power consumption product monotonically increases in the range 27 – 600 °C: from 90 to 150 nJ and from 100 to 220 nJ for v1 and v2, respectively. Such values are similar to those reported in [3] for the same technology. The lower propagation delay and higher power consumption of v1 can be related to the lower resistance values selected for some of the resistors.

Figure 5 Dynamic performance of the OR-NOR gate v1 and v2 up to 600 °C. (a) - (b) Switching waveforms (V_{EE} = -15 V and f_{in} = 100 kHz). Dashed lines represent the input voltage, solid lines the output voltage. (c) Propagation delay and total current consumption temperature dependence.

Figure 6 ECL-based 11-stage ring oscillator: optical image.

Figure 7 Performance of the ECL-based 11-stage ring oscillator in the range 27-600 °C ($V_{EE} = -15$ V). (a) Output characteristics. (b) Propagation delay of a single stage and total current consumption.

was observed for both propagation delay and total current consumption (see Fig. 7 (b)).

Summary

The operating temperature of bipolar SiC integrated circuits has been extended to 600 °C. Integrated OR-NOR gates and 11-stage ring oscillator have been fabricated and successfully tested from 27 up to 600 °C. In order to allow reliable circuit operation at such extreme temperatures and even higher operating temperatures a suitable metallization system has to be developed.

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11-stage ring oscillator.

This circuit, whose optical images is shown in Fig. 6, is able to oscillate in the entire temperature range with an oscillation frequency of about 1 MHz in the range 27-500 °C that decreases to 0.6 MHz at 600 °C (see Fig. 7 (a)). Nevertheless, compared to the gate v2 a reduced output voltage swing can be observed at each temperature. This can be related to the fall times of the NOR output that being longer than half of the oscillation period prevent each stage from settling the nominal high or low output voltages. In the range 27 – 600 °C the expected temperature dependence