WIDE TEMPERATURE RANGE THROUGH SILICON VIAS MADE OF INVAR AND SPIN-ON GLASS FOR INTERPOSERS AND MEMS

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ABSTRACT

Through silicon vias (TSVs) are used e.g. to create electrical connections through MEMS wafers or through silicon interposers used in 2.5D packaging. Currently available technologies do not address situations in which TSVs through unthinned wafers have to withstand large temperature variations. We propose using ferromagnetic Invar metal alloy for this purpose due to its low mismatch in heat induced strain in comparison to silicon. We demonstrate the suitability of a magnetic assembly process for Invar TSV fabrication and the use of spin-on glass as a TSV insulator. We demonstrate TSVs, with contact pads, that tolerate temperature cycling between -50 °C and 190 °C and can withstand elevated temperatures of at least up to 365 °C.

INTRODUCTION

Through silicon vias (TSVs) are used in 3D integration to electrically connect vertically stacked chips. In 2.5D integration, TSVs are utilized in silicon interposers which can be placed between stacked chips to reroute contacts and ease thermal control [1]. A high-density redistribution layer also allows chips to be placed side by side on top of the interposer [1]. This packaging solution offers shortened signal paths between heterogeneous dies, such as MEMS, application specific ICs and passives, on a common interposer substrate. This paper specifically aims to demonstrate a TSV structure reaching through unthinned wafers and being applicable to systems undergoing large temperature variations such as those in automotive environments where temperatures can range between 200 °C [2] and very low ambient temperatures. TSVs through unthinned wafers are needed for rigid interposers so that an additional organic package substrate is not necessary for support [3] and complicated thin wafer handling is avoided. In addition, long TSVs allow electrical connections through thick MEMS device or capping wafers [4] when necessary.

MATERIALS

TSVs typically use electrochemically deposited (ECD) copper as a conductive material [5]. The large mismatch of the coefficients of thermal expansion (CTE) between copper and silicon can lead to TSV failures [6]. Embedded copper increases the interposer's global CTE [7]. This can result in a thermal expansion mismatch between the interposer and mounted chips, thereby causing strain to the microbumps connecting them [7]. CTEs can be presented either in instantaneous or mean formats. Mean CTE refers to the average value of the CTE between a reference temperature and the current temperature whereas instantaneous CTE refers to the actual rate of the change of strain at each temperature [8]. Instantaneous CTEs of different materials are presented in Figure 1 as a function of temperature. The reference temperatures of the instantaneous CTE curves for silicon [9], copper [10], tungsten [11] and Invar (curve range from -193.15 °C to 26.85 °C) [12] have been moved to 25 °C. As can be seen from Figure 1, tungsten has a significantly better matched CTE with silicon than copper has. However, chemical vapor deposited tungsten suffers from high film stress and wafer bow [5], thereby limiting tungsten film thicknesses to few microns [13] meaning that tungsten can only be used in small TSVs [5].

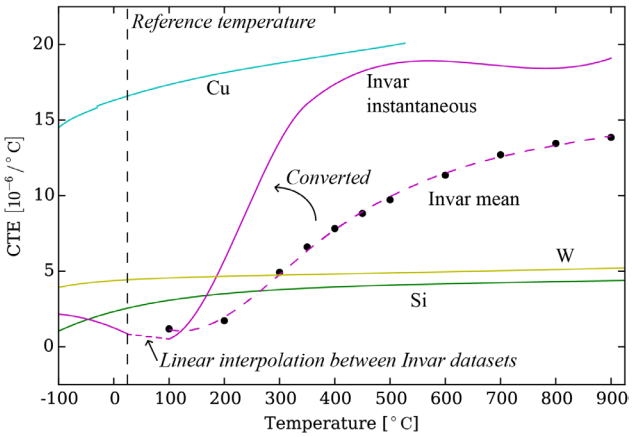

Figure 1: Instantaneous CTEs of different materials together with a fit to Invar's mean CTE data for temperatures above 100 °C. The reference temperature is set to 25 °C. Figure is based on experimental data [9, 10, 11, 12, 14].

Invar metal alloy (Ni 36%, Fe 64%) has a low instantaneous CTE near room temperature as can be seen from Figure 1. In contrast to the other materials and Invar below 26.85 °C, CTE data points [14] for Invar above 100 °C are given as a mean CTE instead of instantaneous CTE. A third order piecewise polynomial fit using the least squares method was done to obtain a curve representing this data. The resulting polynomial coefficients are shown in Table 1. The resulting mean CTE curve has been converted [8] to instantaneous CTE. Both are plotted in Figure 1. A gap in Invar CTE data exists between 26.85 °C and 100 °C. It was filled with an interpolating line connecting the two datasets. The line is shown in Figure 1 and the line parameters are presented in Table 1. Thermally induced length changes in Invar around room temperature are minimal [14] and therefore low and linear CTE behavior in this range is a reasonable assumption.

Instantaneous CTE curves in Figure 1 were integrated using 25 °C as an integral starting point. Integral values

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represent the strain of each material and 25 °C is the strain free temperature. The strain of silicon was subtracted from other strains in order to extract strain mismatches between silicon and different metals. The results are plotted in Figure 2. Invar and tungsten have comparable strain mismatches to silicon at temperatures below 297 °C and Invar is superior over copper in the full temperature range.

Table 1: Invar CTE curve parameters for a polynomial of the form $a+bT+cT^2+dT^3$.

	26.85 °C - 100 °C	100 °C - 350 °C		350 °C - 900 °C	
	Inst.	Mean*	Inst.	Mean*	Inst.
a	$9.242 \cdot 10^{-1}$	4.242	5.673	$-1.070 \cdot 10^{1}$	$-1.247 \cdot 10^{1}$
b	$-4.108 \cdot 10^{-3}$	$-5.722 \cdot 10^{-2}$	$-1.291 \cdot 10^{-1}$	$7.085 \cdot 10^{-2}$	$1.453 \cdot 10^{-1}$
c		$2.934 \cdot 10^{-4}$	$9.036 \cdot 10^{-4}$	$-7.275 \cdot 10^{-5}$	$-2.203 \cdot 10^{-4}$
d		$-3.213 \cdot 10^{-7}$	$-1.285 \cdot 10^{-6}$	$2.715 \cdot 10^{-8}$	$1.086 \cdot 10^{-7}$

*The mean CTE value of 11.18 from H. Harada *et al.* [14] for the first data point was interpreted to be a typographical error and 1.18 was used instead on the basis of other datasets and figures in the same source.

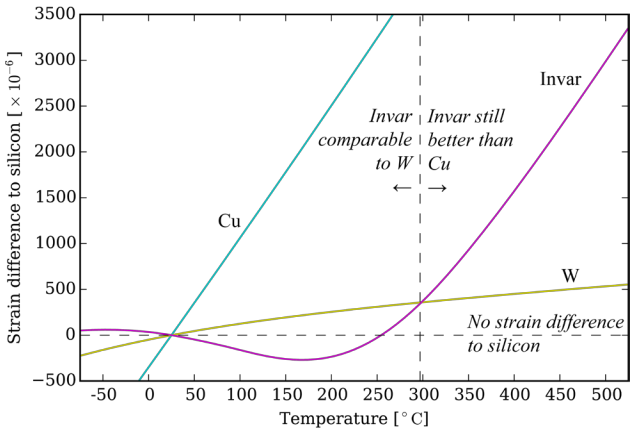

Figure 2: Strain mismatches between TSV metals and silicon.

FABRICATION

Invar TSVs were fabricated using a magnetic assembly method [15, 16] which allows using Invar as a TSV conductor without the need for a challenging ECD process development [5] as has been pursued for copper to achieve void free TSVs. In magnetic assembly, voids are not a problem since inherently void free Invar wire is used as a starting material for TSV cores. The fabrication process started by cutting Invar wire (California Fine Wire Co., USA) to rods to be later assembled into holes in a device wafer. Invar wires with a diameter of 45 µm were placed on a silicon carrier wafer and embedded in a thick photoresist layer by spin-coating. The wires were cut to 320 µm long rods using a dicing saw. Burrs at the ends of the Invar rods that were caused by the dicing process were removed by etching in $FeCl_3$ (3.5 mol/L) for 30 s while the rods were still embedded in the photoresist. The photoresist was stripped in acetone and the Invar rods were collected using a magnet.

The TSV fabrication process is illustrated in Figure 3. A 300 µm thick silicon wafer is thermally oxidized and the SiO_2 layer on the top side of the wafer is patterned using reactive ion etching (RIE) to create circular openings with a diameter of 55 µm and a pitch of 350 µm (Figure 3a). The patterned SiO_2 layer is used as a hard

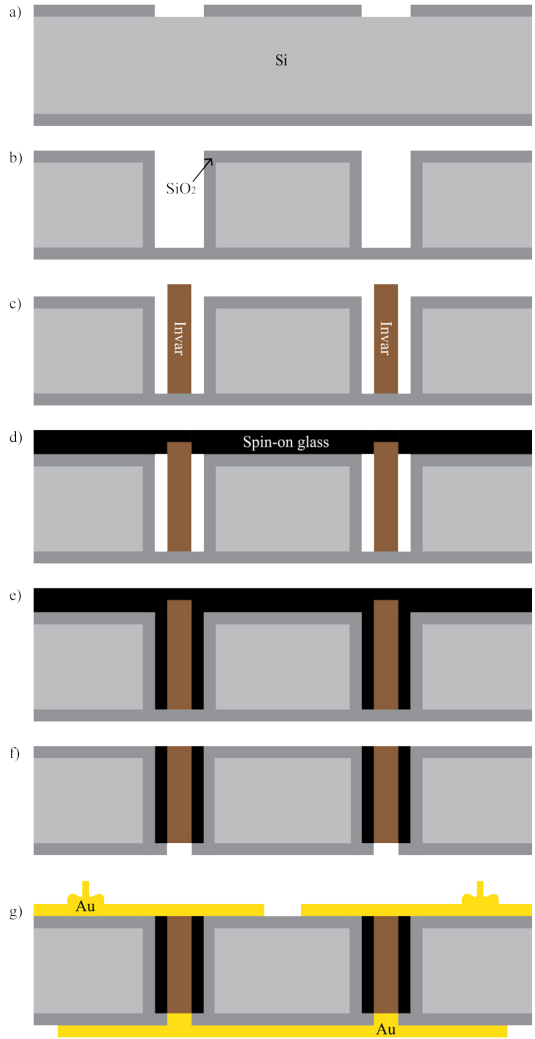

Figure 3: Schematic presentation of the magnetic assembly and integration of the TSV Invar rods. a,b): Creation of TSV holes. c): Assembly of Invar rods using a magnet. d,e): SOG filling. f): Opening backside oxide and top side grinding. g): Metallization, patterning and wire bonding.

mask for DRIE creating the TSV holes. The DRIE process is stopped at the SiO_2 on the backside of the wafer. The wafer goes through another thermal oxidation cycle in order to remove the passivation layer left behind by DRIE process on the TSV-hole sidewalls and to oxidize these sidewalls for improved isolation between the wafer and the TSVs (Figure 3b). The Invar rods are spread on the wafer and pulled inside the TSV holes by moving a permanent magnet underneath the wafer (Figure 3c). A spin-on glass (400F, Filmtronics Inc., USA) layer with a thickness of several millimeters is drop-casted on top of the wafer (Figure 3d). A vacuum treatment at 0.2 bar for 10 minutes drives out trapped air between the Invar rods and the TSV sidewalls allowing the spin-on glass (SOG) to fill the gap without voids (Figure 3e). The SOG is baked in an ambient atmosphere at a temperature of up to 250 °C. The SiO_2 membrane covering the TSV holes on the backside of the wafer is removed using RIE. Excess SOG and protruding ends of the Invar rods are removed from the top side by grinding (Figure 3f). TiW/Au layers (50 nm / 504 nm) are sputtered on both

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sides of the wafer. Both sides are patterned in order to create TSV pairs where two TSVs are connected in series (Figure 3g).

Figure 4 shows a cross sectional view of the top left corner of a single TSV demonstrating void-free SOG filling between the Invar rod and the TSV sidewall. The wafer was diced and five chips were attached to ceramic chip carriers using high temperature glue (930-4, Epoxy Technology Inc., USA) and gold wire interconnect bonding.

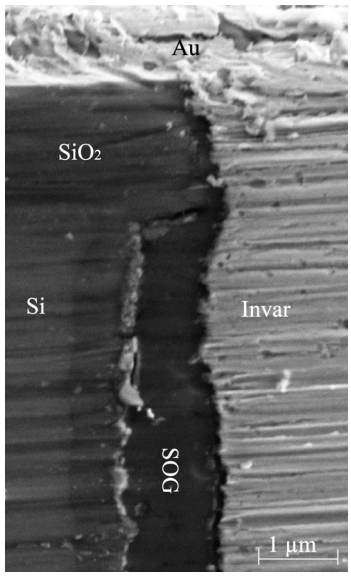

Figure 4: SEM image showing a cross section of the top left corner of a single TSV. The top gold metallization layer is connecting the top end of the Invar rod. The Invar rod is separated from the TSV sidewall by a SOG layer. The SiO_2 can be seen on top of Si and on TSV sidewall.

CHARACTERIZATION AND RESULTS

The TSV performance was investigated by measuring the changes in resistance after temperature cycling and after elevated temperature treatments. Since two-point resistance measurements were used, all the measurement values include resistances from wire bonds and package leads. In order to measure a single TSV resistance, four-point resistance measurements were done for four TSV pairs after they had undergone all cycling and elevated temperature treatments. The lowest value obtained from these measurements for a TSV pair was 569 mΩ, giving a nominal single TSV resistance of 285 mΩ. This is reasonably close to the expected value of 141-160 mΩ obtained using the Invar rod dimensions and a resistivity of 750-850 nΩ·m [17] for Invar metal alloy. The difference to the expected value presumably originates from contact resistances between TiW/Au metallization layers and the Invar rods.

The test chips were temperature cycled 100 times between -50 °C and 190 °C with a typical cycle taking 66 minutes. The temperature range was limited by the characterization setup and does not necessarily represent the widest range the TSVs can tolerate. The verified working range is wider than the largest cycling range of from -65 °C to 150 °C reported in the literature [18] for a complete TSV structure with surface metallization for electrical characterization. In addition, achieving tolerance for such a large temperature variations in our 20 times longer TSVs is more demanding than in the short TSVs [5].

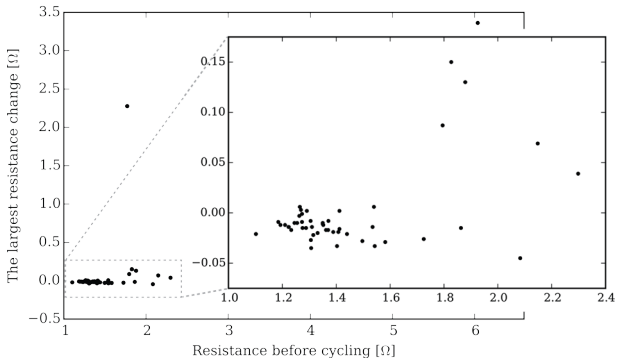

Figure 5: The maximum resistance deviation as a result of thermal cycling versus the initial resistance. A single TSV pair that failed during testing is not shown.

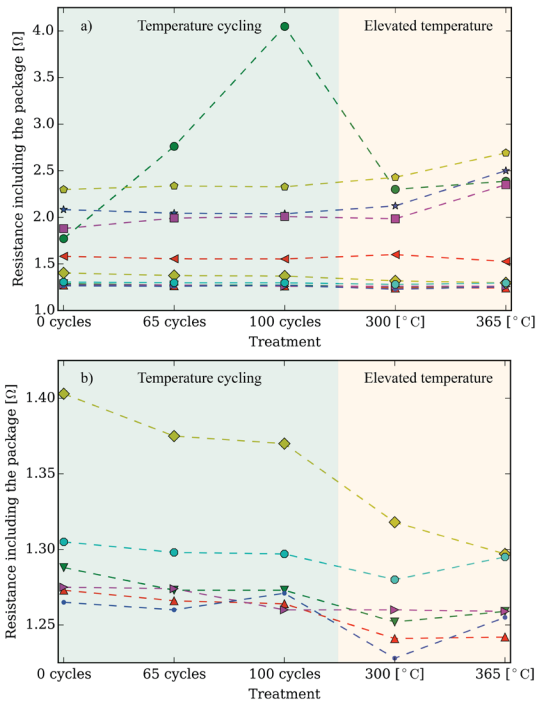

Figure 6: Resistance evolution of TSV pairs a) on a single chip and b) a close-up to the lower resistance pairs on the same chip. Temperature treatments are divided into thermal cycling and elevated temperature treatments.

Resistances of all 51 TSV pairs were measured before temperature cycling, after 65 cycles, and after 100 cycles. Figure 5 shows the largest change from the original resistance, whether after 65 or 100 cycles, for each TSV pair together with their original resistances. One TSV pair with an initial resistance of 2.052 Ω failed before 65 cycles and is not included in Figure 5. TSV pairs with an initial resistance below 1.6 Ω show the maximum resistance increase of 6 mΩ and the maximum decrease of 35 mΩ. As most of these pairs decrease in resistance as a response to cycling, it is possible that resistance stability would have benefitted from an

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annealing step at the end of the TSV fabrication process.

One chip containing 11 TSV pairs was further exposed to elevated temperatures in order to establish the available temperature budget in the later processing steps. First, the chip was heated to 300 °C during 11 minutes and kept at this temperature for one hour, followed by a slow cooling to room temperature taking several hours. Subsequently, the chip was heated to 365 °C during 18 minutes and kept at the elevated temperature for one hour followed again by slow cooling. It should be noted that 365 °C does not necessarily represent the maximum tolerable temperature for our TSVs. Figure 6 presents the resistance data of the TSVs on this chip. It can be observed that the TSVs with low initial resistances show more stable behavior during cycling and elevated temperatures than the TSVs with higher initial resistance.

CONCLUSIONS

Analysis of CTEs and mismatch strains of different metals in comparison to silicon shows that Invar metal alloy is a viable option for metallization of TSVs exposed to high thermal stresses. A magnetic assembly process was adapted to realize void-free metal TSV cores made of Invar without the process optimization required by ECD. SOG can be used as a void-free high-temperature-resistant filling and insulation layer in TSVs fabricated using the magnetic assembly method. Fabricated structures show variation in their initial resistance, likely due to differences in contact resistance between Invar and horizontal metallization layers, but the TSVs with low initial resistance have relatively stable resistance behavior under stress from thermal cycling. Notably, changes are mainly towards lower resistances opening a possibility for further process optimization by adding an annealing step at the end of the fabrication cycle. A tolerable temperature of at least 365 °C is established for the proposed TSVs.

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