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4.5-kV 20-mΩ.cm² Implantation-Free 4H-SiC BJT with Trench Structures on the Junction Termination Extension

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Abstract. A single-mask junction termination extension with trench structures is formed to realize a 4.5 kV implantation-free 4H-SiC bipolar junction transistor (BJT). The trench structures are formed on the base layer with dry etching using a single mask. The electric field distribution along the structure is controlled by the number and dimensions of the trenches. The electric field is distributed by the trench structures and thus the electric field crowding at the base and mesa edges is diminished. The design is optimized in terms of the depth, width, spacing, and number of the trenches to achieve a breakdown voltage (V_B) of 4.5 kV, which is 85% of the theoretical value. Higher efficiency is obtainable with finer lithographic resolution leading to smaller pitch, and higher number and narrower trenches. The specific on-resistance (R_{ON}) of 20 mΩ.cm² is measured for the small-area BJT with active area of 0.04 mm². The BV - R_{ON} of the fabricated device is very close to the SiC limit and by far exceeds the best SiC MOSFETs.

Introduction

Silicon carbide (SiC) is one of the most promising materials for high voltage and high power electronics due to its marvelous electrical properties such as high critical electric field, low intrinsic concentration, and high saturation velocity. Among different type of power devices, SiC bipolar junction transistors (BJTs) attract interests for high power electronics due to the fast switching speed, low on-resistance, and high blocking voltage (V_B) [1,2]. In spite of these advantages, the fabrication processes still need refinement and optimization. Process steps such as lithography, etching, and doping concentration of SiC layers still have undesirable variations. In recent years, with the maturity of the SiC wafer growth, higher breakdown voltages were achieved by having a thicker low-doped drift layer. However, it is yet important to increase the efficiency of the termination technique in order to reduce the area of the termination to increase the yield and to make it cheaper for industrial applications. Moreover, a reasonable current gain (β) and a high current density (J_C) are required in power applications. The current density can be increased by having more emitter fingers, however the current gain highly depends on the base-emitter distance [3]. Therefore, for a fixed area, there is always a trade-off between the current gain and current density which should be considered in the device design. Also, a low specific on-resistance (R_{ON}) is required to reduce the power loss during switching. Several high voltage SiC devices have been reported where the junction termination extension (JTE) is formed by using ion implantation [4-10]. However, ion implantation with the mandatory following high-temperature annealing increases the number of defects which may severely decrease the current gain (β) and reliability of the device under stress conditions [11,12]. Implantation-free devices with very low R_{ON} have been reported which have been fabricated by dry etching and lift-off processes to avoid using ion implantation [13-18]. The former devices degrade with increased on-resistance and current capability because of the implantation defects, while the latter have large deviation from the ideal V_B mainly because of variations in the etching and doping process steps as well as the misalignments. Hence there is a drive to find simple methods to reduce the processing variations. Therefore, in this paper a single-mask junction termination extension is designed and demonstrated to realize a 4.5 kV implantation-free 4H-SiC BJT for high voltage applications. The fabricated structure has a number of trenches on

Fig. 1. Schematic cross-sectional view of the fabricated BJT with trench structures on the p-base layer.

Fig. 2. (a) Optical microscopic image of photoresist mask to form the trench structures. (b) scanning electron microscopic (SEM) image of the trench structures.

the p-base layer which modifies the electric field distribution along the surface of the device. The structure is implemented in the Sentaurus two-dimensional (2-D) TCAD device simulator [19]. The simulator is calibrated with our experimental data and a good agreement is achieved. By employing simulation, device design is optimized in terms of the remaining dose of the JTE, and the depth, number, and scaling of the trenches.

Results and Discussion

Fig. 1 represents the schematic cross-sectional view of the BJT with the trench structures. The junction termination extension is realized by one lithographic step. Although it was found by the simulations that smaller trench widths and higher number of trenches result in better modulation of the surface electric field, it is recommended to have wider openings and less number of trenches due to the uncertainties in the process steps. A 100-mm 4H-SiC substrate with five epilayers including an n-buffer layer ($\sim 18 \mu\text{m}$, $1 \times 10^{18} \text{ cm}^{-3}$), n-drift layer ($45 \mu\text{m}$, $1.7 \times 10^{15} \text{ cm}^{-3}$), p-base layer ($0.76 \mu\text{m}$, $2.5 \times 10^{17} \text{ cm}^{-3}$), n-emitter layer ($2 \mu\text{m}$, $1 \times 10^{19} \text{ cm}^{-3}$), and n^+ -cap layer ($0.2 \mu\text{m}$, $3 \times 10^{19} \text{ cm}^{-3}$) on top of the starting material. Inductively coupled plasma (ICP) etching with 5% over-etching with a patterned hard mask of SiO_2 is used to form the emitter (first mask) and deep mesa structure (second mask). Due to the sensitivity of the JTE dose and trench depth, multi-step reactive ion etching (RIE) is employed to form the trench structures (third mask). Fig. 2a illustrates the optical microscopy image of the photoresist mask used to pattern the trench structures with the depth of 300 nm. The minimum width of the trenches is limited by the lithography resolution and the etching method. Fig. 2b shows the scanning electron microscopy (SEM) image of the trench structures. All trenches have the same depth without any further etching variation and probable misalignments caused by fabrication process or extra lithography steps. Other process steps including oxide etching and metallization are quite similar to the implantation-free BJTs [14,18]. It has been reported that the presence of the charges at the interface of the JTEs affects the breakdown voltage of the SiC BJTs [20]. Thus by considering the positive charges ($4.5 \times 10^{11} \text{ cm}^{-2}$) for the SiO_2/SiC interface, the JTE remaining dose of $1.3 \times 10^{13} \text{ cm}^{-2}$ is chosen by the simulation. It is worth noting that the trench structures can be realized with a single mask. This reduces the number of lithographic levels, diminishes the effect of variation in the etching processes, makes it cheaper, and eliminates any further risk of misalignment. The active area of the device is 0.04 mm^2 and the total area of device with the junction termination extension is about 0.5 mm^2 .

Fig. 3 presents the (I_C - V_C) characteristic of the small-area BJT device. The emitter of the device has interdigitated fingers which has higher current density. The majority of the current is carried by the fingers. A maximum current gain of 35 at $I_C = 150 \text{ mA}$ ($J_C = 375 \text{ A/cm}^2$) is achieved. The R_{ON} of $20 \text{ m}\Omega \cdot \text{cm}^2$ is measured at a collector current of 0.1 A. It is worth noting that the current gain can be improved with optimized passivation techniques [20,21]. The maximum breakdown voltage of 4.5 kV is achieved at a leakage current of 0.1 μA , which is 85% of the theoretical value.

Fig. 3. Measured I_C - V_C forward and reverse characteristics of the fabricated BJT. The device active area is 0.04 mm^2 .

Fig. 4. The simulated electric field distribution along the fabricated BJT compared with conventional JTE structures at reverse voltage of 4.5 kV.

As it is mentioned earlier, higher efficiency is achievable with finer lithography which results in higher number and higher density of trenches. This improves the electric field spreading along the device that improves the breakdown voltage. However, depending on the available lithography and etch technology it is recommended to not design too narrow trenches because of process variations.

A high electric field can lead to higher leakage current and premature breakdown at the surface of the device. Fig. 4 compares the simulated electric field distribution of the fabricated BJT with single- and double-JTE for the applied reverse voltage. A severe electric field crowding occurs at the base and mesa edges for high and low dose of the JTE, respectively. Apparently, the electric field is suppressed by the influence of the trench structures. Simulation results show that the high electric field is distributed efficiently into the trenches and reduces the peak at the edges. Therefore, one can expect that a more uniform electric field distribution can be achieved by squeezing the trench size and adding more trenches.

The comparison between the performance of the fabricated device and the recent reported BJTs with different termination techniques are summarized in Table I. Even though the breakdown voltage is in the mid-range, the termination efficiency of the device is among the highest values. It means that higher breakdown voltage is achievable by employing the same termination technique on a thicker drift layer with lower doping concentration without increasing the JTE length. Moreover, compare to the other counterparts the termination is realized with a single-mask lithography. This makes it cheaper and simpler to fabricate as well as tolerant to fabrication process variations such as misalignment and etching variation. The current gain of the device is reasonable and can be improved by enhanced passivation techniques [21]. Also the on-resistance is in the low-range that can significantly reduce the power loss. These results confirm the device performance for high voltage and high power switching applications.

Summary

An implantation-free single-mask junction termination extension (JTE) with trench structures is formed to demonstrate a 4.5 kV 4H-SiC bipolar junction transistor (BJT). Compared to conventional termination structures with multi-step etchings, only a single-step etching with one mask to form the trench structures is needed. A more uniform electric field

Table I. Comparison between the performances of the fabricated structure with the recent reported power BJTs.

Reference	V _B (kV)	R _{ON} (mΩ.cm ²)	Gain	Termination Efficiency (%)
[4]	1.8	10.8	20	58
[5]	3.2	28	20	60
[6]	1.6	4.5	27	—
[7]	6	28	--	> 90
[8]	1.8	4.4	40	—
[9]	10.5	110	75	91
[12]	23.5	321	63	78
[13]	9.2	49	7	—
[14]	2.7	12	50	—
[15]	1.3	11	31	—
[16]	2.3	4.5	35	85
[17]	1.8	2.8	117	—
[18]	2.8	4.5	55	75
This work	4.5	20	35	85

distribution is obtained by forming the trenches which modifies the field crowding at base and mesa edges. A breakdown voltage of 4.5 kV is measured, which is 85% of the theoretical value. The specific on-resistance (R_{ON}) of 20 mΩ.cm² is achieved for the small-area BJT with an active area of 0.04 mm². The V_B-R_{ON} of the fabricated device is very close to the SiC limit. The performance comparison of the fabricated device with the recently reported BJTs proves its ability for high power switching applications.

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