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A Dual-Output Thermoelectric Energy Harvesting Interface with 86.6% Peak Efficiency at 30 μW and Total Control Power of 160 nW

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Abstract—A thermoelectric energy harvesting interface based on a single-inductor dual-output (SIDO) boost converter is presented. A system-level design methodology combined with ultra-low power circuit techniques reduce the power consumption and minimize the losses within the converter. Additionally, accurate zero-current switching (ZCS) and zero-voltage switching (ZVS) techniques are employed in the control circuit to ensure high conversion efficiency at μW input power levels. The proposed SIDO boost converter is implemented in a 0.18 μm CMOS process and can operate from input voltages as low as 15 mV. The measurement results show that the converter achieves a peak conversion efficiency of 86.6% at 30 μW input power.

Index Terms—Boost converter, energy harvesting, single-inductor dual-output, zero-current switching, zero-voltage switching, dead time, low-power design.

I. INTRODUCTION

EXTENSIVE investigation of potential harvesting solutions is driven by the increase need of self-powered, long-lifetime, and small-size wireless sensor systems. For instance, wearable and implantable biomedical systems could particularly benefit from autonomous, miniature, biocompatible and ECO-friendly harvesting devices. However, for most biomedical systems, harvesting solutions remain challenging to implement due to their constrained size and excessive power consumption in comparison to the available energy extracted from the environment. Recent micro-/nano-technology advances have pushed the power consumption of biomedical systems to extremely low values. At the same time, the power density of the miniature harvesters is constantly improving, making energy harvesting a feasible powering solution.

Among harvesting sources that are suitable for biomedical systems [1], [2], the latest thermoelectric generators (TEGs) provide the highest power densities at miniature scales (more than 100 $\mu\text{W}/\text{cm}^3$ [3]). However, in wearable, and especially in implantable biomedical applications, the expected temperature differences across the plates of a TEG are very low, ranging from 0.5 K to 3 K [4], [5]. At these temperature differences, the TEG [3] can provide voltages of 15 mV–90 mV and power levels of 1 μW –40 μW to a matched load. So, a customized boost converter is necessary to efficiently

up-convert such low voltages to the levels required by a biosensor system. Extremely low input voltages combined with high conversion ratios and ultra-low power levels set very challenging specifications for the boost converter.

Recent literature demonstrates various low input voltage boost converters for thermoelectric energy harvesting [6]–[10]. Different approaches have been proposed to overcome the challenges and improve the conversion efficiency. For instance, a low power control method has been proposed in [6] to facilitate the up-conversion of very low input voltages. A maximum power extraction (MPE) technique has been introduced in [7] to maximize the end-to-end transfer of the extracted energy. In [8], a fully electrical start-up circuit has been demonstrated. High conversion efficiencies (above 80%) are achieved in [9] and [10] due to improved control schemes. However, all these solutions obtain high efficiencies at relatively high input power levels (from hundreds of μW to mW). As the input power decreases, the efficiencies degrade and become insufficient at μW power levels. This is because the power consumption of the control circuit and the losses within the converter become comparable to the input power. To overcome these challenges, this paper proposes a combination of methods and circuit techniques to reduce the power consumption, and further suppress the losses within the converter. First, losses expressions are used to find the optimal switching frequency, inductor value and switch sizes of the converter. Next, a dual-output architecture is employed to reduce the power consumption of the control circuit to nW level. Finally, accurate zero-current and zero-voltage switching techniques mitigate the losses related to the accuracy of the control. This paper is organized as follows. Section II introduces the system architecture and its advantages. Section III presents a thorough losses analysis and a design methodology for achieving a high efficiency. Section IV focuses on detailed circuit implementations of individual building blocks. Section V highlights the measurement results. Finally, concluding remarks are given in Section VI.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the proposed single-inductor dual-output (SIDO) architecture of the boost converter. It consists of a DC-DC core circuit and a control block. The control block includes a switch control, driver circuit, supply multiplexer, voltage divider, voltage monitor circuit, clock generator, and reference circuits. To achieve a high conversion efficiency at

Fig. 1. System architecture of the boost converter.

μW input power levels, besides reducing the losses within the converter, the power consumption of the control circuit has to be minimized relative to the input power. Considering that the control circuit is almost entirely digital [6]–[8], the most effective way to reduce its power consumption is to reduce the supply voltage [11]. The control circuit is usually powered from the output of the converter [6], [8]–[10], and since the converter is driving a biosensor system, its output voltage is defined by the requirements of the biosensor rather than optimized for the low power consumption of the control circuit. Instead, in this work a separate output is added to the converter and used to power the control circuit. The additional output is beneficial for multiple reasons. First, since it is independent of the requirements of the biosensor system, it can be optimized for a low power consumption of the control circuit. Second, to start-up the converter, instead of charging a large storage capacitor, C_{ST} , a much smaller second output capacitor, C_{CTRL} , is charged. Finally, the second output can also be used as a second voltage supply for the biosensor system. The boost converter transfers the energy extracted from the harvester to only one of its two outputs at the time. The main output, V_{ST} , is used to power the load (duty cycled biosensor) and the additional output, V_{CTRL} , powers the internal circuits (control block) of the converter. The timing diagrams of the output voltages are also shown in Fig. 1. The output V_{CTRL} is regulated to around 1 V. The control block assures that the energy is forwarded to the capacitor C_{CTRL} whenever $V_{CTRL} < 1$ V is detected. When the second output is not used, C_{CTRL} is charged roughly once in every 80 cycles in typical conditions (the input power $\sim 17 \mu\text{W}$). Most

of the time, the harvested energy is transferred to V_{ST} and accumulated over time in the storage capacitor C_{ST} . When sufficient energy is accumulated ($V_{ST} = 2$ V), the signal V_{ST_OK} (active high) is triggered to enable the load. The load is enabled until C_{ST} is discharged to 1.8 V, the point at which V_{ST_OK} becomes inactive again. Therefore, the load is enabled asynchronously to accommodate for unpredictable input power levels.

III. DESIGN METHODOLOGY

The main goal of the boost converter is to provide as much power as possible to the load (at the appropriate voltage level). In order to do so, it first has to extract the maximum possible power from the TEG, then efficiently transfer that power to the load and, at the same time, convert the voltage to a higher level. The proposed methodology aims to maximize the efficiency by jointly optimizing the total losses within the converter and the power consumption of its control circuit.

The MPE is achieved by matching the equivalent input resistance of the converter, R_{IN} , to the internal resistance of the TEG, R_{TEG} . Assuming that $V_{ST} \gg V_{IN}$, R_{IN} can be expressed as [7]:

$$R_{IN} \approx \frac{2L}{\tau_N^2 f_s}, \quad (1)$$

where L is the inductor value, τ_N is the duration of the nMOS switch ON time and f_s is the switching frequency of the converter.

The conversion efficiency of the boost converter is defined as:

$$\eta = \frac{P_{out}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}} - \frac{P_{ctrl}}{P_{in}}, \quad (2)$$

where P_{in} and P_{out} are the input and output power of the converter, respectively, P_{loss} represents the total losses within the converter and P_{ctrl} is the power consumption of the control block. The total losses within the boost converter are a sum of conduction, switching, synchronization and leakage losses. The synchronization losses arise from inaccurate turn ON and OFF timings of the pMOS switches (in Fig. 1), where in both cases the body diode or the reverse conduction introduce some additional losses to the already present conduction losses [6], [12]. The leakage losses originate from the subthreshold leakage currents through the switches and may become significant when very low input power levels are targeted [13].

A. Losses Analysis

The two pMOS switches of the boost converter are identically sized, and since only one is working at a time, in terms of the conduction losses this is approximately equivalent of having one output which turns ON in every cycle. A similar observation can be made regarding the switching losses. However, the additional switch, M_{PC} , introduces more parasitic capacitance at node X increasing the switching losses related to this node. The leakage loss of M_{PC} is negligible compared to the leakage loss of the main switch, M_P . This is because in the off-state, the drain voltage of M_{PC} is twice lower while its gate voltage is the same as of M_P , so the drain-induced barrier lowering (DIBL) effect is much less pronounced [14]. For these reasons and the sake of simplicity, the losses' analysis is done considering that the converter has a single output, but the total capacitance at node X is estimated considering both pMOS switches.

1) *Conduction Losses*: The conduction losses originate from the nMOS and pMOS switches ON resistances (R_N and R_P , respectively), the inductor's equivalent series resistance (R_L) and the total parasitic series resistance (R_{par}). The resistance R_{par} includes all parasitic resistances in the power path, such as resistances from PCB tracks, bondwires and other. The inductor core losses are neglected. Assuming that $V_{ST} \gg V_{IN}$, the inductor's volt-second balance can be approximated as $V_{IN} \cdot \tau_N \approx V_{ST} \cdot \tau_P$ indicating that $\tau_N \gg \tau_P$. Therefore, the conduction losses can be expressed as:

$$\begin{aligned} P_{cond} &= \frac{I_{L,max}^2}{3} \tau_N f_s (R_N + \frac{V_{IN}}{V_{ST}} R_P + R_L + R_{par}) \\ &= \frac{2\sqrt{2}V_{IN}^2}{3\sqrt{R_{IN}^3}} \frac{1}{\sqrt{f_s}\sqrt{L}} (R_N + \frac{V_{IN}}{V_{ST}} R_P + R_L + R_{par}), \end{aligned} \quad (3)$$

where τ_N is extracted from (1) and $I_{L,max} = (V_{IN} \cdot \tau_N)/L$ is the maximum inductor current.

2) *Switching Losses*: The switching losses arise from driving the gate capacitances of the nMOS and pMOS switches, C_N and C_P , respectively, and the parasitic capacitance at node X, C_X [13]. The switching losses can be approximated as:

$$P_{sw} = (kC_N + kC_P + \frac{1}{2}C_X)V_{ST}^2 f_s. \quad (4)$$

where k is the power consumption factor of a driver circuit. The driver circuit usually consists of several buffer stages, so

Fig. 2. Detailed switching diagrams during the dead time when (a) dead time is accurate, (b) dead time is short, and (c) dead time is long.

besides the power required to charge and discharge the gate capacitance, the additional power is consumed in the driver circuit. For this reason, the factor k is not equal but higher than one. In this work, the driver circuit is implemented as a 4-stage tapered buffer, which presents $k \approx 2$.

3) *Synchronization Losses*: These losses can be completely eliminated if ON and OFF timings of the pMOS switches are perfect. However, in reality small timing errors are inevitable.

Turn-off timing losses are defined by the duration of the pMOS switch ON time, τ_P . The duration of τ_P is accurate if the pMOS switch is turned off when the inductor current reaches zero. As a result, almost lossless Zero-Current Switching (ZCS) is achieved. For short τ_P , the switch is turned off early, the inductor current flows through the body diode of the transistor and introduces the additional losses. When τ_P is long, the pMOS switch is turned off late. In this situation, the inductor current changes polarity and discharges the output capacitor introducing relatively high losses. The losses introduced when τ_P is short ($P_{sync,s}$) are much lower than when τ_P is long ($P_{sync,l}$) for the same timing error, t_{err} . This is evident from $\frac{P_{sync,s}}{P_{sync,l}} = 1 - \frac{t_{os}}{t_{err}}$, which can be extracted from [6], where t_{os} is the overshoot time (usually very close to t_{err}). The fact that $P_{sync,s}$ is much lower than $P_{sync,l}$ for the same t_{err} will be utilized during the design of the control block to further suppress the synchronization losses.

Turn-on timing losses of the pMOS switch are defined by the dead time, t_{dead} . During t_{dead} both switches are OFF and the inductor current is charging C_X . The pMOS switch should turn on when V_X reaches the output voltage, as it is shown in Fig. 2(a). In this case, almost lossless Zero-Voltage Switching (ZVS) is achieved. If t_{dead} is short, the switch is turned on early, as it is illustrated in Fig. 2(b). Since V_X is still lower than the output voltage, C_X is charged from the output capacitor. The reverse current flow introduces significant losses. When t_{dead} is long, the switch is turned on late, as it is shown in Fig. 2(c). As a result, V_X exceeds the output voltage and, eventually, the body diode of the transistor becomes forward-biased introducing the additional losses. The dead time has to be adaptive to successfully eliminate the dead time losses. Otherwise, the efficiency can be degraded

Fig. 3. ESR versus inductance for the miniature inductor family [16].

with more than 2% [15]. Nevertheless, typical designs consider only a fixed dead time. In this work, an adaptive dead time generator is incorporated in the control circuit to suppress the dead time losses and achieve ZVS.

4) *Losses from Parasitics*: The capacitance C_X and the resistance R_{par} are the major parasitic contributors to the total losses of the boost converter. They include parasitics from the PCB tracks, package, bondwires, PADs, ESD protection, on-chip interconnections and switches of the converter. In μW boost converters, all these parasitics have to be carefully addressed. Otherwise, they can significantly reduce the overall efficiency of the converter. The additional problem is that most of the techniques that are used to reduce C_X will increase R_{par} and vice versa. Both C_X and R_{par} can be reduced by using a miniature, no-lead chip package, such as a quad-flat no-lead package (QFN) or similar. Besides parasitics from the chip leads, the miniature package also reduces the length and, consequently, the resistance of bondwires. The use of multiple bondwires/PADs for node X and ground connections also reduces R_{par} , but at the same time increases C_X . In this design, optimal numbers of bondwires/PADs for these nodes are empirically determined. In addition, to further reduce the parasitic resistance, the on-chip interconnections for the power path are implemented using networks of multiple metal layers. Finally, the achieved values of C_X and R_{par} are estimated to 10 pF and 0.15 Ω , respectively.

B. Efficiency Optimization

To achieve a high efficiency, the sum of P_{loss} and P_{ctrl} has to be minimized, as it can be seen from (2). In [13], the optimal values of the switching frequency and power transistors' widths for given R_{IN} , V_{IN} , V_{ST} and L provide optimal losses. In this work, the optimization is extended to the power consumption of the control circuit. This is possible because the control is mostly digital, so its power consumption is frequency dependent [11]. In addition, the optimal inductor value is also obtained, contrary to the common practice of intuitively selecting the inductor value as a trade-off between efficiency and form-factor [6]–[8], [13].

Equation (3) indicates that the higher inductance reduces the conduction losses. However, for the inductors limited by form-factor, the equivalent series resistance of the inductor (ESR) increases proportionally with the inductance. Fig. 3 shows the

Fig. 4. Sum of P_{loss} and P_{ctrl} versus individual variables: (a) widths of the nMOS and pMOS switches W_N and W_P , (b) switching frequency f_s and (c) inductance L .

ESR versus inductance for miniature inductors, family 744043 [16]. Therefore, the ESR value (R_L) can be roughly approximated as $p_1 \cdot L$, where p_1 is an inductor family dependent constant coefficient. Consequently, the overall contribution of R_L to the conduction losses increases (it is proportional to $\sqrt{L}$) when a higher inductance is used. In fact, there is an optimal inductance for which the losses are minimized.

Assuming that the control circuitry is successfully suppressing the synchronization losses, by combining (3) and (4), the sum of P_{loss} and P_{ctrl} can be expressed as:

$$\begin{aligned}
 P_{loss} + P_{ctrl} = & \frac{2\sqrt{2}V_{IN}^2}{3\sqrt{R_{IN}^3}\sqrt{f_s}} \left(\frac{R'_N}{W_N\sqrt{L}} + \frac{R'_P V_{IN}}{W_P V_{ST}\sqrt{L}} \right. \\
 & + p_1\sqrt{L} + \frac{R_{par}}{\sqrt{L}} \Big) + f_s (kC'_N W_N V_{ST}^2 \\
 & + kC'_P W_P V_{ST}^2 + \frac{1}{2}C_X V_{ST}^2 \\
 & + C_{c,eff} V_{CTRL}^2) + V_{IN} I_{leak,N} W_N \\
 & + (V_{ST} - V_{IN}) I_{leak,P} W_P, \quad (5)
 \end{aligned}$$

where R'_N and R'_P are the resistances per unit width, C'_N

Fig. 5. Current and voltage references.

and C'_P are the gate capacitances per unit width, $I_{leak,N}$ and $I_{leak,P}$ are the leakage currents per unit width of the nMOS and pMOS transistors, W_N and W_P are the transistors' widths and $C_{c,eff}$ is the total effective capacitance of the control circuitry [11]. Optimal values of W_N , W_P , f_s and L can be obtained, for which the sum of P_{loss} and P_{ctrl} is minimum for given R_{IN} , V_{IN} , V_{ST} and V_{CTRL} . Fig. 4 shows the sum of P_{loss} and P_{ctrl} versus individual variables (W_N , W_P , f_s and L) while other variables are set to their optimal values obtained from (5). For instance, Fig. 4(b) shows how this sum depends on the switching frequency when W_N , W_P and L are optimal. The arrows in Fig. 4 display the direction in which the certain types of losses are increasing. The input voltage is set to 60 mV, which is expected in typical conditions. The input resistance is assumed to be matched to the internal resistance of the TEG and equal to 210 Ω [3]. The voltage V_{ST} is set to its mean value of 1.9 V and V_{CTRL} is set to 1 V. The capacitance C_X and resistance R_{par} are estimated to 10 pF and 0.15 Ω , respectively. The coefficient p_1 is fixed to 10 m Ω/μ H, which corresponds to the inductor family [16] after accounting for tolerance. The capacitance $C_{c,eff}$ is estimated to around 5 pF in this particular case.

IV. CIRCUIT IMPLEMENTATION

The design methodology presented in Section III is complemented by ultra-low power circuit techniques in order to obtain a high efficiency. The power dissipation of digital circuits is reduced by using a low voltage supply. The short-circuit currents are additionally reduced by making the rise/fall time at the input and the output of the gates similar [11]. The analog blocks are either low-frequency dynamic circuits (voltage divider and comparators) or operate in the weak inversion region (voltage and current reference), so their power dissipation is also very low. As a result, the complete control circuit consumes 160 nW, from which the static power amounts for only 80 nW.

A. Current and Voltage References

Fig. 5 shows the current and voltage references. The power consumption of both circuits is at nW levels. The current

Fig. 6. Clock generator.

reference is voltage supply independent, operates in the weak inversion region and generates a PTAT biasing current. The resistance R_s and the transistors M_1 and M_2 are sized so that the biasing current is equal to 10 nA. According to the Monte Carlo simulation (process and mismatch variations, 1000 runs), the average value of the biasing current is 10.26 nA and the standard deviation is 0.98 nA. The start-up circuit does not consume any static power [17]. The voltage reference, proposed in [18], is adopted since it provides a very good performance at low power levels. The power consumption is reduced to 30 nW at the expense of higher supply and temperature sensitivities. The voltage reference operates correctly when the supply voltage is greater than 0.8 V. The average value of the output voltage according to the Monte Carlo simulation (process and mismatch variations, 1000 runs) is 500.7 mV and the standard deviation is 12.7 mV. The simulated temperature coefficient is 50 ppm/ $^{\circ}$ C in a temperature range from -40° C to 85° C.

B. Driving the nMOS Switch

The switching frequency and the value of the inductor are set to minimize the losses within the converter, as it is shown in Fig. 4. Therefore, τ_N and the duty cycle of the boost converter, $D = \tau_N f_s$, are determined by (1). For $R_{IN} = 210 \Omega$ and the optimal values of f_s and L (15 kHz and 33 μ H, respectively), the calculated τ_N is 4.6 μ s and D is approximately 7%. The signal for driving the nMOS switch is obtained directly from the clock generator. Fig. 6 shows the clock generator circuit, which consists of a current-starved ring oscillator and logic gates. The ring oscillator is composed of 15 stages. The multiple output signals of the oscillator are processed through logic gates to derive the clock signals clk_N , clk_D and clk_C .

Fig. 7. Switch control and switch driver circuits.

All clock signals are running at 15 kHz with 7% duty cycle and are delayed with respect to each other, as it is shown in Fig. 6. A 2-bit digital signal a_1a_0 adjusts the biasing current and, consequently, the operating frequency, for process variations if necessary. The signal clk_N is used to drive the nMOS switch, as it is shown in Fig. 7. The level shifter modifies the high level of clk_N from V_{CTRL} to the greater of V_{CTRL} and V_{ST} . Finally, the driver circuit (tapered buffer) drives the gate of the nMOS switch. The signal clk_D is used for the voltage divider and clk_C for the voltage monitor circuit.

C. Zero-Current Switching

The ZCS is achieved when τ_P is accurate. In previous works [6]–[8], the value of τ_P is adjusted after every switching cycle according to the 1-bit information obtained from sensing the voltage V_X . Over time, τ_P approaches the accurate value, but when it gets very close, it fluctuates around that value. Consequently, τ_P is always slightly shorter or slightly longer, and introduces synchronization losses as it was already explained. The timing error t_{err} depends on the unity delay in the one-shot pulse generator (the resolution of τ_P). The slightly shorter τ_P is preferred in terms of synchronization losses. This result is utilized in this work, so τ_P is kept to its closest to the accurate, but slightly shorter value [19]. Equivalently, the ZCS of the additional pMOS switch is achieved when its ON time, τ_{PC} , is accurate. Considering the inductor's volt-second balance in both cases $V_{IN} \cdot \tau_N \approx V_{ST} \cdot \tau_P$ and $V_{IN} \cdot \tau_N \approx V_{CTRL} \cdot \tau_{PC}$, the accurate τ_{PC} can be related to the accurate τ_P as $\tau_{PC} \approx \frac{V_{ST}}{V_{CTRL}} \tau_P$. For the targeted input voltage, τ_P varies from 36 ns to 218 ns with the step of approximately 12 ns and τ_{PC} from 70 ns to 414 ns with the step of approximately 23 ns. As a result, the switch control circuit can share the counter and the sensing circuitry for both switches, but separate one-shot signal generators are required.

Fig. 8. Adaptive dead time circuit.

Fig. 9. Accurate dead time and the dead time introduced by the circuit. The introduced dead time is slightly longer than accurate to avoid a lossy reverse conduction of the pMOS switch.

The proposed implementation for the ZCS scheme is shown in Fig. 7. The signal V_{CTRL_OK} is active as long as $V_{CTRL} \geq 1$ V, in which case the transistor M_P (in Fig. 1) is operating. Otherwise, the energy is forwarded to the additional output through M_{PC} . The voltage V_X is sensed two times per cycle. The sensing is triggered by the delayed rising edges of one

Fig. 10. Voltage divider and voltage monitor circuits.

of the signals q_P or q_{PC} . The sensed 2-bit digital signal (b_1b_0) provides the information whether τ_P and τ_{PC} are long ($b_1b_0 = 00$), short ($b_1b_0 = 11$) or accurate ($b_1b_0 = 10$). The reading $b_1b_0 = 01$ is not used. The counter value is updated according to b_1b_0 or stopped if the accurate durations are reached. Based on the counter value, the one-shot signal generators with controllable signal width adjust the durations of ON times for the next switching cycle. A 4-bit counter is used in this work as a good trade-off between accuracy and complexity.

D. Zero-Voltage Switching

The dead time for which ZVS is achieved can be approximated as [15]:

$$t_{dead} \approx \frac{C_X L}{\tau_P}. \quad (6)$$

The dead time is introduced as a delay of the falling edge of the signal q_N which triggers the one-shot signal generator, as it is shown in Fig. 7. According to (6), the same counter that is used to define τ_P can be used to control the dead time. The additional output of the boost converter requires a separate dead time circuit.

The proposed implementation for the adaptive dead time circuit is shown in Fig. 8. The circuit operates as a digitally programmable delay element controlled by the decoded counter value. A 2-bit signal d_1d_0 adjusts the dead time for variability of C_X . The signal d_1d_0 is also used to prolong the dead time during measurements at node X to compensate for the capacitance added at this node by an oscilloscope probe. Fig. 9 shows the typical dead time introduced by the circuit and the accurate dead time required for a perfect ZVS. Similarly as in the ZCS scheme, the introduced dead time is slightly longer than the accurate dead time to avoid a lossy reverse conduction of the pMOS switch.

Fig. 11. Supply MUX circuit.

E. Voltage Divider, Voltage Monitor and Supply Multiplexer Circuits

A conventional resistive voltage divider requires a very high total resistance so that its power consumption is negligible compared to other losses within the converter. For instance, a 10 M Ω voltage divider dissipates around 0.36 μ W from the output and reduces the efficiency of the converter with approximately 2% in the typical case. Further increasing the resistance requires even more chip area. For these reasons, a switched capacitor voltage divider was selected for this work. This solution enables significant area and power savings because the low operating frequency allows using small capacitors while obtaining a high equivalent resistance at the same time. The voltage monitor circuit compares the output voltages V_{CTRL} and V_{ST} with the reference and defines their levels. It also generates V_{CTRL_OK} and V_{ST_OK} signals. The proposed implementations for the voltage divider and voltage monitor circuits are shown in Fig. 10.

The smaller of the two output capacitors, C_{CTRL} , is charged to start-up the boost converter. This means that in the initial phase of the converter's operation, V_{CTRL} is higher than V_{ST} , until enough energy is accumulated in C_{ST} so that V_{ST} surpasses V_{CTRL} . For the proper operation of the converter and to prevent conduction of body diodes, the driver circuits and the bulk terminals of the pMOS switches of the converter should be powered from the greater of V_{CTRL} and V_{ST} at any time. The supply MUX circuit compares V_{CTRL} and V_{ST} and connects the greater of the two voltages, V_{MAX} , to the

Fig. 12. Die photo of the test chip and the evaluation board.

Fig. 13. Measured input voltage of the boost converter.

corresponding circuits [20]. The supply MUX circuit is shown in Fig. 11. A track and latch dynamic comparator compares the supply voltages and controls the switches accordingly. The outputs of the comparator are buffered to drive the switches M_1 and M_2 . The level of the negative output is adjusted so that the switch M_2 is properly turned off. Unlike the supply MUX in [20], this solution does not consume any static power.

V. MEASUREMENT RESULTS

The proposed SIDO boost converter was implemented in a $0.18 \mu\text{m}$ CMOS process. Fig. 12 shows the die photo of the test chip and the evaluation board with the TEG connected. The total chip area is 2.3 mm^2 , from which the active area occupies around 0.3 mm^2 . The evaluation board solution was designed so that the parasitics added to the power path are minimized. The off-chip components include a $33 \mu\text{H}$ inductor L ($4.8 \text{ mm} \times 4.8 \text{ mm} \times 2.8 \text{ mm}$, number 744043330 [16]), a $1 \mu\text{F}$ input capacitor C_{IN} , a 100 nF storage capacitor C_{ST} and a 30 nF control supply capacitor C_{CTRL} . The load (duty cycled sensor) is modeled as a resistor in series with a switch, which is enabled by the V_{ST_OK} signal from the chip. To start-up the boost converter, C_{CTRL} was precharged to 1 V . The chip was evaluated using two tests. In the first test, the equivalent circuit of the TEG (in Fig. 1) was used to fully

(a)

(b)

(c)

Fig. 14. Measured voltages. (a) Control supply voltage V_{CTRL} , (b) Storage voltage V_{ST} , and (c) Voltage across the load V_L .

characterize the converter. In the second test, the chip was evaluated with a commercially available packaged TEG from Micropelt (model TGP-651 in Fig. 12) [3]. The TEG has a typical internal resistance of 210Ω and a Seebeck voltage of 60 mV/K .

The voltage of the equivalent circuit, V_{TEG} , was initially set to 100 mV . Fig. 13 shows the measured input voltage of the converter. Since the average value of V_{IN} is approximately $V_{TEG}/2$, the MPE is achieved ($R_{IN} = R_{TEG}$). Fig. 14 shows

Fig. 15. Measured voltage at node X, V_X .

the measured output voltages V_{CTRL} and V_{ST} , and the voltage across the load, V_L . The transistor M_{PC} (in Fig. 1) switches only when V_{CTRL} drops below 1.04 V (or more precisely below $2 \cdot V_{ref}$) to recharge C_{CTRL} . The rest of the time, M_P is switching, accumulating the energy on C_{ST} . When V_{ST} reaches 1.99 V, the signal V_{ST_OK} becomes active and enables the load (a 48.7 k Ω resistor). The load is powered until V_{ST} drops to 1.83 V. Fig. 15 shows the measured voltage at node X, V_X . The measured f_s is 15.2 kHz, τ_N is 4.68 μ s and D is around 7.1%. The dead time is slightly longer than the accurate, since V_X surpasses V_{ST} and turns on the body diode for a few nanoseconds. The duration of τ_P is slightly shorter, but very close to the accurate value. At the moment when M_P turns off, the inductor current I_L is still flowing through the switch but it is so close to zero that it can not completely turn on the body diode. Therefore, both ZCS and ZVS are achieved. While measuring V_X , the oscilloscope probe adds the capacitance to the node X. To account for this

Fig. 16. Measured conversion efficiency of the boost converter versus the input voltage.

capacitance, the dead time is intentionally prolonged according to (6) by using the signal $d_1 d_0$ (in Fig. 8). To evaluate the conversion efficiency, V_{TEG} was varied from 30 mV to 180 mV. As a result, V_{IN} changes between 15 mV and 90 mV. The measured efficiency (given by (2) where P_{out} represents the power delivered to the load) versus the input voltage is shown in Fig. 16. This figure also shows the theoretical efficiency, obtained from (2) and Eq. (5). The small deviation of the measured efficiency from the theoretical one is due to process variations, tolerances and used approximations. The efficiency is relatively flat for input voltages higher than 45 mV. For these values, the sum of P_{loss} and P_{ctrl} in (5) is dominated by the conduction losses, which are scaled down with the input voltage, keeping the efficiency almost constant. The efficiency starts to roll-off when the input voltage drops below 45 mV. From that point, the switching losses dominate and reduce the efficiency as the input voltage decreases further. The boost converter is still operating when the input voltage is below 20 mV. However, in such case the entire energy is transferred to the additional output to power the control circuit, meaning that the power delivered to the load is equal to zero, so as the efficiency. When the input voltage drops below 15 mV, the converter shuts down and requires a new start-up procedure.

The chip was also tested with the packaged thermoelectric device [3]. When the hot plate of the device was pressed against the skin on the wrist while the cold plate was connected to a heat sink, to maintain the temperature of the surrounding air, the harvester was generating the voltage of around 150 mV, which corresponds to 2.5 K temperature difference between the plates. In this case, the converter was extracting 27 μ W from the TEG and was delivering around 23 μ W to the load.

Table I compares this work with the state-of-the-art low power boost converters [6]–[10], [13], [21]. It can be seen that the proposed SIDO boost converter provides the highest conversion efficiency and it is one of the lowest power designs among the CMOS μ W power solutions.

TABLE I
COMPARISON OF THE CONVERTER WITH STATE-OF-THE-ART WORK.

	[6]	[7]	[21]	[8]	[13]	[9]	[10]	This Work
Year	2010	2011	2012	2013	2014	2015	2015	2015
Process	0.13- μ m	0.35- μ m	-	65-nm	0.18- μ m	0.18- μ m	0.13- μ m	0.18- μ m
Output Voltage	1 V	1.8 V	1.8-5.5 V	1.2 V	1 V	0.5 V	1.2 V	1.9 V
Min. Input Voltage	20 mV	25 mV	80 mV	30 mV	20 mV	100 mV	10 mV	15 mV
Peak Efficiency	75% $P_{in} = 0.2\text{mW}$	58% $P_{in} = 0.5\text{mW}$	72%* $P_{in} = 2\text{mW}$	73% $P_{in} = 0.4\text{mW}$	53% $P_{in} = 1.2\text{nW}$	83.4% $P_{in} = 0.3\text{mW}$	83% $P_{in} = 11\text{mW}$	86.6% $P_{in} = 30\mu\text{W}$
Start-up	no	yes	yes	yes	no	no	yes	no
MPE	no	yes	yes	yes	yes	no	yes	yes

* At the comparable input voltage ($V_{IN} = 0.2$ V).

VI. CONCLUSION

This paper has presented a high-efficiency SIDO boost converter for micropower thermoelectric energy harvesting. The dual-output architecture has enabled a significant reduction of the control circuit's power consumption. A theoretical analysis has indicated the optimal switching frequency, inductor value and switch sizes of the converter for minimizing the power and losses. High-efficiency at very low input power levels is reached by combining the obtained optimal values with the accurate ZCS and ZVS techniques. The converter achieves over 80% conversion efficiency for input powers higher than 9 μ W and a peak conversion efficiency of 86.6% at 30 μ W input power. The converter can operate with input voltages as low as 15 mV, which corresponds to 1 μ W input power. Such high efficiency at so low harvested power levels is an extremely important improvement with respect to previously reported works and it paves the way to the development of self-powered wearable and implantable biosensors.

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