Design and Process Issues of Junction- and Ferroelectric- Field Effect Transistors in Silicon Carbide

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Ph.D. Thesis

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Stockholm, 2003
Design and Process Issues of Junction- and Ferroelectric- Field Effect Transistors in Silicon Carbide

A dissertation submitted to Kungliga Tekniska Högskolan, Stockholm, Sweden, in partial fulfillment of the requirements for the degree of Teknisk Doktor (Ph.D.)

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To My Parents

Abstract

In today’s solid-state electronics, Si and SiO₂ are the dominant materials used. However, new materials such as SiC or ferroelectrics are required for some special applications since superior characteristics can be achieved in electronic devices. The main objective of this work is the design, fabrication and characterization of different field effect transistors (FETs) including the new device structures referred to as junction-gated metal-oxide-semiconductor FET (JMOSFET) and ferroelectric-FETs (FeFET) as well as the conventional junction-FET (JFET).

Buried-gate JFETs with two different structures have been fabricated in epitaxial layers of 4H-SiC using only 2- to 3-mask steps. It has been shown that the trenching effect during dry etching can induce static induction transistor (SIT)-like drain conduction for JFETs with small channel thickness (less than 0.5 micro-meter). The conduction mechanism in these JFETs is examined by the potential profiles from two-dimensional numerical simulations. The trenching effect can be reduced for JFETs using an oxide mask for dry etching with sloped etch profile (an angle of around 30°). It has also been demonstrated that, by introducing a sacrificial oxidation (SO) step on the inductively coupled plasma (ICP)-etched surface of SiC, the electrical properties of MOS capacitors and Ohmic contacts can be effectively recovered after dry etch damage. The switching performance of JFETs in a test circuit has been investigated with an inductive load and compared with numerical device simulations. A drain voltage rise/fall time of around 30 ns has been observed for turn-off and turn-on. The results have been compared to numerical mixed-mode circuit simulations with finite element structures.

To improve the high temperature stability and to lower the on-state resistance, we have designed the so-called ‘JMOSFET’, which is a buried-gate JFET with an additional MOS-gate on top. The JMOSFETs have shown the feasibility for operation with a constant current level from room temperature all the way up to 300 °C by applying proper backside-gate voltage. An advantage of this device is the improved channel transconductance (2.5 times), which results from accumulating the n-channel with the MOS gate.

In realizing ferroelectric devices above room temperature and in severe environment, high temperature polarization behavior and retention of ferroelectric thin films are critical factors to explore. Thus SiC is one of the most attractive semiconductor material for these applications. We have found an optimum ferroelectric gate structure (using pulsed laser deposition) of PZT/Al₂O₃/4H-SiC (large C-V memory window of 10 V, low conductance <0.1 mS/cm², tangent delta of 0.0007 at 400kHz). Based on this structure, the nonvolatile operation of FeFETs in SiC has been shown for the first time at elevated temperatures. The transistor showed a memory effect from room temperature up to 200 °C and stable transistor operation was observed up to 300 °C. The retention of the nonvolatile memory was 2×10⁴ seconds at 150 °C without applying bias on the gate.

Keywords: silicon carbide, ferroelectrics, PZT, field effect transistor, FET, JFET, MOSFET, device simulation, capacitance-voltage measurements, pulsed laser deposition
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I. Electrical characteristics of metal-oxide-semiconductor capacitors on plasma-etch damaged silicon carbide
   S.-M. Koo, S.-K. Lee, C.-M. Zetterling, and M. Östling

II. Ohmic contact formation on inductively coupled plasma etched 4H-silicon carbide
    S.-K. Lee, S.-M. Koo, C.-M. Zetterling, and M. Östling

III. Influence of trenching effect on the characteristics of buried-gate SiC junction field-effect transistors

IV. Simulation and Measurement of Switching Characteristics of 4H-SiC buried-gate JFETs
    S.-M. Koo, M. Domeij, C.-M. Zetterling, M. Östling, U. Forsberg and E. Janzen

V. Combination of JFET and MOSFET devices in 4H-SiC for high-temperature stable circuit operation
   S.-M. Koo, C.-M. Zetterling, H.-S. Lee, and M. Östling
   *Submitted to IEE Electronics Lett.*

VI. Ferroelectric Pb(Zr,Ti)O₃/Al₂O₃/4H-SiC diode structures
    S.-M. Koo, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling

VII. Towards ferroelectric field effect transistors in 4H-silicon carbide (Invited)
     S.-M. Koo, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling

VIII. Ferroelectric Pb(Zr,Ti)O₃-SiC field effect transistor
     S.-M. Koo, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling
     *In manuscript*

The appended papers in the thesis comprise the following four topics in general.

(i) Processing issues in SiC devices: **Paper I - II**
(ii) Fabrication, characterization and simulation of buried-gate junction field effect transistors (JFETs): **Paper III-IV**
(iii) Design, fabrication, characterization and simulations of junction- and MOS-gated field effect transistors (JMOSFETs): **Paper V**
(iv) Fabrication and characterization of ferroelectric-gated devices: **Paper VI-VIII**
Other Works Not Included in the Thesis

1. **Devices in SiC (Book Chapter)**  
   C.-M. Zetterling, S.-M. Koo, and M. Östling  

2. **Challenges for High Temperature Silicon Carbide Electronics (Invited)**  

3. **Processing and Properties of Ferroelectric Pb(Zr,Ti)O$_3$/Silicon Carbide Field-Effect Transistor**  
   S.-M. Koo, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling  
   *To be published in Integrated Ferroelectrics.*

4. **Challenges and Recent Advances in SiC Device Technologies (Invited)**  
   M. Östling, S.-M. Koo, M. Domeij, E. Danielsson, and C.-M. Zetterling  
   *To be presented at IEEE Conference on Electron Devices and Solid-State Circuits, Kowloon, Hong Kong 2003.*

5. **Recent advances and issues in SiC process and device technologies (Invited)**  
   M. Östling, S.-M. Koo, S.-K. Lee, E. Danielsson, and C.-M. Zetterling  

6. **SiC device technology for high voltage and RF power applications (Invited)**  
   M. Östling, S.-M. Koo, S.-K. Lee, E. Danielsson, M. Domeij and C.-M. Zetterling  
   *Proc. 23rd IEEE Int. Conf. Microelectronics (MIEL), Nis, Yosgoslia, 2002., vol. 1, pp. 31-39.*

7. **Metal-oxide-semiconductor structures in inductively coupled plasma etch damaged 6H- and 4H-SiC**  
   S.-M. Koo, S.-K. Lee, C.-M. Zetterling, and M. Östling  

8. **Static and Dynamic Characteristics of Junction Field Effect Transistors in 4H Silicon carbide**  
   S.-M. Koo, M. Domeij, C.-M. Zetterling, and M. Östling  
   *In proceedings of Nordic Workshop on Power and Industrial Electronics, Stockholm, Sweden, 2002.*

9. **Resonant tunneling in Dy or Gd-doped Al$_2$O$_3$ magnetic tunnel junction**  
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10. Ferroelectric Thin Film Multilayers by Pulsed Laser Depositiontors  
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11. BaRuO$_3$ thin film electrode for ferroelectric lead zirconate titanate capacitors  

12. Structural and Electrical Properties of SBT Thin Films  

13. Preparation and Properties of PGO Thin Films by PLD  

14. Multiple electrical conductive properties and microstructure of epitaxial thin films of BaRuO$_3$  
*In manuscript*

15. Nd substitution effects in YBa$_2$Cu$_4$O$_8$ prepared by a conversion reaction from Y$_1$-xNd$_x$Ba$_2$Cu$_3$O$_{7-4}$ and CuO  

16. Annealing effect on transport properties of Nd$_{0.67}$Sr$_{0.33}$MnO$_3$ thin films  

17. Magnetoresponse Studies in CMR Manganites Thin Films  

18. PLD of Ferroelectric Thin Films and Heterostructures using an Nd:YAG laser  

19. Thermopower measurements on CMR Manganites  
Presentations (only personally given by the author)

1. Towards ferroelectric field effect transistors in 4H-silicon carbide (Oral, Invited)
   S.-M. Koo, S. I. Khartsev, C.-M. Zetterling, A. M. Grishin, and M. Östling

2. Simulation and Measurement of Switching Characteristics of 4H-SiC buried-gate JFETs (Poster)
   S.-M. Koo, M. Domeij, C.-M. Zetterling, M. Östling, U. Forsberg and E. Janzén

3. Static and Dynamic Characteristics of Junction Field Effect Transistors in 4H Silicon carbide (Oral)
   S.-M. Koo, M. Domeij, C.-M. Zetterling, and M. Östling

4. Influence of trenching effect on the characteristics of buried-gate SiC junction field-effect transistors (Poster)

5. Thermopower measurements on CMR Manganites (Oral)
   International Conference on Magnetism & Magnetic Materials (MMM), San Jose, California, USA, 15-18 Nov. 1999.


7. Structural and Electrical Properties of SBT Thin Films (Oral)

8. Preparation and Properties of PGO Thin Films by PLD (Poster)
Overview of Appended Papers

The summary of each paper and the description on the author’s contribution are given as follows:

**Paper I**
This paper investigates the electrical properties of oxides on ICP etch-damaged 6H- and 4H-SiC. *C-V* and *I-V* characteristics of the fabricated MOS capacitors have been studied. It has been shown that a sacrificial oxidation treatment improves the electrical characteristics of MOS capacitors on etch-damaged SiC. The author performed all the processing and the electrical characterization and wrote the manuscript.

**Paper II**
Another investigation of the ICP etch damage on 4H-SiC is presented. Ohmic contacts have been formed on etch-damaged SiC using sputtered TiW. We found that the specific contact resistance is highly related to the surface condition from TLM measurements and AFM study. The author contributed with characterizing the samples and writing the manuscript.

**Paper III**
The paper shows how the trenching effect in buried-gate SiC JFET influences its electrical characteristics. Two different structures of JFETs have been fabricated in 4H-SiC and the *I-V* measurements have been examined by using two-dimensional numerical simulations. The author designed the different structures, performed all the processing, characterizations, the device simulations after material growth, as well as writing.

**Paper IV**
The dynamic switching characteristics of the 4H-SiC JFETs have been studied in a circuit with inductive load. The drain voltage fall and rise time in the order of 25-30 ns has been observed and those results have been compared to the results of numerical mixed-mode simulations. The author performed all the processing, participated in the characterization and analysis and wrote the manuscript.

**Paper V**
In this paper, a new structure of JFETs with additional depletion MOS-gate have been fabricated and characterized in 4H-SiC. The high-temperature stable operation in terms of constant currents has been explored (together with numerical simulation) in the J-MOSFETs. The author performed all the processing and writing and took part in the simulation and characterization.

**Paper VI**
This paper presents the structural and electrical properties of ferroelectric PZT/Al₂O₃/4H-SiC diode structures. X-ray diffractions and *C-V* measurements shows the proposed structure is promising the ferroelectric field-effect devices in SiC. The author performed a major part of the processing, all the characterization, and wrote the manuscript.
Paper VII
An extensive result on the integration of PZT on SiC has been presented and different types of metal-ferroelectric-SiC FET structures have been proposed based on the characterization results. The author performed or participated in all processing steps and characterization and wrote the manuscript.

Paper VIII
The first experimental results on the ferroelectric FETs in SiC have been presented. The nonvolatile operation up to 200 °C has been demonstrated with the depletion mode transistors with ferroelectric gate. The author designed the structure, performed all the clean room processes for the devices, carried out the characterization and wrote the manuscript.
Acknowledgements

The work presented in this thesis has mainly been carried out at the Device Technology group of the Department of Microelectronics and Information Technology, Royal Institute of Technology - KTH from 2000 to 2003, whereas my licentiate work in 1999 at Engineering Materials Physics, KTH has partly been a foundation for the work. During this time I am indebted to many people for their help and encouragement.

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Stockholm, March 2003

Sang-Mo Koo
### Abbreviations Used

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Meaning</th>
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<tbody>
<tr>
<td>ACCUFET</td>
<td>accumulation mode MOSFET</td>
</tr>
<tr>
<td>AFM</td>
<td>atomic force microscopy</td>
</tr>
<tr>
<td>BJT</td>
<td>bipolar junction transistor</td>
</tr>
<tr>
<td>BST</td>
<td>barium strontium titanate</td>
</tr>
<tr>
<td>C-V</td>
<td>capacitance-voltage measurement</td>
</tr>
<tr>
<td>CVD</td>
<td>chemical vapor deposition</td>
</tr>
<tr>
<td>DLTS</td>
<td>deep level transient spectroscopy</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>double-diffused MOSFET</td>
</tr>
<tr>
<td>DRAM</td>
<td>dynamic random access memory</td>
</tr>
<tr>
<td>DRO</td>
<td>destructive read out</td>
</tr>
<tr>
<td>FE</td>
<td>field emission</td>
</tr>
<tr>
<td>FeFET</td>
<td>ferroelectric field-effect transistor</td>
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<tr>
<td>FET</td>
<td>field-effect transistor</td>
</tr>
<tr>
<td>FM</td>
<td>figure of merit</td>
</tr>
<tr>
<td>FRAM</td>
<td>ferroelectric random access memory</td>
</tr>
<tr>
<td>GaAs</td>
<td>gallium arsenide</td>
</tr>
<tr>
<td>GaN</td>
<td>gallium nitride</td>
</tr>
<tr>
<td>GTO</td>
<td>gate turn-off thyristor</td>
</tr>
<tr>
<td>HEMT</td>
<td>high electron mobility transistor</td>
</tr>
<tr>
<td>HF</td>
<td>hydrofluoric acid</td>
</tr>
<tr>
<td>HTCVD</td>
<td>high temperature chemical vapor deposition</td>
</tr>
<tr>
<td>ICP</td>
<td>inductively coupled plasma</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IMPATT</td>
<td>impact ionization avalanche transit-time</td>
</tr>
<tr>
<td>I-V</td>
<td>current-voltage measurement</td>
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<tr>
<td>JBS</td>
<td>junction barrier Schottky</td>
</tr>
<tr>
<td>JFET</td>
<td>junction field-effect transistor</td>
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<tr>
<td>JMOSFET</td>
<td>junction-gated metal-oxide-semiconductor FET</td>
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<tr>
<td>JTE</td>
<td>junction termination extension</td>
</tr>
<tr>
<td>LED</td>
<td>light emitting diode</td>
</tr>
<tr>
<td>LPCVD</td>
<td>low pressure chemical vapor deposition</td>
</tr>
<tr>
<td>LPE</td>
<td>liquid phase epitaxy</td>
</tr>
<tr>
<td>MEMS</td>
<td>micro electro mechanical system</td>
</tr>
<tr>
<td>MESFET</td>
<td>metal-semiconductor field-effect transistor</td>
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<tr>
<td>MFS</td>
<td>metal-ferroelectric-semiconductor</td>
</tr>
<tr>
<td>MFIS</td>
<td>metal-ferroelectric-insulator-semiconductor</td>
</tr>
<tr>
<td>MFMS</td>
<td>metal-ferroelectric-metal-semiconductor</td>
</tr>
<tr>
<td>MISFET</td>
<td>metal-insulator-semiconductor field-effect transistor</td>
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<tr>
<td>MODFET</td>
<td>modulation doped field-effect transistor</td>
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<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>MOS</td>
<td>metal-oxide-semiconductor</td>
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<tr>
<td>MOSFET</td>
<td>metal-oxide-semiconductor field-effect transistor</td>
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<tr>
<td>NDRO</td>
<td>non-destructive read out</td>
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<tr>
<td>NO</td>
<td>nitrous oxide</td>
</tr>
<tr>
<td>NV</td>
<td>non-volatile</td>
</tr>
<tr>
<td>NVFRAM</td>
<td>non-volatile ferroelectric random access memory</td>
</tr>
<tr>
<td>ONO</td>
<td>oxide-nitride-oxide</td>
</tr>
<tr>
<td>P-E</td>
<td>polarization-electric field measurement</td>
</tr>
<tr>
<td>PECVD</td>
<td>plasma enhanced chemical vapor deposition</td>
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<tr>
<td>PVD</td>
<td>physical vapor deposition</td>
</tr>
<tr>
<td>PLD</td>
<td>pulsed laser deposition</td>
</tr>
<tr>
<td>PZT</td>
<td>lead zirconate titanate, Pb(Zr,Ti)O₃</td>
</tr>
<tr>
<td>RAM</td>
<td>random access memory</td>
</tr>
<tr>
<td>RBS</td>
<td>Rutherford backscattering spectrometry</td>
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<tr>
<td>RF</td>
<td>radio frequency</td>
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<tr>
<td>RIE</td>
<td>reactive ion etching</td>
</tr>
<tr>
<td>RTA</td>
<td>rapid thermal annealing</td>
</tr>
<tr>
<td>SAW</td>
<td>surface acoustic waves</td>
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<tr>
<td>SBH</td>
<td>Schottky barrier height</td>
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<tr>
<td>SEM</td>
<td>scanning electron microscopy</td>
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<tr>
<td>SEMOSFET</td>
<td>static channel expansion MOSFET</td>
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<tr>
<td>Si</td>
<td>silicon</td>
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<td>SIAFET</td>
<td>static induction injected accumulated FET</td>
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<tr>
<td>SiC</td>
<td>silicon carbide</td>
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<tr>
<td>SIMS</td>
<td>secondary ion mass spectrometry</td>
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<tr>
<td>SIT</td>
<td>static induction transistor</td>
</tr>
<tr>
<td>SO</td>
<td>sacrificial oxidation</td>
</tr>
<tr>
<td>TE</td>
<td>thermionic emission</td>
</tr>
<tr>
<td>TEM</td>
<td>transmission electron microscopy</td>
</tr>
<tr>
<td>TEOS</td>
<td>TetraEthylOrthoSilicate, Si(OC₂H₅)₄</td>
</tr>
<tr>
<td>TFE</td>
<td>thermionic field emission</td>
</tr>
<tr>
<td>Ti</td>
<td>titanium</td>
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<td>TiC</td>
<td>titanium carbide</td>
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<tr>
<td>TiW</td>
<td>titanium tungsten</td>
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<tr>
<td>TLM</td>
<td>transfer length method / transmission line method</td>
</tr>
<tr>
<td>UMOSFET</td>
<td>U-shaped groove MOSFET</td>
</tr>
<tr>
<td>UV</td>
<td>ultraviolet</td>
</tr>
<tr>
<td>VCR</td>
<td>video cassette recorder</td>
</tr>
<tr>
<td>VJFET</td>
<td>vertical JFET</td>
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<tr>
<td>XPS</td>
<td>X-ray photoelectron spectroscopy</td>
</tr>
<tr>
<td>XRD</td>
<td>X-ray diffraction</td>
</tr>
</tbody>
</table>
CHAPTER 1

Introduction

Solid-state devices such as transistors can be found almost everywhere in our daily lives not to mention mobile phones and computers. In fact, the era of solid-state electronics had already begun with the invention of the transistor in 1947 by John Bardeen, Water Brattain, and William Shockley[1-3]. Although the basic idea of the field-effect transistor (FET) has been known by J. E. Lilienfeld in as early as 1925[4], the theoretical description of a FET made by Shockley in 1952[5] paved the way for development of a classic electronic device which provides the designer the means to accomplish nearly every circuit function. The field-effect transistor has also been known as a “unipolar” transistor because the current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor (BJT) carriers of both polarities (majority and minority) are involved. In the early 60s, the integrated circuit (IC) was developed by incorporating many transistors and other components on a single small chip of semiconductor material. Since then, IC technology has been continuously developed and improved to date. The early solid-state devices used germanium (Ge) because it was relatively simple to produce the single-crystal material. Silicon (Si) had more desirable properties such as a wider energy bandgap and a stable natural oxide that can be used as a mask, an isolation barrier, or as a gate dielectric in field effect transistors. Although Si was difficult to manufacture due to its higher melting point, it replaced Ge and the rate of development of Si devices was phenomenal once those early problems were solved.

Today we are still working with Si and SiO2 in solid-state electronics including FETs. However, new materials are required for some special applications, since the characteristic properties of material play a key role for the performance of the fabricated electronic devices. Silicon carbide (SiC) is one of such promising materials for niche applications.

Recently, SiC has drawn much attention due to its interesting physical properties[6-9]. It possesses extreme thermal stability, wide energy bandgap, and high breakdown field and SiC devices offer great advantages to overcome the physical device limitations in Si devices: Due to its large band gap (3.0-3.3 eV, depending on polytype), SiC possesses a
very high breakdown field and low intrinsic carrier concentration, which consequently makes high voltage and high temperature operation possible. SiC is also suitable for high frequency device applications, thanks to the high saturation drift velocity and low permittivity. SiC is the only compound semiconductor, which can be thermally oxidized to form a high quality native oxide (SiO₂). This makes it possible to fabricate metal-oxide-semiconductor (MOS)-gated devices in SiC. Although SiC has been known since the first observation by Jöns Jacob Berzelius in 1824[10], it was in the late 80s that SiC wafers became commercially available after the breakthrough had been made in growth technology[7]. Up to now the material quality and the diameter of silicon carbide wafers have steadily been improved and the micro-pipe densities have been reduced to 10 cm⁻² at production level (0.9 cm⁻² for a 50mm 4H-SiC wafer in research stage)[11, 12]. This is promising for future fabrication of larger than millimeter-sized devices. Presently, 6H- and 4H-SiC wafers of n- and p-type with a diameter of 50 mm are readily available in low resistivity and semi-insulating forms while 75 mm wafers are entering commercialization. 100-mm diameter wafers are only shown at research level. Most of the key SiC process technologies including doping, dry etching, oxide growth, Schottky and Ohmic contacts, are relatively mature and compatible to those in Si processing[13]. However, there are still some key processing issues that are critical to be overcome for device commercialization.

The advances in SiC technology have enabled the field effect transistor (FET) to be demonstrated for power electronics and sensor applications with relatively low leakage currents, large breakdown voltages and high temperature operations. Applications of SiC FETs in the electrical power systems include motor drives, switch-mode power supplies, high-voltage DC current transmission systems, electronics for vehicles and traction, active filters and flexible power generation. Several types of FET technologies have been demonstrated in SiC so far[8, 14-16], but the excessive reverse-bias Schottky gate leakage of metal-semiconductor field effect transistors (MESFETs) at high temperature is a factor which restricts their use. The junction field-effect transistors (JFETs), being unipolar devices without any Schottky gates, have advantages due to the higher barrier and inherent stability of the p-n junction gates[17, 18].

In SiC device technology one interesting issue is to use deposited insulators. So far, dielectrics including AlN and TiO₂ have been investigated on SiC, which shows that the best performance was obtained when those deposited insulators are integrated with SiO₂[19]. Ferroelectrics are a special kind of dielectric material that can be deposited on semiconductors. In ferroelectrics, the spontaneous polarization can be switched by an externally applied electric field, and thus are attractive for nonvolatile memory and sensor applications. Ever since the first metal-ferroelectric-semiconductor (MFS) field effect transistor was demonstrated in Si by Wu in 1974[20], silicon has long been studied to be integrated with ferroelectric thin films for MFS field-effect devices. There has been recent interest in utilizing ferroelectrics above room temperature and in severe environment. In such cases, high temperature polarization behavior and retention of ferroelectric thin films are critical factors to be explored. Therefore ferroelectric devices in SiC may offer great advantages to overcome the physical limitations of those in Si, which are set by its material properties. The first ferroelectric-field effect transistors (FeFETs) in SiC are presented in this thesis.
The objective of this thesis is on the design and process issues for junction-, MOS- and ferroelectric- field effect transistors in SiC, which potentially can be used as high power and high temperature devices. In this work, 4H-SiC buried-gate JFETs have been fabricated and characterized, whereas in earlier work those devices have been studied mainly in 6H-SiC. Moreover, junction-gated MOS field effect transistors (J-MOSFETs) have been proposed and fabricated to improve high-temperature stability in terms of current level and improved current density by accumulating the channel. Most of all, the FeFETs have been demonstrated for the first time in SiC. In Chapter 2, the material properties of SiC are discussed together with those of ferroelectrics. Chapter 3 describes the basic process steps for fabricating devices in SiC and integrating ferroelectrics. Chapter 4 covers the materials and electrical characterization for the structures studied in the thesis. The fabricated device structures and their characterization results are discussed in chapter 5. Finally Chapter 6 gives a summary and future outlook.
CHAPTER 2

Materials Properties

In this chapter the basic materials properties and the advantages of SiC and ferroelectrics are discussed. Physical models and parameters of SiC for device simulations are also presented with the values based on the recent literature, which are applicable to electronic devices.

2.1 Properties of SiC

2.1.1 Crystal Structures and Polytypes

Crystal structure is the arrangement of atoms in a solid-state material in a regular repeatable pattern or an ordered arrangement. Most crystal structures can be described using a unit cell, which represents the locations of all atoms in the crystal. SiC has complex structures to satisfy the directional restraints imposed by the bonding. SiC occurs in so called zinc-blende or sphalerite structure[21] as shown in Fig. 2.1.

Fig. 2.1 The (a) diamond and (b) zinc blende unit cell. For SiC, the large bright atoms are Si and the small dark atoms are C. The tetrahedral bonding of (c) C atom surrounded by 4 Si atoms and (d) Si atom with nearest 4 C atoms are shown as well.
SiC is composed of silicon and carbon, which are group IV elements. Si and C are bonded covalently in SiC, which means that every atom has exactly four neighbors, and the atom bonds are in four directions. The carbon atom is situated at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms or vice versa as shown in Fig. 2.1 (c) and (d). The distance between the C atom and each of the Si atoms is approximately 1.89 Å and the distance between neighboring of same kinds of atoms (Si or C) is around 3.08 Å. Compared to Si or GaAs, one of the distinct features of SiC is that it is not as symmetric in three dimensions. The stack in a SiC unit cell does not alternately repeat itself and the stacking order (so-called ‘polytype’) of planes of unit cell differs in the same material.

Fig. 2.2 The different order of stacking in SiC is shown: (a) The position of the first layer of atoms of Si and C is illustrated as A whereas the next layers can be shown as B and C. The top- and side-view of 3C-, 4H-, and 6H-polytype stacks are shown in (b), (c), and (d), respectively.
Three different planes of A, B, and C can be defined as shown in Fig. 2.2 (a), where each layer is a double layer of Si and C atoms. Different polytypes are referred by using the Ramsdell notation[22]: For example, if it has two repeating layers and a hexagonal structure, it is referred to as 2H SiC. The top-view and side-view of the stacking order for 3C, 4H, and 6H polytypes are illustrated in Fig. 2.2 (b), (c), and (d) respectively. If we instead stack the layers ABC etc, we have a cubic crystal when viewed along an axis diagonal to the hexagonally close packed plane, and it is referred to as 3C (see Fig. 2.2 (b)). Similarly, stacking orders of ABAC and ABCACB are called 4H and 6H, respectively (see Fig. 2.2 (c) and (d)). Among over 500 known polytypes in SiC, $\beta$-SiC denotes the polytype of 3C-SiC, and $\alpha$-SiC refers to all the others including 6H- and 4H-SiC.

As shown in Fig. 2.3, Miller indices for hexagonal crystal structures are given by using a four-axis coordinate system with principal axes of $a_1$, $a_2$, $a_3$ and $c$. The sum of the reciprocal intercepts with $a_1$, $a_2$ and $a_3$ is zero. The three $a$-vectors (with 120° angles between each other) are all in the close packed plane of the double layers, also called the $a$-plane, whereas the $c$-axis is perpendicular to this plane. There are two different faces of Si $<0001>$ and C $<000\bar{1}>$ perpendicular to the $c$-axis[23], and Si-faced SiC is commonly used for device applications due to its better quality of epitaxial layers grown on this face. SiC bulk material is generally cut and polished 3–8 degrees off-axis towards $<11\bar{2}0>$ to avoid the growth of 3C inclusions in the epitaxial layers of 6H- or 4H-SiC, by means of using the so-called ‘step-controlled epitaxy’[24].
2.1.2 Figures of Merit

SiC exhibits higher values of thermal conductivity (3-13 times), critical electric field (2-10 times), and saturated carrier velocity (2-2.5 times) compared to other semiconductor materials such as Si or GaAs. The physical properties of SiC and other semiconductor materials are summarized[24-27] in Table 2.1.

Because of its high bond strength and hardness, SiC is physically rugged and chemically inert. The energy bandgap is quite different for the different polytypes of SiC, varying from 2.2 to 3.4 eV. SiC is an indirect bandgap semiconductor and the optical properties do not vary much among the different polytypes. For high temperature devices, a wide bandgap is certainly an advantage since the thermal generation of electron-hole pairs is low. Thanks to its wide bandgap, SiC has an intrinsic temperature over 900 °C (depending on polytype and doping). At these temperatures the devices are more likely to stop working due to other problems such as contact or package failure. The impact ionisation energy is also high in SiC, which means that a very high electric field can be reached without avalanche multiplication of ionised carriers.

Table. 2.1 Comparison of mechanical and electrical properties of SiC and other semiconductors

<table>
<thead>
<tr>
<th>Properties</th>
<th>Si</th>
<th>GaAs</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>2H-GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ [eV]</td>
<td>1.12</td>
<td>1.43</td>
<td>2.4</td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
<td>5.5</td>
</tr>
<tr>
<td>Lattice const. [Å]</td>
<td>a=5.43</td>
<td>a=5.65</td>
<td>a=4.36</td>
<td>a=3.08</td>
<td>c=15.12</td>
<td>c=10.08</td>
<td>c=5.185</td>
</tr>
<tr>
<td>Critical field $E_c$ [MV/cm]</td>
<td>0.25</td>
<td>0.3</td>
<td>2.0</td>
<td>2.5</td>
<td>2.2</td>
<td>3.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Sat. velocity $v_{sat}$ [10^7 cm/s]</td>
<td>1.0</td>
<td>1.0</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
<td>2.5</td>
<td>2.7</td>
</tr>
<tr>
<td>Electron mobility $\mu_n$ [cm²/Vs]</td>
<td>1300</td>
<td>8500</td>
<td>1000</td>
<td>415</td>
<td>947</td>
<td>400</td>
<td>2200</td>
</tr>
<tr>
<td>Hole mobility $\mu_p$ [cm²/Vs]</td>
<td>480</td>
<td>400</td>
<td>40</td>
<td>80</td>
<td>120</td>
<td>30</td>
<td>1600</td>
</tr>
<tr>
<td>Dielectric Const. $\varepsilon_r$</td>
<td>11.9</td>
<td>13.0</td>
<td>9.7</td>
<td>10.0</td>
<td>10.0</td>
<td>9.5</td>
<td>5.0</td>
</tr>
<tr>
<td>Thermal cond. $\lambda$ [W/cmK]</td>
<td>1.5</td>
<td>0.5</td>
<td>3.5-5.0</td>
<td>3.5-5.0</td>
<td>3.5-5.0</td>
<td>1.3</td>
<td>20.0</td>
</tr>
<tr>
<td>Th. exp. coeff. [10⁶%/K]</td>
<td>2.6</td>
<td>5.73</td>
<td>3.0</td>
<td>4.5</td>
<td>5.6</td>
<td>5.6</td>
<td>0.8</td>
</tr>
<tr>
<td>Density [g/cm³]</td>
<td>2.3</td>
<td>5.3</td>
<td>3.2</td>
<td>3.2</td>
<td>3.2</td>
<td>6.1</td>
<td>3.5</td>
</tr>
<tr>
<td>Melting point [°C]</td>
<td>1420</td>
<td>1240</td>
<td>2830</td>
<td>2830</td>
<td>2830</td>
<td>2500</td>
<td>4000</td>
</tr>
<tr>
<td>Direct/Indirect</td>
<td>I</td>
<td>D</td>
<td>I</td>
<td>I</td>
<td>I</td>
<td>D</td>
<td>I</td>
</tr>
</tbody>
</table>
As SiC has a critical electric field around ten times higher than that of Si, the breakdown voltage $V_B = E_C W/2$ can be ten times higher for the same depletion width. Similarly, for the same breakdown voltage design, a 10 times thinner depletion region or 100 times higher doping in the low-doped region of a $p-n$ junction can be realized in SiC. As a result, a simple calculation of the unipolar on-resistance $R_{on} = W/q \mu_n N_D = 4V_B^2/\varepsilon E_C^3$ for the low-doped region gives 1000 times lower values by using a 10 times thinner depletion region and 100 times higher doping (see Fig. 2.4). In the actual case, however the electron mobility $\mu_n$ and dielectric constant $\varepsilon$ are lower in SiC than in Si, and the advantage is between 200 and 400 depending on the polytype[24]. Moreover, high-frequency SiC devices can exhibit better performance than in Si due to the higher saturated drift velocity $v_{sat}$ (delay time $\tau = W/v_{sat}$) and lower permittivity $\varepsilon_r$ (capacitance $C \propto \varepsilon_r$). In principle, the high thermal conductivity $\lambda$ of SiC allows higher power densities as compared to Si and GaAs[24, 32]. A higher thermal flow ($P/A$, where $P$ is the power dissipation and $A$ is the area normal to heat flow) can be provided for the same amount of junction temperature increase $\Delta T = P \cdot t / (A \cdot \lambda)$, where $t$ is the thickness).

These properties are thus desirable for efficient high power, high temperature and high frequency device operation in harsh environments. Among several SiC polytypes, 4H-SiC is the most attractive one due to the higher carrier mobility and more isotropic nature of its properties. Several figures of merit (FM) have been suggested to further quantify the intrinsic performance of power devices are shown in Fig. 2.5 and table 2.2. The critical field and thermal conductivity as well as carrier mobility are important physical parameters for FMs. A low frequency FM (e.g. BFM) shows 10–100 times improvement over Si due to lower on-resistance. Better values of high frequency FM (i.e. BHFM) results from the reduced capacitance with decreased active area. Considering also other FMs (i.e. QF and JFM), it is clear that SiC semiconductor power devices can operate at a
higher temperature, a higher frequency and a lower power loss, combined with a less stringent heat-sinking requirement than silicon devices.

**Fig. 2.5** Normalized figures of merit for different semiconductors

**Table 2.2** List of Figures of Merits (FMs)

<table>
<thead>
<tr>
<th>Name</th>
<th>Year</th>
<th>Equation</th>
<th>Note</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFM (Johnson’s FM)</td>
<td>'65</td>
<td>$\frac{E_B^2 v_{sat}}{4\pi^2}$</td>
<td>High frequency and power capability of transistors</td>
<td>Johnson et al.[28]</td>
</tr>
<tr>
<td>KFM (Keyes’ FM)</td>
<td>'72</td>
<td>$\lambda \sqrt{\frac{C_0 v_{sat}}{4\pi\varepsilon_S}}$</td>
<td>Taking account the switching speed of transistor and its thermal limitation due to generated heat</td>
<td>Keyes et al.[29]</td>
</tr>
<tr>
<td>BFM (Baliga’s FM)</td>
<td>'82</td>
<td>$\varepsilon \mu E_C^3$</td>
<td>Low frequency (Considering the on-resistance of Power FETs)</td>
<td>Baliga et al.[30]</td>
</tr>
<tr>
<td>BHFM (Baliga’s High Frequency FM)</td>
<td>'89</td>
<td>$\mu E_C^2$</td>
<td>High frequency (Considering switching losses as well)</td>
<td>Baliga et al. [6]</td>
</tr>
</tbody>
</table>
| Thermal QF (Thermal Quality Factors) | '89  | $Q_{F1} = \lambda \sigma_A$  
$Q_{F2} = \lambda \sigma_A E_C$  
$Q_{F3} = \sigma_A$ | Considering thermal properties | Shenai et al.[31]        |
2.2 Electrical Models for SiC

2.2.1 Band Structure

The electron band structure and effective masses in SiC are complex because several non-parabolic bands in reciprocal k-space are to be considered. It has been observed that the exact theoretical band structure calculations vary in different works. The small variations in the atomic positions of the hexagonal planes affect the spin-orbit splitting and crystal-field splitting [33] and stacking faults may have to be considered[34]. However, the effective electron and hole masses are not significantly affected and they are given as in Eq. 2.1 by assuming parabolic bands [35]. The model for the temperature dependent energy gap for 4H-SiC is taken from 6H-SiC, the room temperature value of $N_C$ and $N_V$ were taken from references[36] and calculating the density of states gives $1.67 \times 10^{19}$ and $3.19 \times 10^{19}$ for $N_C$ and $N_V$, respectively.

$$N_C(T) = 2 \left( \frac{2\pi m_{de}kT}{\hbar^2} \right)^{3/2}$$ [Eq. 2.1a]

$$N_V(T) = 2 \left( \frac{2\pi m_{dh}kT}{\hbar^2} \right)^{3/2}$$ [Eq. 2.1b]

Table 2.3 Bandgap-related physical properties of SiC and Si

<table>
<thead>
<tr>
<th></th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$, $T=300$ K (eV)</td>
<td>3.26</td>
<td>3.0</td>
<td>1.08</td>
</tr>
<tr>
<td>$dE_g/dT$ (eV/K)</td>
<td>$-3.3 \times 10^{-4}$</td>
<td>$-3.3 \times 10^{-4}$</td>
<td>$-4.73 \times 10^{-4}$</td>
</tr>
<tr>
<td>$m_{de}$</td>
<td>$0.76 m_0$</td>
<td>$2.3 m_0$</td>
<td>$m_0$</td>
</tr>
<tr>
<td>$m_{dh}$</td>
<td>$1.20 m_0$</td>
<td>$m_0$</td>
<td></td>
</tr>
</tbody>
</table>

The obtained values are very close to the values based on the multiple-band model[37]. The intrinsic carrier concentration $n_i$ is determined by the energy gap $E_g$ and by the conduction and valence band density of states, $N_C$ and $N_V$, respectively.

$$n_i = \sqrt{N_C N_V} \exp \left( -\frac{E_g}{2kT} \right)$$ [Eq. 2.2]

The intrinsic carrier concentration $n_i$ of SiC is extremely low (less than 1 cm$^{-3}$ at room temperature) due to its wide bandgap. Because of the low value of intrinsic carrier concentration, SiC devices can operate at higher temperature than other materials as shown in Fig. 2.6. The horizontal line shows the temperature where devices may stop working since $n_i$ exceeds the background doping concentration (e.g. typically $10^{14}$ cm$^{-3}$ for the low-doped region of power devices).
2.2.2 Dopants and Incomplete Ionization

As in silicon, dopant atoms can be selected from group III and V in the periodic table for $p$-type and $n$-type SiC, respectively. However, the energy levels of dopants are much deeper than in Si and therefore the dopants are not fully ionized at room temperature in SiC\cite{25, 38-42}. This effect is also known as the dopant freeze-out in Si at low temperatures\cite{43}. The ionization energies of commonly used dopant atoms in SiC are shown in table 2.4.

### Table 2.4 Dopants in SiC and their ionization energy with the lattice site.

<table>
<thead>
<tr>
<th>Type</th>
<th>Dopant</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n$ (Donors)</td>
<td>N</td>
<td>42 (hex), 84 (cub)</td>
<td>82 (hex), 137 (cub)</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>53 (hex), 93 (cub)</td>
<td>82 (hex), 115 (cub)</td>
<td>45</td>
</tr>
<tr>
<td>$p$ (Acceptors)</td>
<td>B</td>
<td>285</td>
<td>300</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>Al</td>
<td>191</td>
<td>210</td>
<td>67</td>
</tr>
<tr>
<td></td>
<td>Ga</td>
<td>281</td>
<td>290</td>
<td>72</td>
</tr>
</tbody>
</table>
Al (substituting on Si site) and N (substituting on C site) are the most common acceptor and donor impurities for SiC, respectively. Doping with nitrogen (N) leads to a donor with two different energy levels below the conduction band due to the existence of two different lattice sites, one with cubic surrounding and the other with hexagonal surrounding. A nitrogen atom sitting on these sites will therefore give rise to different ionization energies. In actual simulations, these two donor levels can be lumped together and replaced by a single level[35]. P is known for its superior activation to Nitrogen at high dopant concentrations.

The ionization rate is given by[44]

\[
I_D(E_D) = \frac{N_D^+}{N_D} = -1 + \sqrt{1 + 4g_c N_D \exp \left( \frac{E_C - E_D}{kT} \right)}
\]

[Eq. 2-3]

where \(E_C-E_D\) is the energy difference between the conduction band minimum and the donor level, and \(N_D^+\) is the number of ionized donors. For donor levels of 4H-SiC at 300K, \(E_C-E_D=69\text{meV}\) with donor level generacy factor, \(g_c=2\), and the effective density of the states in the conduction band, \(N_C=1.7\times10^{19}\text{cm}^{-3}\) is used (\(E_C-E_D=72\text{meV}\) when the incomplete ionization is not considered[35]). The shallowest p-type doping can be achieved with Al acceptors (\(E_A-E_V=191\text{meV}\) for 4H-SiC with \(g_c=4\)), while \(E_A-E_V=281\text{meV}\) is reported for Ga[40]. The calculated values of \(I_D\) as a function of temperature are shown in Fig. 2.7. In the simulation, Poisson’s Equation is solved for the ionized impurity concentrations (\(N_D^+, N_A^\)).

![Fig. 2.7 Calculated degree of ionization \(I\) as a function of the temperature for nitrogen and phosphorus doping of n-type 4H- and 6H-SiC(24).](image)
2.2.3 Bandgap Narrowing

At high doping levels, carrier-carrier interaction, carrier-impurity interaction, and overlap of the electron wave functions can cause alteration of the band structure. As a result, the bandgap decreases as the doping increases. This ‘bandgap narrowing’ has not been measured for SiC but theoretically studied for different polytypes of SiC by Person et al. [45] and Lindefelt[46].

The bandgap narrowing is caused both by doping and by carrier injection, and can be obtained by extracting the valence band and conduction band change as a function of ionized dopant concentration or carrier concentration for 3C, 4H-, and 6H-SiC.

\[
\Delta E_g = A_x \left( \frac{\Xi}{N_0} \right)^{\frac{1}{k}} + B_x \left( \frac{\Xi}{N_0} \right)^{\frac{1}{l}} \tag{Eq. 2-4}
\]

where \( \Xi \) is the controlling property of the bandgap narrowing, and \( A, B, N_0, k, \) and \( l \) are fitting parameters where \( k \) and \( l \) are positive integers.

However, most of the commercial simulators only allow the symmetrical narrowing of the bandgap, depending only on the chemical dopant concentration. Generally a model that is valid for Si is borrowed for simulations of SiC devices because of the similarity between Si and SiC.

\[
\Delta E_g = 9 \cdot 10^{-3} \left\{ \ln \frac{N}{1 \cdot 10^{17}} + \left[ \ln \frac{N}{1 \cdot 10^{17}} + 0.5 \right]^2 \right\} \tag{Eq. 2-5}
\]

2.2.4 Mobility

The low field mobility is dependent on the doping and can be given as

\[
\mu_{n,p} = \mu_{n,p,min} \left( \frac{T}{300} \right)^{\alpha_{n,p}} + \frac{\mu_{n,p,max}}{1 + \left( \frac{N_D + N_A}{N_{n,p,ref}} \right)} \left( \frac{T}{300} \right)^{\alpha_{n,p}} \tag{Eq. 2-6}
\]

where \( N_D \) and \( N_A \) are the density of donors and acceptors respectively.

The parameter values for different materials are listed in table 2.5. The mobilities are plotted in Fig. 2.8 (a) and (b) for \( \mu_n \) and \( \mu_p \), respectively (perpendicular to the \( c \)-axis). The mobility is more anisotropic for 6H-SiC than it is for 4H-SiC. The ratio between the electron mobilities perpendicular and parallel to the \( c \)-axis are 0.83 for 4H-SiC and 5 for 6H-SiC[35, 47]. The high electron mobility in 4H-SiC and its small anisotropy favor using this polytype. The low field mobility in SiC is not high compared to other semiconductor materials. Nevertheless, at high fields, the carrier drift velocity \( v \) saturates due to the increase of the optical phonon scattering and reaches the saturation velocity \( v_{sat} \), which is
two times higher than in Si. The high field mobility in SiC can be described by the same model as Si (see Table 2.5 for the relevant parameters):

\[
\mu_{n,p}(E) = \frac{\mu_{n,p}^0}{1 + \left(\frac{\mu_{n,p}^0 E}{v_{sat}}\right)^{\gamma/\beta}} \tag{Eq. 2-7}
\]

<table>
<thead>
<tr>
<th>Si</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mu_{n,min} [\text{cm}^2/\text{Vs}])</td>
<td>92</td>
<td>20</td>
</tr>
<tr>
<td>(\mu_{n,max} [\text{cm}^2/\text{Vs}])</td>
<td>1300</td>
<td>415(\perp_c)</td>
</tr>
<tr>
<td>(N_{n,ref} [\text{cm}^3])</td>
<td>1.3(\times 10^{17})</td>
<td>4.5(\times 10^{17})</td>
</tr>
<tr>
<td>(\gamma_n)</td>
<td>0.91</td>
<td>0.45</td>
</tr>
<tr>
<td>(\alpha_n)</td>
<td>-2.42</td>
<td>-3</td>
</tr>
<tr>
<td>(\mu_{p,min} [\text{cm}^2/\text{Vs}])</td>
<td>52</td>
<td>6.8</td>
</tr>
<tr>
<td>(\mu_{p,max} [\text{cm}^2/\text{Vs}])</td>
<td>453</td>
<td>99</td>
</tr>
<tr>
<td>(N_{p,ref} [\text{cm}^3])</td>
<td>1.9(\times 10^{17})</td>
<td>1(\times 10^{19})</td>
</tr>
<tr>
<td>(\gamma_p)</td>
<td>0.63</td>
<td>0.5</td>
</tr>
<tr>
<td>(\alpha_p)</td>
<td>-2.2</td>
<td>-3</td>
</tr>
</tbody>
</table>

**Fig. 2.8** Calculated mobility values for (a) electron and (b) hole in 4H-SiC as a function of doping concentration at different temperatures.
2.2.5 Recombination

Although the majority carrier concentration is close to the number of ionized doping atoms, a further consideration of recombination and generation is required in terms of thermal equilibrium. Upon the injection of excess carriers, recombination of the injected carriers restores the equilibrium. Shockley-Read-Hall (SRH) recombination is a process with phonon transitions via defects or traps. The SRH recombination rate is given by

$$R_{\text{SRH}} = \frac{np - n_i^2}{\tau_p (n + n_i \exp(E_{\text{Trap}} - E_C)) + \tau_n (p + n_i \exp(E_v - E_{\text{Trap}}))}$$  \[\text{Eq. 2-8}\]

where the life times $\tau_n$ and $\tau_p$ (for electrons and holes respectively) can be described by the Selberherr relation\[49\].

$$\tau_n = \frac{\tau_{n0}}{1 + \left(\frac{N_D + N_A}{N_{n\text{SRH}}^0}\right)}$$  \[\text{Eq. 2-9}\]

Lifetimes in the order of 1-100ns have been observed for 6H-SiC\[50\]. The relation between the electron lifetime and hole lifetime for Si may also be used for SiC\[35, 44\].

$$\tau_n = 5\tau_p$$  \[\text{Eq. 2-10}\]

Auger recombination occurs at high doping levels due to the direct band-to-band recombination between an electron and a hole across the band gap, accompanied by the transfer of energy to another free electron or hole. The Auger recombination rate is given by

$$R_{\text{AU}} = (C_p p + C_v n)(np - n_i^2)$$  \[\text{Eq. 2-11}\]

where the Auger coefficient for electrons in 4H-SiC is $C_v=5\cdot10^{-31}$ [cm$^6$s$^{-1}$] at RT leading to $C_p=2.0\cdot10^{-31}$ [cm$^6$s$^{-1}$]\[51, 52\].

2.2.6 Impact Ionization

If the field across a $p$-$n$ junction is high enough, impact ionization occurs since carriers can gain enough kinetic energy to collide and break the bonds thereby creating additional electron-hole pairs. There exist reported values of measured impact ionization for 6H-SiC and 4H-SiC\[51, 53, 54\]. The maximum electric field (critical field; $E_C$) and the blocking voltage ($V_B$) are determined by the impact ionization rate $\alpha_n$ and $\alpha_p$ for electrons and holes respectively. Unlike Si, SiC shows a lower impact ionization rate for electrons than for holes. The ionization integral is given by
\begin{align*}
\int_0^w \left[ \alpha_n(x) \exp \left( \int_a^x \left( \alpha_n(x) - \alpha_p(x) \right) dx \right) \right] dx &= 1 \\
\text{where} & \quad \left\{ \begin{array}{l}
\alpha_n(x) = a_n \exp \left( -\frac{b_n}{E(x)} \right) \\
\alpha_p(x) = a_p \exp \left( -\frac{b_p}{E(x)} \right)
\end{array} \right. \quad [\text{Eq. 2-12}]
\end{align*}

The breakdown voltage is then deduced by solving the equation above for the depletion width at breakdown \( W \). The values need to be calculated numerically, as there is no closed solution. The electric field and the voltage across an abrupt \( p^+ - n \) junction is given by\[43\]

\begin{align*}
E(x) &= \frac{qN_D}{\varepsilon_s} (W - x), \quad 0 < x < W \quad [\text{Eq. 2-13}]
V(x) &= \frac{qN_D}{\varepsilon_s} \left( Wx - \frac{x^2}{2} \right) \quad [\text{Eq. 2-14}]
\end{align*}

From the values of \( W \) and the corresponding \( N_D \), the critical field and the breakdown voltage can be obtained as

\begin{align*}
E_{\text{max}} &= \frac{qN_D W}{\varepsilon_s} \quad [\text{Eq. 2-15}]
V_n &= V(x) \bigg|_{x=W} = \frac{qN_D W^2}{2\varepsilon_s} \quad [\text{Eq. 2-16}]
\end{align*}

The critical field for the given impurity concentration of \( 10^{15} < N_D < 10^{18} \) is known as

\[ E_{\text{CR}} = \frac{E_{\text{CR,Ref}}}{1 - \frac{1}{4} \log_{10} \left( \frac{N_D}{N_{\text{Ref}}} \right)} \quad [\text{Eq. 2-17}] \]

The total impact ionization rate can be given by

\[ G^\Pi = \alpha_n \frac{\bar{J}_n}{q} + \alpha_p \frac{\bar{J}_p}{q} \quad [\text{Eq. 2-18}] \]

In 6H-SiC, the breakdown behavior is reported to be anisotropic, which means that the critical field parallel to the \( c \)-axis \( (E_c) \) is half the critical field perpendicular to the \( c \)-axis \( (E_\perp) \). For simulations in this work, the specific impact ionization parameters have been used from Ref. [25, 53].
2.2.7 Physical simulations of SiC devices

As described so far in this chapter, the material data from recent publication are used for SiC device simulations in this thesis. The physical models in the simulation software are basically based on Si device technology. Therefore the model parameters in the simulators have been adjusted for the closest agreement with the physical models for 4H-SiC. However, it has to be noted that the published models and experimental data for 4H-SiC are still far from complete. The simulators used in this work were ATLAS from SILVACO International[55], MEDICI from TMA (currently Synopsys Inc.)[56], and DESSIS from ISE Inc[57]. The physical models can be mostly implemented in all three simulators. In MEDICI, anisotropic properties are relatively easily handled and a faster convergence is achieved whereas ATLAS and DESSIS have a superior graphical interface. The simulation is accomplished by solving the Poisson’s equation and the continuity equations based on the Boltzmann carrier transport theory. The heat flow equation can be included for simulations in case the thermal effect is considered.

Poisson’s equation which takes account of the electrostatic potential $\psi$ and the charge carriers is given by

$$\epsilon \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) - \rho_S$$  \[Eq. 2.19\]

where $\epsilon$ is the dielectric constant of semiconductor material. For anisotropy, $\epsilon$ can have a tensor property.

The continuity equations for electrons and holes are given as

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n - U_n = f_n(\psi, n, p)$$  \[Eq. 2.20\]

$$\frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_p - U_p = f_p(\psi, n, p)$$  \[Eq. 2.21\]

where $U_n$ and $U_p$ are net electron and hole recombination, respectively.

The electron and hole current density equations based on Boltzmann transport theory are:

$$\vec{J}_n = -q\mu_n n \nabla \phi_n = q\mu_n \vec{E}_n + qD_n \nabla n$$  \[Eq. 2.22\]

$$\vec{J}_p = -q\mu_p p \nabla \phi_p = q\mu_p \vec{E}_p + qD_p \nabla p$$  \[Eq. 2.23\]

In the continuity equations, Shockley-Read-Hall and Auger recombination models are used. The concentration and temperature dependent low-field and high-field mobilities are considered as well as impact ionization. The incomplete ionization due to the carrier freeze-out and the temperature dependent intrinsic concentration, energy bandgap, effective density of states are modeled as well.

$$\rho C_p \frac{\partial T}{\partial t} = \nabla k \nabla T + H$$  \[Eq. 2.24\]
In the heat flow equation shown in Eq. 2.24, $\rho$, $C_p$, $k$, and $H$ are the specific mass density, and specific heat of the material, thermal conductivity and locally generated heat, respectively. By solving the heat flow equation combined with the basic semiconductor equations, all the physical parameters become temperature dependent and electro-thermal simulation can be performed. This equation can be disregarded unless self-heating is of interest for the simulation.

### 2.3 Properties of Ferroelectrics

#### 2.3.1 Ferroelectricity

Ferroelectrics are a special group of dielectric materials which are spontaneously polarized and possess the ability to switch their internal polarization upon the application of an electric field. In a normal dielectric material, positive and negative charges will be displaced from their original position (a concept characterized by the dipole moment or polarization) by an electric field. However, this polarization will disappear when the electric field returns back to zero.

According to the elements of symmetry, a crystal may belong to one of 230 space groups, 32 point groups (=crystal classes), 14 Bravais lattices, and 7 crystal systems. The structural symmetry of a crystal affects both structural and physical properties of the material. Fig. 2.9 shows the various properties of dielectric materials. Among 32 crystalline lattices with dielectric properties, there are 20 point groups, which do not have centrosymmetry and exhibit piezoelectric effects. When a dimensional change is imposed on the piezoelectric materials, polarization occurs and a voltage or field is created. Half of the piezoelectric classes of materials, i.e. 10 of the original crystal classes have a permanent value of polarization in the absence of an applied electric field or stress[58, 59].

![Fig. 2.9 Schematics of various sub-class of dielectric materials.](image-url)
The polarization can be defined by the value of the dipole moment per unit volume or by the value of the charge per unit area on the surface perpendicular to the polarization axis. As illustrated in Fig. 2.10, the direction of this polarization can be reversed or reoriented by applying an appropriate electric field. A good analogy to ferroelectric materials is ferromagnetic materials. The magnetization in ferromagnetic materials is spontaneous and reorientable, which is similar to the polarization in ferroelectrics. The direction of magnetization can be switched from one state to another by applying an appropriate magnetic field[60].

An appropriate electric field is able to displace the central atom from its previous stable position and to change the polarization state of the unit cell. Although the polarization of each individual unit cell is tiny, the net polarization of several domains (each of which comprises a number of aligned unit cells) can be large enough to be detected using regular sensing amplifiers.

2.3.2 Lead Zirconate Titanate, PZT

The general chemical formula for perovskite ferroelectrics is ABO₃, where A represents a cation with a larger ionic radius, and B a cation with a smaller ionic radius. Perovskite ferroelectrics can have either tetragonal or orthorhombic structures. Most of the perovskite ferroelectrics are compounds with either A²⁺B⁵⁺O₃²⁻ or A¹⁺B³⁺O₃²⁻ type formula. The A³⁺B⁵⁺O₃²⁻ formula has not been observed with ferroelectrics. One of the most studied, important group of perovskite ferroelectric materials are lead based ferroelectric materials, such as Pb(ZrₓTi₁₋ₓ)O₃ of which the unit cell is shown in Fig. 2.10.

Fig. 2.11 is the temperature-composition T-x phase diagram of the PZT pseudo-binary system, where the curie temperature Tₕ-line is the boundary between the cubic paraelectric phase and the ferroelectric phase. A morphotropic phase boundary divides the region of the ferroelectric phase into two parts: a tetragonal phase region on the Ti rich side and a rhombohedral phase region on the Zr rich side. At room temperature, the boundary is at the point of Zr/Ti = 53/47. In the region where Zr/Ti lies between 100/0 to 96/4, the solid solution is an antiferroelectric orthorhombic phase exhibiting no observable piezoelectric effect.

![Fig. 2.10 Two stable states in a cubic perovskite ferroelectric material of Pb(ZrₓTi₁₋ₓ)O₃](image-url)
Chapter 2. Materials Properties

Fig. 2.11 Phase diagram of PbTiO$_3$-PbZrO$_3$ system (after Jaffe et al.[61]).

Fig. 2.12 Composition dependence of dielectric constant and electromechanical coupling factor of PZT ceramic[62].
The lattice parameters of PZT changes abruptly near the morphotropic phase boundary, where some physical properties, such as the dielectric permittivity and the electromechanical coupling factor show anomalous behaviors (see Fig. 2.12). This indicates the presence of a strong cooperative interaction between localized moments leading to a large relative permittivity in compositions near the morphotropic phase boundary. The films of PZT-compounds have been extensively studied as promising material for nonvolatile memory devices and sensors.

2.3.3 Polarization and Hysteresis

The polarization can be defined as:

$$P(r) = \lim_{\Delta v \to 0} \frac{\sum p}{\Delta v}$$

[Eq. 2.25]

where the dipole moment $p$ for two opposite point charges is defined as $p=QI$. $Q$ is the charge magnitude of each point charge and $I$ is the spatial vector from the negative to the positive point charge. $\Delta v$ is the volume over which the average is taken and $r$ is the location vector. When a dielectric is placed in an electric field, there would be a slight displacement of the electron cloud with respect to the nucleus in each atom, generating a tiny electric dipole. Assuming uniform distribution of dipoles in the bulk, it can be noted that the surface charge density is equal to the polarization in magnitude.

The electric displacement $D$ is related to the polarization through the linear expression:

$$D = \varepsilon_0 E + P$$

[Eq. 2.26]

where the derived constant $\varepsilon_0$, the permittivity of free space, is $8.854 \times 10^{-12}$ C/Vm. By applying this equation to a capacitor with unit area and thickness, $E$ corresponds to the voltage across the capacitor and $D$ is the total stored charge on the capacitor. Eq. 2.26 then states that the total charge on the capacitor is due to the superposition of two sources of charge: $\varepsilon_0 E$, which is the charge in the absence of dielectric, and $P$ which is the extra charge introduced by a dielectric between the electrodes. For linear dielectrics, $P$ is proportional to $E$, and Eq. 2.26 can thus be simplified and shown as:

$$D \equiv \varepsilon E$$

[Eq. 2.27]

where $\varepsilon$ is the dielectric permittivity and can be interpreted as the capacitance of the unit-area, unit-thickness capacitor with dielectric.

In ferroelectric materials, $P$ is not only a function of $E$ but also depends on the previous history of the material. This means that the instantaneous voltage across a ferroelectric capacitor does not provide enough information to determine the capacitor charge. Therefore, it is not possible to express $D$ as a closed form function of $E$. 
However, as the polarization in ferroelectric materials is at least two or three orders of magnitude larger than $\varepsilon_0 E$, Eq. 2.26 can be approximated by:

$$D \cong P$$  \hspace{1cm} [Eq. 2.28]

This equation implies that the magnitude of the total surface charge density on a capacitor with ferroelectric material is equal to that of the polarization. The polarization can be separated into the two fundamental components of electronic polarization and ionic polarization. The terms of electronic and ionic polarizations refer to the electronic cloud and ionic displacements with electric field, respectively. Ionic displacement, in turn, can be elastic or inelastic. If the electric field is removed from the material, the electron clouds and ions that are displaced only slightly with respect to their original position. However, those ions that are displaced through an inelastic mechanism (central ions such as Ti$^{4+}$ or Zr$^{4+}$ for PZT in Fig. 2.10), keep their new positions, even after the removal of the electric field. These ions are responsible the polarization in ferroelectrics as compared to ordinary dielectrics.

In ferroelectric materials, spontaneous polarization can occur where the electrical polarization can be reoriented between its different equilibrium orientations by applying an electric field. This gives rise to a dielectric hysteresis loop between applied electric field and the polarization charge as is illustrated in Fig. 2.13 together with some of the important parameters. In this figure, the $x$- and $y$- axes are the polarization $P$ and the electric field $E$, respectively. $P$ can be replaced by $D$ if one assumes $\varepsilon_0 E \ll P$, which is the case for ferroelectric materials and it can be considered as the plot of $D$ versus $E$. Moreover, as the electric displacement and the electric field are proportional to the total capacitor charge and the voltage across the capacitor, respectively, the same loop is also a scaled version of total charge $Q$ versus voltage $V$. As the voltage across the ferroelectric capacitor increases, corresponding to the lower branch of the hysteresis loop, the net polarization also increases. At the beginning ($E=0$), the major contribution is from electronic and elastic polarization. Afterwards, as the voltage increases, the number of switching domains increases inside the material and the inelastic polarization forms the major part of the total polarization. This part does not return to its original value as the
voltage across the capacitor starts decreasing. Therefore, the total polarization does not follow the same branch of the hysteresis loop when decreasing the field to zero. Similar description applies to the left side of the hysteresis loop if the properties of the ferroelectric material are assumed to be symmetrical.

The hysteresis loop only provides steady state information about the ferroelectric material. The hysteresis loop will change distinctly if the period of the voltage waveform approaches the time that is necessary for the switching of most of the domains in the material. Hysteresis loop is not only a characteristic of the ferroelectric material alone but also a characteristic of the electrode material and the applied waveform. The saturation polarization $P_{\text{sat}}$, the remanent polarization $P_r$, and the coercive Field $E_c$ are the three different parameters of the hysteresis loop. These parameters are normally used to compare different ferroelectric materials. As larger electric fields are applied to a ferroelectric material, domains favorably oriented with respect to the field direction grow at the expense of other domains. This process continues with increasing electric field until the least favorably oriented domains switch to the polar direction most closely coinciding with the electric field direction. When no further domain reorientation can occur, the $P$ versus $E$ response usually becomes linear. If the linear response is extrapolated to the polarization axis ($E=0$), the polarization value at the intersection is designated as the saturation polarization, $P_{\text{sat}}$, as shown in Fig. 2.13.

The magnitude of polarization at $E=0$ is called remanent polarization and it is shown by $P_r$, in Fig. 2.13. If no domains change direction while removing the electric field, $P_r$ and $P_{\text{sat}}$ would be the same. However, mechanical boundary conditions normally impose direction changes in some domains, causing $P_r$ to be less than $P_{\text{sat}}$. The coercive field, $E_c$, is defined as the horizontal intercept of the hysteresis loop or the field at which the net polarization becomes zero. In a single domain crystal, $E_c$ can be interpreted as the field at which the polarization switches from one state to another. In a multi-domain crystal, however, $E_c$ will lose its interpretation, as there is no single field at which all domains can switch. As shown in Eq. 2.27, permittivity is defined as the ratio of electric displacement to electric field in linear dielectrics. In ferroelectric materials, which are nonlinear, two types of permittivity can be defined, namely small-signal and differential permittivity. The former, denoted as $\varepsilon$, is defined as the incremental change in electric displacement per unit electric field when the magnitude of the measuring field is very small compared to the coercive electric field. Macroscopically, $\varepsilon$ is found by measuring the capacitance. The units of permittivity are C/Vm. The measuring field or voltage must be kept small to prevent ferroelectric domain reorientation from contributing to this type of permittivity. In other words, only electronic and nonswitching polarizations should contribute to small signal permittivity. Differential permittivity is defined as the slope of the hysteresis loop (electrical displacement versus electric field) at any point. Note that the differential permittivity is partly affected by the inelastic polarization and therefore, is different from the small signal permittivity.

2.3.4 Applications of Ferroelectrics

Among the applications of ferroelectric thin films, the greatest emphasis has been on nonvolatile random-access memories (NVFRAM). Two main concepts, i.e. destructive read out (DRO) and nondestructive readout (NDRO), are being explored for NVFRAM
designs. In this work, the non-volatile memory effect has been demonstrated in metal-ferroelectric-insulator-semiconductor (MFIS) structures (Paper VI, VII) and field effect transistors in SiC at elevated temperatures (Paper VIII). The general applications are described in this section below.

Currently, the first generation of NVFRAM is based on DRO schemes and a ferroelectric memory cell is normally composed of one transistor and one capacitor in this scheme. As shown in Fig. 2.14, it is similar to a DRAM cell, except that the DRAM capacitor is replaced by a ferroelectric capacitor[63-65]. It can be fabricated in megabit and gigabit capacities through current using state-of-the-art circuit technology. An alternative architecture involves two capacitors per bit, one of which is a reference capacitor. This is more reliable for read-out, but takes up more space. The polarization state can be read when a positive switching voltage is applied to the memory cell. If the cell polarization is already ‘+’ (logic state 1), then only a linear non-switching response is measured in the form of a voltage across a 10–50-ohm resistor. If the cell is ‘-’ (logic state 0), a switching response greater than the linear response is measured because it contains the additional displacement current term \( \frac{dP}{dt} \), where \( P \) is the polarization. A sense amplifier then compares this response with that of a reference cell, which is always polarized to ‘-’. Thus, in destructive read-out (DRO) scheme, the read operation is based on monitoring currents caused by polarization changes when a voltage is applied, which causes the memory to be erased and require rewriting.

![Fig. 2.14 1T-1C Cell and Lateral, low density architecture of DRO NVFRAM](image)
In NDRO approach, which prevents re-polarization of the ferroelectric after a read operation, a ferroelectric thin film is deposited over the gate of a field-effect transistor (FET) as is illustrated in Fig. 2.15. In this structure, the polarization state of the ferroelectric layer controls the source-to-drain current through the FET. The fast write time and the capability of high-density integration are also great advantages as well as nondestructive readout. Moreover, the device size in this one-transistor (1T) memory can be reduced in accordance with the scaling rule, which cannot be realized by traditional capacitor-type or one-transistor and one-capacitor (1T1C)-type memory.

However, unstable and excessive charge injection from the ferroelectric/semiconductor interface (between lead-based ferroelectrics and Si or GaAs semiconductor substrates) has been an obstacle to fabricate Metal-Ferroelectric-Semiconductor (MFS) devices on Si and GaAs wafers so far. The first demonstration of ferroelectric PZT-gated field effect transistors in SiC is included in the appended Paper VIII.

There is also extensive research performed to integrate ferroelectric materials into DRAM capacitors. Ferroelectric materials have a high permittivity $\varepsilon$, which can be exploited to store information as charge. High permittivity DRAMs work in the same way as conventional DRAMs. The polarization of a high-$\varepsilon$ layer depends linearly on the applied voltage, as required for charging the DRAM capacitors. Therefore high-$\varepsilon$ materials do not exhibit polarization-voltage hysteresis loops and have a high breakdown field and a great resistance to charge injection. Generally, the capacitance of DRAM capacitors $C$ is given by $\varepsilon A Q / t$, where $A$ is the area of the parallel capacitor, $Q$ is the total charge and $t$ is the thickness of the layer. In order to increase $C$, the conventional route has been to increase $A$, which results in a convoluted geometry, which is difficult to fabricate for gigabit DRAMs. An alternative way to increase $C$ is to use materials with higher permittivities, which is the case for ferroelectric DRAMs. For example, barium strontium titanate, $\text{Ba}_{x}\text{Sr}_{1-x}\text{TiO}_3$ (BST), has a relative permittivity $\varepsilon / \varepsilon_o$ of 300–400, compared with 3.9 for $\text{SiO}_2$. Because of the high permittivity, a BST capacitor could be 100 times smaller than one made from $\text{SiO}_2$.

Ferroelectric materials, especially thin films, can be employed in the manufacture of wide range of other devices that exploit their special properties. Ferroelectric materials also manifest piezoelectricity, which can be made use of in the manufacture of micro-machines, such as accelerometers, displacement transducers and actuators of various kinds including those required for inkjet printers, VCR head positioning and micro-

![Fig. 2.15 Schematic diagram of NDRO NVFRAM architecture](image-url)
machining. Pyroelectricity of ferroelectric materials can be used as the basis for highly sensitive infrared room temperature detectors. The pyroelectric effect are seen as the form of a voltage (potential difference) between the opposite faces of a ferroelectric layer when heat (a temperature change) causes positive and negative ions to drift to opposite faces of the crystal. Ferroelectric materials also exhibit electro-optic effect. Their refractive indices change when a voltage is applied across them. This effect can be used in color filter devices, computer displays, image storage systems and optical switches for integrated optical systems.

Ferroelectric materials have a variety of useful properties that can be exploited in thin film devices and some specific terms for the different reliability aspects of ferroelectric elements are described below.

**Fatigue** limits the write endurance by causing a reduction of signal during the repeated switching of polarization:

- **Fatigue**: the gradual decay of the polarization with repeated switching of the material. Particularly, a ferroelectric DRO memory is prone to fatigue since polarization switching may occur during each read operation. A minimum polarization of 100 fC/m² is necessary in a normal DRAM application to avoid errors. The level of available polarization in PZT is known to move below this limit after $10^{12}$ cycles.

Ferroelectric memories also suffer from **retention** failure caused by polarization **aging** and **imprint**:

- **Retention**: the ability of memory to retain its state, to be able to read-out the stored information at a certain time without external power source.

- **Imprint**: the tendency of a ferroelectric capacitor to prefer one state to another if it stays for a long period of time in that state. Imprint causes the polarization to gradually return to a different, previously written orientation (e.g. an increase of the signal from a "0" state).

- **Aging**: a degradation of polarization parameters with time. Aging causes the polarization to freeze in one direction so that it does not respond to read operation. In the literature a power-law decay or a logarithmic decay of aging have been reported.

As in normal dielectric, **relaxation** and **breakdown** are to be considered in ferroelectrics:

- **Relaxation Phenomenon**: a reduction of the remanent polarization in a short time regime (typically microseconds or less), if the capacitor is left unaccessed following a sequence of continuous cycling.

- **Time Dependent Dielectric Breakdown**: the thin film dielectric breakdown of a ferroelectric capacitor if the voltage stress is applied for a sufficient period of time and a device is considered failed if the leakage current exceeds a certain limit.
CHAPTER 3

Process Integration

The chapter describes general processes for fabricating SiC devices. Processes such as material growth, doping, cleaning, etching, metallization, oxidation, laser-deposition are included.

3.1 General Aspects

Most of the key SiC process technologies including doping, dry etching, oxide growth, Schottky and Ohmic contacts, are relatively mature. In addition SiC process technology is similar or compatible to that of conventional Si and GaAs.

However, there are a few differences:

(i) There are no wet etching methods for SiC at room temperature. Hence plasma etching is the most practical technique in etching SiC.
(ii) Higher temperatures are required to activate implanted dopants in SiC than those in conventional semiconductors.
(iii) The oxidation rate in SiC is very low and therefore relatively higher temperatures are needed.
(iv) Contact anneals need higher temperature as well.

The high temperature during the process can be a major difficulty in SiC process. The small size of SiC wafers necessitates extra consideration to handle the wafers with equipments. Moreover, some material quality issues are critical to overcome for device commercialization.

3.2 Bulk, Epitaxial Growth and Doping

The seeded sublimation technique, where the crystal is grown from a solid source, has proven successful in SiC since its initial development by Tairov and Tsvetkov in 1978[69]. A high quality SiC seed crystal is used in this method, which still is basically the favored method with modifications for substrate fabrication. SiC bulk growth is under continuous improvement in terms of micro-pipe defects, background doping and mechanical stress. Nowadays 50 and 75 mm wafers are commercially available and 100 mm wafers have been reported[11]. Companies such as CREE Research[12], Okmetic[70],
and Sterling Inc.[71], which currently is a part of Dow Corning, are producing SiC wafers, and semi-insulating substrates are available in addition to n- and p-type wafers. The semi-insulating wafers are more expensive at present. For device applications, generally a buffer layer is needed on semi-insulating wafers below the channel to avoid traps.

The chemical vapor deposition (CVD) technique is usually used to grow epitaxial layers in SiC. In CVD, silicon- and carbon- containing gases are transported from precursors to the sample with hydrogen as carrier gas. High temperature chemical vapour deposition (HTCVD) can be used as an alternative to standard CVD for thick epitaxial layers. High quality layers of several mm-thickness have been reported by using HTCVD. Liquid phase epitaxy (LPE) is another commonly used method that shows relatively stable polytypes[24].

The color of the material depends on the doping and polytype in SiC: for example, p-type materials (>10^18) show dark-blue color whereas n-type (>10^18) is brown (4H), green (6H) or yellow (15R) depending on polytypes. Low-doped or semi-insulating materials are transparent. Normally one or more epitaxial layers are needed for the device processing, since the substrate (wafer) has too high doping. Ion implantation can be used to selectively define the highly doped regions[24, 72]. The wafer needs to be heated up to 500 – 700 °C during the ion implantation in order to reduce the damage and therefore silicon dioxide or metal masks are used instead of photo resist. Even higher temperature is required to anneal the crystal damage after implantation, around 1200 °C for n-type and up to 1700 °C for p-type. No implantation step has been applied in this work.

The starting wafers for the experiments in the thesis were 6H- and 4H-SiC with Si-face orientation (0001). The initial wafers with 1 ½ inch or 2 inch in diameter were purchased from a commercial vendor (CREE Research Inc.[12]). Standard highly doped substrates (∼10^18 cm^-3) were used with lowly doped epitaxial layers (10^15–10^17 cm^-3) for buffer or channel region whereas highly doped epitaxial layers (10^19–10^20 cm^-3) were employed to form Ohmic contacts. Epitaxial layers were grown at Linköping University or Acreo AB. Nitrogen and aluminum are used for n- and p-type dopants respectively.

### 3.3 Surface Cleaning

It is of great importance to prepare and to clean the wafers. Normally, the cleaning may include plasma cleaning, UV-cleaning and chemical cleaning and each of them can be a broad topic. Most of chemical cleaning recipes for SiC are from Si. In this work, in order to remove possible contamination during polishing and transport, a conventional sacrificial oxidation was performed for the newly purchased wafers. Then, each wafer was normally divided into several smaller samples, as the wafers are extraordinarily expensive compared to for example Si. Before each processing, whenever required, the samples were directly degreased in acetone, isopropanol, and de-ionized (DI) water for 2 min each. This is to get rid of resists or any grease that may be present on the sample surface. The acetone removes unhardened resist and grease while isopropanol is mainly used for degreasing and dissolving acetone. Methanol can be used to remove residues of acetone and isopropanol effectively. Some standard chemical cleaning is listed in Table 3.1[37, 73, 74].
Table 3.1 Chemicals used for cleaning of SiC wafers and removing SiO₂.

<table>
<thead>
<tr>
<th>Chemicals</th>
<th>Temp. / Time</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H₂O:NH₄OH:H₂O₂ (5:1:1)</td>
<td>75°C/5min</td>
<td>RCA SC1</td>
</tr>
<tr>
<td>H₂O:HCl:H₂O₂ (5:1:1)</td>
<td>75°C/5min</td>
<td>RCA SC2</td>
</tr>
<tr>
<td>H₂SO₄:H₂O₂ (2.5:1)</td>
<td>100°C/5min</td>
<td>Seven-up</td>
</tr>
<tr>
<td>H₂O:HF:CH₃(CH₂OH)CH₃(100:1:1)</td>
<td>25°C/100s</td>
<td>IMEC</td>
</tr>
<tr>
<td>HCl:HNO₃ (3:1)</td>
<td>50°C/5min</td>
<td>Aqua regia</td>
</tr>
<tr>
<td>HF:H₂O(1:10)</td>
<td>25°C</td>
<td>Dilute HF</td>
</tr>
<tr>
<td>HF:NH₄F (1:7)</td>
<td>25°C</td>
<td>BHF</td>
</tr>
<tr>
<td>BHF+NH₄OH</td>
<td>25°C</td>
<td>pH-modified BHF (pH 12)</td>
</tr>
</tbody>
</table>

Two different chemical cleaning recipes, so called "Seven-up" and "IMEC", were used prior to the oxidation and metal deposition. Seven-up is very useful to remove hardened resist as well as most metals. RCA SC1 and SC2 is to remove any organic and metallic contaminations, respectively. Oxygen plasma cleaning is another way to remove hardened resist.

3.4 Etching

It is not a straightforward task to etch SiC because of its hardness (H=9⁺) and chemical inertness. In fact, SiC is one of the most widely used lapping and polishing abrasives for metals, metallic components and semiconductor wafers.

Table 3.2 Etchants for selected metals.

<table>
<thead>
<tr>
<th>Material</th>
<th>Etchant</th>
<th>Etch rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>H₃PO₄:CH₃COOH:HNO₃:H₂O (4:4:1:1)</td>
<td>350 Å/min at 35°C</td>
</tr>
<tr>
<td>Au</td>
<td>KI:I₂:H₂O (4g:1g:40ml)</td>
<td>3500 Å/min</td>
</tr>
<tr>
<td>Mo</td>
<td>H₃PO₄:CH₃COOH:HNO₃:H₂O (5:4:2:150)</td>
<td>5000 Å/min</td>
</tr>
<tr>
<td>Ni</td>
<td>HCl:HNO₃:H₂O (4:1:5)</td>
<td>1500 Å/min (at 65°C)</td>
</tr>
<tr>
<td></td>
<td>H₃PO₄:CH₃COOH:HNO₃:H₂O (4:4:1:1)</td>
<td>500 Å/min at 35–40°C</td>
</tr>
<tr>
<td>Pd</td>
<td>HCl:HNO₃:CH₃COOH(1:10:10)</td>
<td>1000Å/min</td>
</tr>
<tr>
<td>Pt</td>
<td>HNO₃:HCl:H₂O (1:7:8)</td>
<td>400–500Å/min at 85°C</td>
</tr>
<tr>
<td>Ti</td>
<td>HF(5%):H₂O(1:2)</td>
<td>5000 Å/min</td>
</tr>
<tr>
<td>TiW</td>
<td>NH₃:H₂O(2:1:5)</td>
<td>600 – 4000 Å/min</td>
</tr>
<tr>
<td></td>
<td>H₂O₂</td>
<td>45 Å/min</td>
</tr>
</tbody>
</table>
Table 3.3 Wet-etch solutions and etching temperatures for SiC.

<table>
<thead>
<tr>
<th>Solution</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>NaOH</td>
<td>900 °C</td>
</tr>
<tr>
<td>Na₂O₂</td>
<td>&gt;400 °C</td>
</tr>
<tr>
<td>NaOH/Na₂O₂</td>
<td>700 °C</td>
</tr>
<tr>
<td>NaOH/KOH</td>
<td>480 °C</td>
</tr>
<tr>
<td>Na₂O₂/NaNO₂</td>
<td>&gt;400 °C</td>
</tr>
<tr>
<td>KOH/KNO₃</td>
<td>350 °C</td>
</tr>
</tbody>
</table>

The only few possible techniques to etch SiC includes molten salt fluxes, hot gases, electrochemical processes[75, 76] or plasma etching (see table 3.3)[24, 77-79]. Nevertheless, both metals and dielectric materials can be wet-etched and thus wet-etching is employed normally for the SiC device processes. Table 3.2 summarizes several etchants for metals[43, 80].

Whereas the large Si-C bonding energy makes silicon carbide attractive for applications in harsh environments, it becomes problematic in case of etching SiC. As seen in table 3.3, conventional wet chemical etching is not possible at practical process temperatures and no practical mask material can endure those conditions either. Hence plasma-based dry etching plays a crucial role in SiC for the device pattern transfer process. Plasma etching is used for junction termination in mesa structures, devices with various structures such as BJTs and buried-gate JFETs, U-MOSFETs, or via-hole etching in SiC. Fluorine-based plasma etching of SiC has proven to be successful. Recently, inductively coupled plasma reactive ion etching (ICP-RIE) in a SF₆/O₂ plasma have yielded etch rates up to 970 nm/min and a helicon reactor produced etch rates as high as 1.35 µm/min [81, 82](see table 3.4). Reactive ion etching (RIE) plays a important role particularly on the gate recess and device isolation etching. The main problem caused by the RIE technique is the creation of ion-induced damages on the etched surface, due to the high dc self-bias required to reach an acceptable etch rate.

The inductively coupled plasma (ICP) source has significant advantages over RIE, such as lower ion energies, lower process pressure leading to the anisotropic etching, and higher plasma densities (>10¹¹ cm⁻³). In ICP, plasmas are formed in a dielectric vessel encircled by an inductive coil into which rf power is applied. In Fig 3.1, the schematics of RIE and ICP reactors are described.

Anisotropic profiles are obtained by superimposing a rf-bias on the sample to independently control ion energy and by using flow pressure conditions to minimize ion scattering and lateral etching. In the chamber a strong magnetic field is induced, which then generates a high-density plasma (5x10¹¹ cm⁻³). The electrons in this circular path will have a very low probability to be lost to the chamber walls, causing a low dc self-bias. At low pressures (≤20 mTorr), the plasma diffuses from the generation region and drifts to the substrate with relatively low ion energy (<25 eV). Accordingly ICP etching results in higher etch rates (>7500 Å min⁻¹) for SiC with reduced damage on the etched
surface. However, the electrical properties were degraded even with the lower damage of the ICP technique, depending on the processing condition.

In this work, an ICP reactor was used to etch SiC using a fluorine-based chemistry (SF$_6$/Ar/O$_2$). The general process recipe for a typical condition is a mixture of SF$_6$ (21 sccm) and Ar (9 sccm) at 600 W of rf forward power and 5.0 mTorr base pressure with an Al mask. The etch rate was around 0.12 µm/min with 30W of platen power.

![Schematic cross-sections of (a) RIE and (b) ICP reactors](image)

**Table 3.4** Summary of reported dry etch rates of SiC

<table>
<thead>
<tr>
<th>Reactor</th>
<th>Gas</th>
<th>SiC Polytype</th>
<th>Etch Rate [Å/min]</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>RIE</td>
<td>SF$_6$/O$_2$</td>
<td>6H</td>
<td>410</td>
<td>[83]</td>
</tr>
<tr>
<td></td>
<td>CF$_4$/O$_2$</td>
<td>6H</td>
<td>278</td>
<td>[83]</td>
</tr>
<tr>
<td></td>
<td>NF$_3$/O$_2$</td>
<td>6H</td>
<td>493</td>
<td>[83]</td>
</tr>
<tr>
<td></td>
<td>SF$_6$</td>
<td>3C</td>
<td>700</td>
<td>[84]</td>
</tr>
<tr>
<td></td>
<td>NF$_3$</td>
<td>6H, 4H</td>
<td>1500</td>
<td>[85]</td>
</tr>
<tr>
<td>ICP</td>
<td>NF$_3$/O$_2$ or Ar</td>
<td>6H</td>
<td>4000</td>
<td>[86]</td>
</tr>
<tr>
<td></td>
<td>NH$_3$</td>
<td>4H</td>
<td>8000</td>
<td>[87]</td>
</tr>
<tr>
<td></td>
<td>SF$_6$</td>
<td>6H</td>
<td>9700</td>
<td>[81]</td>
</tr>
<tr>
<td>Helicon</td>
<td>30SF$_6$/7/5 O$_2$</td>
<td>4H</td>
<td>13.500</td>
<td>[82]</td>
</tr>
</tbody>
</table>
Fig. 3.2 Scanning electron microscopy (SEM) image of (a, b) the trenching effect on the bottom of the sidewall and (c, d) trenching corner after using angled oxide mask which was wet-etched by using BHF.

The electrical properties of Ohmic contacts and MOS structures on etch damaged surfaces are of interest and in Paper II, it is shown that medium platen power (60W) ICP etching showed significant influence on the Ohmic contact formation whereas low power (30W) ICP etching process did not affect the properties of the subsequently formed Ohmic contacts. It is demonstrated that some damage from a low-energy etched 4H-SiC can be recovered by a sacrificial oxidation.

In Fig. 3.2, scanning electron microscopy (SEM) images of the channel region of the JFETs are shows the trenching effect on the bottom of the sidewall with Ni mask (a,b) and trench corner rounding using an angled oxide mask (c, d). The inset in (c) shows a schematic diagram of oxide mask and SiC. The trenching effect, known to occur in most dry etching conditions for SiC, is due to the deflection of ions on the sidewall inducing enhanced ion bombardment at the bottom. With an etch-depth of 4µm, a trenching profile of 0.2 µm has been observed in the channel groove region of a junction field-effect transistor (JFET) fabricated with Ni metal mask as discussed in Paper III (see Fig. 3.2). It is shown that the trenching effect may result in a local short channel effect in SiC buried-gate JFETs, while a sloped etch wall without trenching effect can be realized by using SiO₂ mask with wet-etched slope to transfer a slope during dry etching of SiC.
### 3.5 Metallization

All devices need good Ohmic contacts. They are particularly important for applications using high current densities that result in large voltage drops even across a small resistance. On the other hand, some devices for instance the MESFET and the Schottky diode should have Schottky contacts in the structure. The specific contact resistance to \(n\)- and \(p\)-type SiC is normally in the range of \(10^{-4}\)~\(10^{-6}\) \(\Omega\)cm\(^2\) and \(10^{-3}\)~\(10^{-5}\) \(\Omega\)cm\(^2\), respectively, and are highly dependent on the surface doping concentration, choice of the metal, sample preparation, and the post metallization heat treatment. Ohmic contacts to \(n\)-type SiC seem to be acceptable for device applications. However, due to the higher barrier height, it is yet more difficult to obtain lower specific contact resistance (\(\rho_c\)) for \(p\)-type SiC. Table 3.5 shows the properties of various Ohmic contacts to \(n\)- and \(p\)-type SiC reported to date. SEM images of nickel (Ni) and titanium tungsten (TiW) contacts after annealing at 950 °C are shown in Fig. 3.3.

<table>
<thead>
<tr>
<th>Type</th>
<th>Metal</th>
<th>Doping (cm(^{-3}))</th>
<th>(\rho_c) ((\Omega)cm(^2))</th>
<th>Condition</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(n)</td>
<td>Ni-Cr</td>
<td>4.8\times10^{17}</td>
<td>1.0\times10^{-4}~1.6\times10^{-5}</td>
<td>1100°C, 3 min</td>
<td>[88]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.3\times10^{19}</td>
<td>1.2\times10^{-5}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ni,Cr,W</td>
<td>10^{17}~10^{18}</td>
<td>10^{-4}~10^{-6}</td>
<td>1000~1050°C, 5 min</td>
<td>[89]</td>
</tr>
<tr>
<td></td>
<td>TiC</td>
<td>1.3\times10^{19}</td>
<td>4\times10^{-5}</td>
<td>950°C</td>
<td>[90]</td>
</tr>
<tr>
<td>(p)</td>
<td>Si/Pt</td>
<td>1\times10^{19}</td>
<td>\sim10^{-3}</td>
<td>30~400°C, 3 min</td>
<td>[91]</td>
</tr>
<tr>
<td></td>
<td>Al/Ti</td>
<td>&gt;10^{20}</td>
<td>\sim10^{-3}~10^{-4}</td>
<td>1100°C</td>
<td>[91]</td>
</tr>
<tr>
<td></td>
<td>TiC</td>
<td>&gt;10^{20}</td>
<td>6\times10^{-5}</td>
<td>950°C, 850°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ti</td>
<td>&gt;10^{20}</td>
<td>8\times10^{-4}</td>
<td>950°C</td>
<td>[93]</td>
</tr>
<tr>
<td></td>
<td>TiW</td>
<td>1.3\times10^{19}</td>
<td>1.2\times10^{-4}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ti/Al</td>
<td>3\times10^{20}</td>
<td>10^{-6}</td>
<td>1000°C, 2min</td>
<td>[94]</td>
</tr>
</tbody>
</table>

**Table 3.5** Reported values of Ohmic contacts to 4H-SiC

**Fig. 3.3** SEM images of (a) Ni and (b) TiW contacts after high-temperature annealing.
Generally, Ni-based and Al-based contacts have been widely used for \textit{n}-type and \textit{p}-type SiC, respectively. The low melting temperature of aluminum and the formation of aluminum oxide make it difficult to apply Al for high power and high temperature device applications. The lowest contact resistivities yet reported for \textit{p}-type SiC is in the $5 \times 10^{-6}$ $\Omega\text{cm}^2$ range using CoSi$_2$ by sequential evaporation of Co and Si on 6H-SiC\cite{95}. In order to form an Ohmic contact, a high doping level ($>10^{19}$ cm$^{-3}$) is required. Having a highly doped region of SiC is necessary to achieve Ohmic contact but it is not sufficient. Usually a high temperature annealing ($>900$ °C) is required after the metallization since a reaction between the metal and the SiC is often needed for a good Ohmic contact. This reaction can be promoted for a damaged surface and also the choice of the metal is very important since the reaction products are to be considered. Generally the reaction between the metal and the SiC causes roughening of the metal film, which makes wire bonding difficult and can cause reliability problems. In this work, Ohmic contacts were annealed at 900–980 °C in Ar or in 10% H$_2$/Ar using rapid thermal annealing (RTA). The characterization of electrical contacts is described in more detail in Chapter 4.

Deposition by electron beam (e-beam evaporation) and sputter deposition (sputtering) has been used for the metal contact process. The main difference between these two methods is the step coverage: e-beam has negligible step coverage whereas sputtering produces films with good step coverage as shown in Fig 3.4. Thus e-beam is used for lift-off process and sputtering is employed in case better step coverage or a higher deposition rate is needed. Normally pure metals including Au, Pt, Ti, Ni, and Al are deposited by e-beam evaporation and alloys such as TiW are sputtered by a DC magnetron sputtering system.

In e-beam evaporation, a focused electron beam is used to heat a metal target to evaporate. Then the evaporated metal radiates out from the target of which some portion is deposited on the surface of the mounted sample. Generally the target is placed on the bottom side of the chamber while the samples are on the ceiling side as shown in Fig. 3.5 (a)[96, 97].

Sputtering can be used to deposit refractory materials, compound and alloys, which are difficult to evaporate. Sputtering is a physical vapor deposition (PVD) process involving the removal of material from a solid cathode. This is done by bombarding the cathode with positive ions emitted from a rare gas discharge. When ions with high kinetic energy are incident on the cathode, the subsequent collisions knock loose, or sputter, atoms from the material. A typical sputter system is shown in Fig. 3.5 (b).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig3_4.png}
\caption{Fig. 3.4 Simplified schematics showing step coverage: (a) poor step coverage with e-beam deposition, and (b) good step coverage with sputter deposition.}
\end{figure}
In this work, contacts such as Ni, Au, Pt and Ti were metallized by using e-beam evaporation under a base pressure of $2 \times 10^{-7}$ Torr and a deposition pressure of $3-6 \times 10^{-6}$ Torr (see Fig. 3.3(a) for an example of Ni-contacts to SiC). A DC magnetron sputter was used for TiW (weight ratio of 30:70) deposition with 50-69 sccm of Ar gas flow, $5 \times 10^{-7}$ Torr base pressure, and $5 \times 10^{-3}$ Torr during the deposition (see Fig. 3.3(b)). The addition of Ti below Pt provides improved adhesion and contact resistance properties. The deposition rate of the TiW metal, the thickness, and the metal resistivity were 500-600 Å/min, 1500-2500 Å, and 85–88 $\mu\Omega$cm, respectively. The sputtered TiW can simply be wet-etched using a mixture of 25% NH$_3$:H$_2$O$_2$(1:5) with an etch rate of 600-4000 Å/min depending on the sample preparation.

Since chemical reactions take place between the metal and the SiC, a chemical analysis of the resulting alloy is of interest[96, 97]. Apart from XRD and RBS, scanning electron microscopy (SEM) can be used to look at the surface of the metal, and cross sections through the metal/SiC interface can be investigated with SEM or transmission electron microscopy (TEM). Atomic force microscopy (AFM) can be used to measure the roughness of the metal surface after annealing (see Fig. 4.4 in chapter 4).
3.6 Oxidation and Dielectrics

SiC is one of the few compound semiconductors that can be thermally oxidized to form SiO$_2$, which is crucial for both fabricating devices with MOS structures and passivation of surfaces. Although the detailed properties of the oxide and its interface are far different from those in Si, thermal oxides can be formed with the same oxidation equipment and techniques as for Si. SiC is normally oxidized at higher temperatures (>1150°C) and at slower rate, due to the stronger Si-C bonds compared to Si-Si bonds (see Fig. 3.6). Details of the oxidation mechanism are not clarified yet and there are some proposed reactions at the interface between the silicon atom in the SiC lattice and the oxygen molecule (SiC+1.5O$_2$ → SiO$_2$+CO or SiC+O$_2$ → SiO$_2$+C)[24]. During thermal oxidation of SiC, Si atoms at the interface are oxidized to form SiO$_2$ with oxygen diffusing through the already formed oxide and C atoms to form CO, which might diffuse out through the oxide. But there is some evidence that carbon forms clusters at the SiO$_2$-SiC interface, which possibly affect the electrical properties of the interface.

One way of reducing the problem of excess carbon is to avoid consumption of the SiC by depositing the oxide. The interface properties of SiO$_2$/SiC have been improved by H$_2$ treatment prior to the oxidation or by post-oxidation annealing in NO or N$_2$O[24].

A serious problem with oxidation of SiC is the low MOS channel mobility. The best values reported for the $n$-channel inversion mobility in 6H-SiC is 70-100 cm$^2$/Vs whereas values of 1-20 cm$^2$/Vs are commonly found for the inversion channel mobility in 4H-SiC[98, 99]. Although the 4H polytypes have higher and more isotropic bulk carrier mobilities than the 6H polytypes, channel mobility in $n$-channel inversion mode MOSFETs is noticeably lower for 4H–SiC compared to 6H SiC. The low mobility is directly related to interface defects that either trap or scatter carriers, due to the result of a relatively high SiO$_2$/SiC interface state density of $10^{13}$ cm$^{-2}$ compared to $10^{10}$ cm$^{-2}$ for Si.

![Fig. 3.6 Dry oxidation of the Si and C faces in 6H-SiC in comparison with Si at 1200 °C. After Zetterling[24, 32].](image-url)
Such inferior performance of 4H-SiC devices is ascribed to the presence of a large and broad interface state density located at around 2.9 eV above the valence band edge in both 4H- and 6H-SiC[100]. The majority of these states lie in the conduction band for 6H–SiC ($E_g \sim 3eV$) and hence hardly affect the inversion channel mobility. On the other hand, for 4H–SiC ($E_g \sim 3.3eV$), the interface states lie mostly in the band gap where they act to reduce channel mobility by field termination, carrier trapping, and Coulomb scattering. The low values of the inversion mobility in 4H-SiC or the low bulk mobility along the $c$-axis in 6H-SiC can be improved by using oxides on 15R-SiC for (0001) Si face or on different faces such as (1120) ($a$-plane) or (0338) [100-102]. Investigations on alternative dielectrics on SiC such as Si$_3$N$_4$ or AlN have been reported but only limited information is presently available[103]. The main problem with AlN is to achieve impurity free, non-conducting films. For high power devices, it is important to terminate the region at which high field crowding and breakdown occurs. Most passivation techniques in Si devices are also applicable to SiC, which includes guard rings, field plate termination, and junction termination extensions (JTE)[104-106]. Other techniques are to implant a high dose of inert ions (either Ar[107] or B[108]) forming a high resistivity region or to create a beveled surface region by etching. Power switching devices appear to perform well with these passivation treatments even though the inadequate passivation affects the sub-threshold or the microwave characteristics of JFETs and MESFETs.

During the thermal oxidation, some part of SiC surface is consumed and then the silicon dioxide can be removed by wet etching with HF. This is the so-called sacrificial oxidation (SO). In this work, the thermal oxidation process has been used to form the MOS gate for depletion-mode control in FETs (Paper V), as well as the passivation or isolation oxides (Papers II, IV, VII, and VIII). The effect of sacrificial oxidation has been studied in terms of the electrical properties of oxides (Paper I) and Ohmic contacts (Paper II) on dry-etch damaged SiC.

### 3.7 Pulsed Laser Deposition of Ferroelectrics

One of the main achievements in this thesis has been on the feasibility of implementing ferroelectrics onto SiC. Pulsed laser deposition (PLD) is a necessary technique for ferroelectric thin film formation. With respect to other processes such as chemical-vapor deposition and sol-gel, PLD allows for easy handling, since the laser source is placed outside the reaction chamber. It was not until 1987 when T. Venkatesan et al.[109] successfully prepared in-situ YBa$_2$Cu$_3$O$_{7-x}$ high $T_c$ superconducting thin films using PLD, that the technique received extensive experimental development[110]. The discovery, that high $T_c$ superconducting films can be grown in a low-pressure oxygen ambient environment by PLD without any further processing, opened the field of oxide ceramic film growth and research on PLD. In PLD, it is easier to grow the films with a good stoichiometric transfer of the target composition. In addition PLD provides the convenience of oxygenating films in situ by reactive deposition in relatively high oxygen pressures. PLD is also a flexible method to deposit multi-layers and has simple operation procedures. The PLD method is based on physical processes, arising from the impact of high-power pulsed laser radiation on solid targets and leading to the removal of partially ionized material (plasma or plume) from the impact zone[58, 111].
A typical PLD system is composed of a pulsed laser, a vacuum chamber, a rotation target holder and a substrate heating block as shown in Fig. 3.7. The target holder is able to contain several targets at the same time for the multilayer thin films. Normally, the target holder is rotating during the deposition in order to keep a fresh surface of the target always exposed to the laser beam. Generally, a substrate heating block is mounted parallel to the target and the focused laser beam incidents on the target at an angle of 45° to make the laser plume normal to the substrate surface. The substrate heating block can reach temperatures as high as 1000 °C. The chamber can be evacuated to a vacuum from 10⁻⁵mTorr to 10⁻⁷mTorr. Optimal laser fluence for film preparation depends on the ambient gas pressure and the substrate-target spacing and the crucial point for the deposition is how the plume interacts with the substrate. In order to suppress droplet formation in the laser deposition process, normally high-density targets are preferable in addition to using as low laser fluence as possible for a given system.

There are possibilities to vary wide range of parameters such as laser beam wavelength, laser pulse energy, frequency, focused spot size, reflectance and absorption coefficient of the target material, substrate temperature, pressure of the ambient gas, target-to-substrate distance and geometrical arrangement in the chamber.

The following are the general characteristics of PLD, compared with conventional film deposition techniques such as e-beam evaporation, sputtering, molecular beam epitaxy (MBE), chemical vapor deposition (CVD)[112].

**Stoichiometric (congruent) transfer of material**
If the focused laser energy density is chosen properly, films can have the same composition as the target. Stoichiometric transfer is the result of the high initial rate of heating and highly nonthermal target erosion by laser-generated plasma.

**Deposition from energetic plasma beam**
In the plume, atoms and ions have typical initial velocities of >10⁶ cm/s, which for an atom of 100 atomic mass units corresponds to a kinetic energy >52eV. The kinetic and internal excitation energies of ablated species can be used to assist film formation and to promote chemical reactions, both in the gas phase and on the growing film surface.
Capability for reactive deposition in the presence of ambient gases
Ambient gases can be used since there is no need for electron beams or hot filaments in the PLD chamber. The energetic species in the ablation plasma react readily with gas molecules to form simple compounds such as oxides, nitrides, and hydrides. Reactive deposition in low pressure oxidants such as O₂, O₃, NO₂, N₂O, or water vapor, in combination with the stoichiometric-transfer property, allows the laser-deposition of high quality thin films of multicomponent ferroelectric, ferrite, and biocompatible oxide ceramic material, which have been difficult to fabricate before.

Growth of multi-layered epitaxial hetero structures
The adjacent layers in the thin film structures have different composition whereas all layers share a common, continuous crystal structure. A separate target can be used to grow each layer, with a multi-target ‘carousel’ for rapid target exchange. The thickness of the each layer can be controlled by calibrating the deposition rate per laser pulse and counting the pulses. By choosing a low deposition rate (0.1Å/pulse), it is possible to control film growth near the atomic layer level.

Surface with Particulates
Particulates with diameters from 0.1 to 10µm (mostly <1µm) are usually present in PLD films. They are of particular concern if films must be lithographically patterned on a micrometer or smaller scale. There are a few experimental techniques developed to minimize the number and the size of the droplets: A laser with short wavelength, such as a deep UV excimer laser, can be used and the deposition conditions, such as the target rotation and laser beam scanning can be controlled for smooth surface. A rotating-vane ‘velocity filter’ can also be used to intercept most of the massive and relatively slow-moving particulates while transmitting the high-velocity atomic and ionic flux.

Small area of uniform thickness
A tightly focused pulsed laser beam produces a distribution of ablated material that is strongly peaked in the forward direction and thus the films with uniform thickness are produced only in a relatively narrow angular range. The practical solution to this problem is to move the ablation plume with respect to the substrate, ‘painting’ the substrate with the plume, or these motions can be combined to obtain uniform thickness depositions. It was shown that laser beam rastering over a large diameter target can produce uniform, large area films with predictable and reproducible growth rates and properties.

Table 3.6 Comparison of the Nd:YAG and Excimer Pulsed Lasers

<table>
<thead>
<tr>
<th>Types</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nd:YAG</td>
<td>• Simple Maintenance</td>
<td>• Large Energy-Drop in 3\textsuperscript{rd} Harmonic Mode</td>
</tr>
<tr>
<td></td>
<td>• Long Operation Life-Time</td>
<td>• Inclusion of other harmonics (1-2%)</td>
</tr>
<tr>
<td>Excimer</td>
<td>• High Power Output in UV</td>
<td>• Complicated Maintenance</td>
</tr>
<tr>
<td></td>
<td>• Good Stability</td>
<td>• Short Operation Lifetime</td>
</tr>
</tbody>
</table>
Among several kinds of lasers, which are commercially available for laser ablation, the choice of laser is one of the most important things before setting up a pulsed laser ablation system. ‘Laser’ stands for ‘light amplification by stimulated emission of radiation’ and one of the most common type of lasers for PLD is eximer (EXCIted state of dimers) laser[58, 111].

Excimer lasers (XeCl, KrF, ArF) are widely used because of the larger absorption coefficient and small reflectivity of materials at their operating wavelengths. Frequency tripled ($\lambda=355$nm) Nd:YAG lasers are also effective from the same point of view. The comparison between the Nd:YAG and the excimer laser in terms of advantages and disadvantages are listed in Table 3.6.

<table>
<thead>
<tr>
<th>Laser type</th>
<th>Wavelength [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nd:YAG</td>
<td>1064</td>
</tr>
<tr>
<td>Nd:YAG (2$^{nd}$ harmonics)</td>
<td>532</td>
</tr>
<tr>
<td>Nd:YAG (3$^{rd}$ harmonics)</td>
<td>355</td>
</tr>
<tr>
<td>Excimer - XeCl</td>
<td>308</td>
</tr>
<tr>
<td>Excimer - ArF</td>
<td>193</td>
</tr>
<tr>
<td>Excimer - KrF</td>
<td>248</td>
</tr>
</tbody>
</table>

In the excimer KrF laser, excimer KrF* is generated and when KrF is disassembled to Kr and F, a photon of 248 nm wavelength is radiated. The Nd:YAG laser is a classified in the category of solid-state lasers. Ionized Nd is used as the lasant and the crystal YAG ($Y_3Al_5O_{12}$) as the host, where 1~2 % of the metal ions is replaced by Nd$^{3+}$ ion. The output wavelength for the fundamental frequency is 1064 nm, which is close to the IR region. In Table 3.7, the typical wavelength values of different lasers are listed for comparison. The first parameter to be considered is the absorption coefficient and reflectivity of the materials to be deposited. For efficient deposition, the corresponding laser should be operated in a wavelength region where target materials have high absorption coefficients and low reflectivity since the absorption coefficient and the reflectivity are wavelength dependent.

In this work, mainly a KrF excimer laser with a 248-nm wavelength has been used to ablate PZT and Al$_2$O$_3$ targets with 3.5 $\text{J/cm}^2$ energy per pulse (Paper VI, VII, and VIII).
CHAPTER 4

Characterization

In this chapter, most of the measurement methods used in this work are discussed in more detail than in the appended papers. Various techniques such as XRD, AFM, SEM, SIMS, I-V, C-V, and P-E measurements are covered in this chapter whereas transistor results are presented in chapter 5.

4.1 Materials Characterization

4.1.1 X-ray Diffraction (XRD)

X-ray diffraction is used for characterizing the orientation and the phase contents of the thin films. The basis of XRD is Bragg’s Law, \( n\lambda = 2d\sin\theta \), where \( \theta \) is the diffraction angle associated with the interplanar spacing \( (d) \) that causes constructive reinforcement of the beam and specific X-ray wavelength \( (\lambda) \).[21]. The \( d \) corresponds to a particular lattice parameter or the spacing between the planes with the same Miller indices. In order to characterize the structural properties, normally three different types of measurements such as \( \theta-2\theta \) scan, \( \omega \)-scan, and \( \phi \)-scan can be used. In \( \theta-2\theta \) scan, the sample is rotating with respect to its own axis by the angle \( \theta \) and the detector is rotating with respect to the sample by the angle \( 2\theta \), as illustrated in Fig. 4.1.

![Fig. 4.1 XRD \( \theta-2\theta \) scan of SiC samples mounted (a) as is according to the wafer-cut direction and (b) on the growth orientation.](image-url)
As shown in Fig 4.1, in the experimental work of the thesis, $\theta$-2$\theta$ scans were performed to identify the phases and the orientation of metal contacts and ferroelectric thin films on SiC. Normally, the samples were mounted as it is cut from the manufacturer (Fig. 4.1 (a)). However, if the SiC substrate reflection needs to be measured, the samples were tilted around 3.5- or 8-degree off-axis depending on the growth orientation (see Fig. 4.1(b)).

In this work, the XRD measurements were accomplished by using a x-ray powder diffraction instrument, Siemens D5000, with Cu-K$\alpha_1$ anode. As shown in Fig. 4.2, $\theta$-2$\theta$ XRD measurements were performed to identify the phases formed on the SiC substrate before and after high-temperature annealing of a Ni contact at 950°C. It is shown that the reaction at the interface at high-temperature annealing only proceeds to the formation of the Ni$_2$Si phase whereas as-deposited Ni shows (111) orientation without Ni$_2$Si.

![Fig. 4.2 Comparison of X-ray patterns of as deposited and annealed (950°C) Ni on 4H-SiC (0001).](image)

The XRD patterns of the PZT films on SiC are shown in Fig. 4.3, where the PZT on SiC exhibits a polycrystalline structure without a preferred orientation for all samples. The top curves show SiC substrate peaks achieved by an 8° tilted scan with respect to the 4H–SiC wafer-cutting plane. As shown in Fig. 4.3(b), a tilted scan is needed to reveal the SiC substrate peak, since the substrates are cut at angle 8° off. The XRD peaks of the non-ferroelectric pyrochlore phase for PZT on SiO$_2$/SiC matches the reflection pattern of cubic Pb$_2$Ti$_2$O$_6$ (PDF 26-0142[113]), which is clearly diminished when PZT is deposited directly on SiC and on Al$_2$O$_3$/SiC.
Fig. 4.3. X-ray diffraction patterns of PZT(450 nm)/Al2O3(5 nm)/SiC, PZT/SiC, and PZT/SiO2 (8 nm)/SiC structures. Symbols (*) denote reflections of Pb2Ti2O6 (PDF 26-0142) pyrochlore phase.

4.1.2 AFM/SEM

The surface morphology of the thin film surface was examined by atomic force microscopy (AFM) and scanning electron microscopy (SEM).

**AFM**

In AFM, a fine tip at the end of a flexible cantilever is brought in contact with the film surface to be imaged. Forces acting between the tip and the surface will cause a bending of the cantilever proportional to the resultant force and it is measured by detecting the size of the bending. The force measured by the AFM is composed of all the attractive and repulsive forces acting between the tip and the sample. The deflection, \(\Delta z\), of the cantilever is proportional to the force, \(F\), acting on the tip; \(F = -k\cdot\Delta z\), where \(k\) is the spring constant of the cantilever. If \(\Delta z\) is comparable to the inter-atomic distance in the material which can be detected, then only \(k\) remains to be chosen properly. In crystals at a given temperature the atoms of mass \(m=10^{-22}\) kg, are vibrating with a frequency of \(f\) (typically \(10^{13}\) Hz or higher), which implies that these imaginary springs would have a spring constant, \(k = f^2 m\), of the order of 10 N/m. Therefore, the atoms at the surface will not be removed nor displaced by using a cantilever with a spring constant less than 10 N/m. Most cantilevers are fabricated with integrated tips from silicon, silicon oxide or silicon nitride using semiconductor device technology, thereby making it possible to fabricate cantilevers of extremely small dimensions and exhibiting force constants around 0.1 N/m. The topography of the sample influences the forces acting on the tip and thus also the deflection of the cantilever. The deflection of the cantilever can be monitored in different ways but the most common technique is the ‘optical lever’.
A laser beam is reflected by the end of the cantilever into a segmented light detector that detects the deflection of the laser spot and thus monitors the forces acting on the tip [114].

In Paper VI, we investigated Ohmic contact formation on the ICP-etched surfaces of 4H-silicon carbide using AFM. Fig. 4.4 shows typical AFM images of SiC surface of unetched sample and 60-W of platen-power etched samples. From the roughness measurements, a sacrificial oxidation (1250 °C, 1hr) seems to improve and recover the roughness to the same extent as that of a 30W etched sample.

**SEM**

The scanning electron microscope (SEM) is an instrument that produces a largely magnified image by using electrons instead of light. Since their development in the early 1950’s, SEM microscopes have been widely used in many areas including materials analysis. In SEM, a beam of electrons is produced at the top of the microscope by an electron gun. The electron beam follows a vertical path through the microscope in vacuum. The beam goes through electromagnetic fields and lenses, which focus the beam down toward the sample. As the beam hits the sample, electrons and X-rays are ejected from the sample. Detectors collect these X-rays, backscattered electrons, and secondary electrons and convert them into signals that generate the final image[114]. In this work a JSM 820 from JEOL has been used for SEM measurements.
Fig. 4.5 (a) A SEM image showing a profile dry-etched SiC with deposited SiO$_2$ mask and (b) a schematic diagram of the same.

Thick oxide masks can be used during dry-etching of SiC as shown in Fig. 4.5. The oxide mask layer can be formed either by PECVD or TEOS and the dry-etching rate of the oxide layer is around 68-70 nm/min while the SiC etching rate is about 110 nm/min under the standard etching condition of this work (600 W coil power, 300 W platen power, 5 mTorr). The oxide layer shows stable dry-etch rate irrespective of the densification or the deposition method. However, different etching angles can be formed for the different wet-etching profiles: PECVD-grown oxide layers have wet-etch rates of 98 nm/min and 75 nm/min for the as-grown and the densified condition, respectively, whereas on TEOS the etch rates are 230 nm/min for as-grown and 72 nm/mm for densified material. Moreover, different oxygen pressure during the etching is known to result in different slope in the profile.

The concentration of defects in a PZT film is a measure of its quality. Fig. 4.6 shows a SEM image of the region with so-called pinholes. In laser-deposited layers, the pinhole may be present with the particles aside. This pinhole can be formed by a bombarding particle from the explosion in the laser-target interaction process.

Fig. 4.6 A SEM image of the PZT surface on SiC showing the existence of pinholes in the PZT layer.
4.1.3 SIMS

In this work, the thickness of the $n$-epi layers on $p$-type SiC was measured by using Secondary Ion Mass Spectroscopy (SIMS). SIMS is an analytical technique, where a focused ion beam is used to bombard the surface of the sample. Since atoms and molecules are ejected under particle bombardment of a target\cite{115}, SIMS data can be recorded as mass spectra, depth profiles and ion images\cite{115}. If secondary ion intensity is recorded as a function of sputtering time, we can obtain depth profiling. In SiC however care must be taken as there can be differences between chemical dopant atoms and the electrically activated atoms. Commonly used primary sputtering ions include $O^-$, $O_2^+$, $Ne^+$, $Ar^+$, $Kr^+$, $Xe^+$ and $Cs^+$ with typical impact energies in the range of 1–20 keV\cite{116}.

SIMS has mainly been used to investigate the dopant depth profile of the epi layers for the device fabrication. The thickness of epitaxial layer has been measured with SIMS in order to check if the desired layers were grown before device processing. Fig. 4.7 shows an example of the depth profile of SIMS with Al concentration from $n$-epi layers over the $p$-layer/$p$-substrate.

![Fig. 4.7 The depth profile of SIMS from $n$-epitaxial layers on $p$-type layer. The inset on the left shows a schematic top and side view of the material and the inset on the right shows the estimated concentration of $p$-type layer and the depth.](image-url)
4.2 Electrical Characterization

For electrical measurements of the fabricated structures a probe station from Cascade Microtech has been used in this work. As described in Fig. 4.8, the probe station is mounted on a vibration free table and composed of a chamber with a chuck for sample mounting, a microscope, positioners with probe needles and a connection panel on the back[117]. The so-called ‘microchamber’ shields the chuck from electromagnetic and electrostatic noise. It is equipped with a roll-out stage that is furnished with a chuck, which is equipped with a heating system. The probe-positioners are mounted on the top lid of the microchamber, which is light proof and provided with dry-air during the measurements.

4.2.1 DC Measurements

For DC current-voltage measurements and transistor characterization, a computer-controlled HP4156A semiconductor parameter analyzer has been used[118]. It is equipped with four so called ‘High Resolution Source/Monitor Units (HRSMU)’. The current range is 20 fA–1 A and the voltage range is 1 µV–300 V with a maximum allowed total power of 2 W. The HP4156A is connected to the probe station via triax cables, which are especially important for measurements of small currents below ~1 nA, where very small leakage currents can have a large impact on the measured result. As shown in Fig. 4.9, the triax cable has both a guard and a shield whereas the coax cable only has only a shield. In a triax cable the signal and the guard is kept at the same potential level while the shield is connected to ground, which means that the guard voltage tracks the signal voltage precisely and no voltage drop occurs between the signal and force. The guard and sense are isolated by a buffer amplifier and this configuration allows a leakage current to flow between the guard and the shield without influencing the measurements.

Fig. 4.8 Schematic of a Cascade Microtech probe station
Specific Contact Resistance Measurements

It is important to characterize the properties of metal-semiconductor contacts in devices. Both rectifying Schottky and non-rectifying Ohmic contacts are required for different applications. In this section, the measurements of contact resistance are described after briefly discussing the theory.

For metals on a well-prepared surface of SiC, ideally the sum of the Schottky barrier height on $n$-type and $p$-type material would be same as the energy bandgap of the semiconductor, which is called the Schottky-Mott limit [119]. In case an offset exists due to Schottky barrier pinning at the interface with surface states, the Bardeen limit may dominate for this Schottky barrier [2]. In Schottky contacts, thermally excited electrons are the dominating current transport, called thermionic emission (TE), over the barrier. However, other mechanisms prevail if the doping concentration is high enough to have the depletion region very narrow. Then, as shown in Fig. 4.10 thermionic field emission (TFE) or field emission (FE) for even higher doping may dominate depending on the doping concentration.

Fig. 4.10 Schematic energy band diagram for a Schottky contact to a (a) low doped (TE), (b) intermediately doped (TFE) and (c) highly doped (FE) $n$-type semiconductor. The arrows indicate the direction of electron transport.
The resistance of the linear part of the current-voltage characteristics is very important for Ohmic contacts. Metallic Ohmic contacts to semiconductor are defined as a metal-semiconductor interface where the voltage drop is very small (ideally close to zero), compared to the active region of the devices. Specific contact resistance or contact resistivity can be given as \( \rho_c = R_C \cdot A \), where \( R_C \) and \( A \) are the contact resistance and the contact area, respectively. Specific contact resistance \( \rho_c \) has a unit of \( \Omega \text{cm}^2 \) and is commonly used to compare the quality of an Ohmic contact.

Fig. 4.11 shows the calculated specific contact resistance for the high doping regime in which FE and TFE may dominate[120]. The doping is very critical especially for contacts to SiC since normally the Schottky barrier heights are relatively high. Normally the specific contact resistance has to be measured for the material and metal after the annealing process. The annealing process needs to be optimised, since the specific contact resistance is reduced for increased temperature and annealing time, but only up to a certain limit.

In this work (Paper IV), the linear TLM method was used in order to determine the specific contact resistance. This method was originally proposed by Shockley[121] and the structure is composed of more than three contacts as shown in Fig 4.11.
In the TLM structure the total resistance between any two contacts \((L \geq 1.5L_T)\) are given as

\[
R_T = \frac{\rho_s d}{Z} + 2R_c, \quad \rho_C = R_c L_T Z
\]  

[Eq. 4.1]

From the total resistance \(R_T\) versus spacing \(d\) plot, as shown in Fig. 4.12, the following three parameters can be extracted: (i) sheet resistance \(\rho_s\) under the contacts - the slope, (ii) contact resistance \(R_C\), and (iii) the transfer length \(L_T\) - the intercept. As a result, the specific contact resistance \(\rho_C\) can be determined from Eq. 4.1.

**Breakdown and F-N Tunneling Measurements of Dielectrics**

In this work, current-voltage \((I-V)\) measurements were performed on 150 \(\mu\)m-diameter contacts using a HP 4156 parameter analyzer to study field-dependent breakdown characteristics and to estimate barrier heights in terms of Fowler-Nordheim analysis\[122\] (Paper III).

The \(I-V\) measurements were performed on accumulated MOS capacitors by stepping the bias of the metal from zero to positive for \(n\)-type and to negative for \(p\)-type SiC. Fig. 4.13 shows breakdown fields \(E_{BD}\) measured from 40 different devices of each set of samples. The breakdown generally occurs in the range of 8-12 MV/cm\[123\] with current densities as high as 100 A/cm\(^2\) at breakdown, which assures an intrinsic mechanism. It has been reported that the increase in the surface roughness causes oxide breakdown as well as the
interface states in MOS structures. The results clearly indicate that the oxide on etched surface has a lower $E_{BD}$ than the reference samples and the oxide on the sacrificial oxidation treated samples.

![Fig. 4.13 I-V breakdown measurements of 40 different MOS capacitors for each set](image)

At high oxide fields (>6 MV/cm), the conduction mechanism of $I$-$V$ characteristics of the 4H-SiC MOS samples could be described by Fowler-Nordheim (F-N) tunneling[122]. The F-N theory predicts the current density to be $J = A e^{B/E}$, and the slope of a typical F-N plot is given as $A = q^3 m / (16\pi^2 \hbar m_{ox} \phi_b)$, and $B = 4(2m_{ox})^{0.5} \phi_b^{1.5} / (3q\hbar)$, where $J$ is the current density, $E$ is the oxide field, $q$ is the electronic charge, $\hbar (=h/2\pi)$ is the reduced Planck's constant, $m_{ox}$ is the electron mass in the oxide, $m$ is the average effective mass for electrons in $n$-type MOS and for holes in $p$-type MOS.

![Fig. 4.14 Schematic diagrams of energy band diagram showing barrier heights in SiC MOS structures in accumulation. The arrows indicate the F-N tunneling or breakdown.](image)
For electrons in the bandgap of SiO$_2$ of n-type SiC MOS, $m=0.42m_0$ is known to be valid as in Si MOS case[124]. Waters et al.[125] have reported values of 0.23-0.37$m_0$ for the effective mass of holes from p-type 6H-SiC MOS structures. It is reported that the values of effective mass of holes in p-type 4H-SiC MOS is in the range of 0.35-0.52$m_0$ by Chanana et al.[126] Based on these investigations on the F-N hole tunneling in p-type SiC MOS, we have used 0.35$m_0$ for the effective mass value for holes. It is assumed that hole tunneling is the dominant conduction mechanism for p-type samples since the electron barrier of Ti is larger than the hole barrier at p-SiC (see the inset of Fig. 4.14(a)). The effective mass value for holes used in this work (0.35$m_0$) may not be physically accurate enough to consider the exact values of band offsets. However, it allows a relative comparison of the barrier heights ($\phi_b$) calculated from the slope of the F-N plots of different samples.

The values of $\phi_b$ obtained for n-type MOS by fitting the measured F-N slope are shown in Fig. 4.15(a). F-N tunneling of electrons from the conduction band of SiC into the oxide occurs for n-type SiC MOS capacitors in accumulation with electron injection. The barrier height difference seen in Fig. 4.15(a) between 6H- and 4H-SiC is due to the bandgap difference between these polytypes. Fig. 4.15(b) shows the barrier heights of p-type MOS extracted from F-N analysis. In p-type SiC MOS structures F-N tunneling of hole from the valence band of SiC to the oxide occurs owing to the smaller barrier for holes (2.5-2.9eV) than for electrons (3.38eV). Therefore, unlike n-type, no difference in the barrier height between 6H- and 4H-SiC was observed. However, it is observed for both n- and p-type MOS capacitors that the corresponding $\phi_b$ at the SiC/SiO$_2$ interface decreases for etch-damaged samples whereas the sacrificial oxidation treated samples shows higher barrier height comparable to the reference samples. The results suggest that the decreased $\phi_b$ in etch-damaged samples be attributed to the increased surface roughness and defect generation after ICP etching while the increase of $\phi_b$ in the sacrificial oxidation treated samples are due to the removal of the damaged region.

![Fig. 4.15](image-url)  
Fig. 4.15 The barrier heights between SiO$_2$-SiC in (a) n-type (b) and p-type samples. The values were extracted from the F-N analysis.
4.2.2 Capacitance Measurements

The interface properties of SiC metal-oxide-semiconductor MOS and metal-ferroelectric-(insulator)-semiconductor MF(I)S structures have been studied using $C-V$ measurements. High frequency $C-V$ measurements have been performed using a HP 4284A multifrequency LCR meter at room temperature[32]. With this equipment, the frequency can be varied from 10 HZ to 100 MHz and mainly the 100-800 kHz range has been used for the test and measurements, in the parallel configuration. The interface properties of SiC metal-oxide-semiconductor MOS and metal-ferroelectric-(insulator)-semiconductor MF(I)S structures have been studied using $C-V$ measurements. All the measurements were performed in equilibrium, by applying a negative bias for $n$-type and positive bias for $p$-type SiC and waiting until the capacitances become stable. Normally it takes 2-5 minutes for SiC capacitors to be in equilibrium with a focused halogen lamp. Dual direction voltage sweeps were performed at room temperature, starting from inversion by optical excitation with a focused halogen lamp to accumulation and then back to deep depletion[32, 127].

![Fig. 4.16](image-url) The $C-V$ voltage curves of $n$-type (a) 6H-SiC and (b) 4H-SiC and $p$-type (c) 6H-SiC, and (d) 4H-SiC MOS capacitors. The measurements were performed at 400kHz.
The maximum capacitance in accumulation reveals the oxide thickness $t_{ox} (=\varepsilon_{ox}/C_{ox})$. The doping in SiC can be determined from the minimum capacitance in inversion or from a plot of $1/C^2$ versus voltage curves in the depletion. The effective fixed charges $Q_F$ and interface states $Q_{IT}$ were determined from flat-band shift and a ledge feature of the $C-V$ curves, respectively.

Typical $C-V$ characteristics of $n$-MOS and $p$-MOS capacitors of 6H- and 4H-SiC are shown in Fig. 4.16. Dual voltage sweeps were performed, by using optical illumination to reach equilibrium at start. Upon the formation of inversion layers by a focused halogen lamp, the donor-type deep interface states in $p$-type SiC MOS are filled with electrons and become neutral whereas the acceptor-type interface states are discharged in $n$-type. The bias was then swept through the depletion region up to accumulation after the illumination was turned off. In the reverse sweep the curve is shifted due to the difference of the charge states of the deep interface states and so-called “interface state ledge” appears, as the deep interface states are present.

From this voltage shift ($\Delta V_{DD}$) between the two depletion sections of the $C-V$ characteristics, the total amount of deep interface states per unit area ($N_{IT}$) can be obtained as $N_{IT} = -C_{ox} \Delta V_{FB} q$, where $C_{ox}$ is the the accumulation capacitance and $q$ is the electronic charge. The flat band voltage shift ($\Delta V_{FB}$) relative to the theoretically calculated value gives the total fixed charge as $Q_{TOT} = (C_{ox} \Delta V_{FB})/q$, which includes the fixed oxide charge ($Q_F$) and $N_{IT}$. Theoretical values of flat band voltage were calculated based on the determination of the band offsets by Afanas’ev et al.[128] The fixed oxide charge is then calculated as $Q_F = Q_{TOT} - N_{IT}$, where $Q_F$ may also include other charges such as mobile ions or charged border traps as well as interface states. The thickness of oxide determined from the accumulation capacitance was in the range of 45-55 nm. For $p$-type MOS capacitors, large negative values of $\Delta V_{FB}$ and $\Delta V_{DD}$ were observed with large positive values of subsequently calculated $Q_{TOT}$ and $N_{IT}$. Such behaviour is known to be typical for MOS capacitors without post-oxidation annealing treatment.

![Fig. 4.17 C-V measurements of PZT/Al₂O₃ stacks on (a) n-SiC and (b) p-SiC, at 400 kHz. The solid lines are photo-illuminated measurements and the dashed lines are measurements in the dark. The thicknesses of PZT and Al₂O₃ are 450nm and 5nm, respectively.](image)
Table 4.1 Summary of the electrical characterization of MFIS structure on SiC

<table>
<thead>
<tr>
<th>Sample</th>
<th>PZT/Al₂O₃/n-SiC</th>
<th>PZT/Al₂O₃/p-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{FB}/C_{ACC}$</td>
<td>0.80</td>
<td>0.78</td>
</tr>
<tr>
<td>$\Delta V_{FB}$ [V]</td>
<td>5.92</td>
<td>-5.54</td>
</tr>
<tr>
<td>$Q_{TOT}[10^{12}\text{cm}^{-2}]$</td>
<td>-2.24</td>
<td>2.19</td>
</tr>
<tr>
<td>$\Delta V_{PH}$ [V]</td>
<td>9.57</td>
<td>-9.11</td>
</tr>
<tr>
<td>$N_{TOT}[10^{12}\text{cm}^{-2}]$</td>
<td>-3.62</td>
<td>3.60</td>
</tr>
<tr>
<td>$\Delta V_{HV}$ [V]</td>
<td>4.95</td>
<td>-4.18</td>
</tr>
<tr>
<td>$Q_{HV}[10^{12}\text{cm}^{-2}]$</td>
<td>-1.87</td>
<td>1.65</td>
</tr>
<tr>
<td>$Q_{F}(=Q_{TOT}-N_{TOT})[10^{12}\text{cm}^{-2}]$</td>
<td>1.38</td>
<td>-1.41</td>
</tr>
<tr>
<td>$N_{IT}(=Q_{PH}-N_{TOT})[10^{12}\text{cm}^{-2}]$</td>
<td>-1.75</td>
<td>1.95</td>
</tr>
</tbody>
</table>

Dry-etch damaged samples show even larger values of $\Delta V_{FB}$ as well as $\Delta V_{DD}$ than those without dry-etch damage. This can be attributed to the increased deep donor-type interface states and positive fixed charges due to the etch damage. On the other hand, sacrificial oxidation treated samples show clearly reduced $\Delta V_{FB}$ and $\Delta V_{DD}$, comparable to those of control reference samples, which is indicative of significantly suppressed generation of the interface states and traps. The calculated values of $N_{IT}$ and the fixed oxide charge ($Q_{F}$) are increased for ICP etch damaged samples, while the samples with a sacrificial oxidation show smaller values close to those of reference samples. It is clear from the calculated values of $N_{IT}$ and $Q_{F}$ that the interface properties are recovered for the sacrificial oxidation-treated samples, which is possibly due to the removal of the damaged region and the reduced roughness.

Similar measurements can be done on MF(IS) capacitors for the information about the interface. In this work, the measurements on MF(IS) structures were performed at a frequency of 400 kHz in parallel configuration, and a voltage sweep rate of 0.2 V/s (see Fig. 4.17).

The conductance at accumulation (12V) was as low as 0.1mS/cm², which was about more than 2 orders of magnitude lower than that of PZT directly grown on SiC (20 mS/cm²). As shown in Fig. 4.18, from an n-type SiC sample, the hysteresis curves both in the darkness can be explained in the following way: For a positive bias, electrons are accumulated in SiC and the polarization of PZT is aligned. Then, as the voltage increases, more and more accumulation would take place in SiC and the electrons are about to be injected. The accumulated electrons are injected towards the PZT/Al₂O₃ interface and consequently some of the carriers are trapped. After sufficient trapping has happened, which accordingly results in the screening of the polarization in PZT, the energy band in the surface of SiC bends upwards and the capacitance starts decreasing.
Fig. 4.18 Schematic energy band diagram and the corresponding $C-V$ measuring points of Au/PZT/Al₂O₃/n-SiC for (a) accumulation, (b) carrier trapping, (c) depletion, and (d) carrier detrapping. Note that the same model can be applied for the gate of a ferroelectric-transistor.
In the same way, the electrons in SiC are depleted as the bias voltage decreases. As the polarization direction of the PZT is reversed, the electrons are about to be detrapped and injected back to SiC side and then at some point the charge injection can finally occur. After enough injections the surface of the energy bands of SiC will now bend downwards, with capacitance increasing.

The different charges can be estimated from different voltage shifts in $C-V$ characteristics, from the $C-V$ curves of $n$- and $p$-type SiC, and with and without optical illumination (see Table 4.1). First, $Q_{\text{TOT}}$, the total charge responsible for the flat-band voltage shift, can be calculated. Then the theoretical flat band voltages of the samples (1.2 V for $n$-type and -1.6 V for $p$-type SiC) can be estimated by the work function difference between Au and 4H-SiC, assuming that no charge is present in the gate stack. Since $Q_{\text{TOT}}$ may consist of the nominal fixed oxide charge $Q_F$ and the total interface state charge $Q_{\text{PH}}$, which can be obtained from the voltage shift from the optical illumination. $Q_{\text{PH}}$ may include the interface states $Q_{\text{IT}}$ and the trapping charge $Q_{\text{HY}}$ in the PZT/Al$_2$O$_3$ stack. $Q_{\text{HY}}$ can be calculated from the voltage shift in the hysteresis in the darkness, and $Q_{\text{IT}}$ and $Q_F$ from the relation of $Q_{\text{TOT}} = Q_F + Q_{\text{PH}} = Q_F + Q_{\text{IT}} + Q_{\text{HY}}$. Although no precise analysis can be done from this simple calculation, we can still estimate the rough ratio of charges involved at room temperature. The detailed characterization results from the $C-V$ measurements.

### 4.2.3 Ferroelectric Properties Measurements

In case of ferroelectric thin films, properties such as remanent polarization $P_r$, coercive field $E_c$, relative dielectric permittivity $\varepsilon$ and loss factor $\tan\delta$ are the important parameters to be determined. Ferroelectric hysteresis is related to the growth and reorientation of the electrical polarization of domains as a function of applied field.

The schematic drawing of a Sawyer-Tower circuit[129, 130], is illustrated in Fig. 4.19(a). A large series capacitor is used to measure the change in polarization on the sample ferroelectric capacitors as a function of voltage.

![Fig. 4.19 Schematic diagram of (a) a Sawyer-Tower circuit and (b) a virtual-ground mode in RT66A.](image-url)
An alternating voltage is imposed across a pair of electrodes on the surface of a ferroelectric sample $C_s$, which is placed on the horizontal plate of an oscilloscope. The quantity plotted on the horizontal axis is proportional to the field across the sample. A linear capacitor $C_r$ is connected in series with the sample, the voltage across $C_r$ is therefore proportional to the polarization of the sample. This voltage is displayed on the vertical axis of the oscilloscope. Normally, by choosing sufficiently large value of $C_r$ compared to that of $C_s$ ($C_r >> C_s$), the potentials on the $x$ and $y$ plates of the oscilloscope can be approximated as $V_x = V$ and $V_y = V C_s / C_r$. If the applied voltage $V_{\text{max}}$ is enough for the sample to be saturated and for the domains to be switched, a well saturated hysteresis loop can be observed on the oscilloscope screen in the $x$-$y$ mode. The saturated polarization $P_{\text{sat}}$ and the coercive field $E_c$ can be determined from $P_{\text{sat}} = V_{\text{max}} C_r / A$ as $E_c = V_c / d$, where $A$ is the area of the ferroelectric capacitor and $d$ is the thickness of the ferroelectric thin film. The Sawyer-Tower circuit has been a common method for characterizing ferroelectric devices, however, it is susceptible to significant errors from parasitic elements (particularly associated with the sense capacitor hook up) and is limited by the accuracy to which the sense capacitor value is known.

The RT66A standard ferroelectric test system by Radiant Technologies Inc. [131] is an accurate and flexible commercial test system. It contains the Sawyer Tower mode and the virtual ground mode and most of the samples of the present work were measured by the RT66A in the virtual ground mode (see Fig 4.18(b)). The virtual ground mode measures the charge store in the ferroelectric sample by integrating the current required to maintain one terminal of the sample at zero volts. By eliminating the external sense capacitor, the circuit reduces the effects of parasitic elements and allows device characterization with high accuracy. In the RT66A, the pulse width and height can be controlled.

![Fig. 4.20 The hysteresis loops measured at room temperature for the MFMIS structure.](image-url)
In this work, the measurement was done with a pulse test system RT66A with 1.6 ms pulse and the saturation polarization $P_s$, remnant polarization $P_r$, and coercive field $E_c$ are 33.7 $\mu$C/cm$^2$, 14.2 $\mu$C/cm$^2$ and 58.9 kV/cm, respectively (Paper VII). These values are comparable to those of reported values of similar structure on Si or other substrates [58, 132], which can be attributed to the crystalline orientation of PZT that was highly dependent on the orientation of Pt (111).
CHAPTER 5

SiC Field Effect Transistors

This chapter is focused on the SiC devices studied in this work. An overview on the reported SiC devices in the recent literature are given in the first section. After a brief description on the physical background of FETs, the main results on the characteristics of the fabricated field effect transistors (FETs) are discussed.

5.1 Overview of SiC Devices

In this section, a brief overview is given on SiC devices including FETs, particularly for high voltage, high frequency, and high temperature applications.

5.1.1 High voltage devices

In SiC, high voltage can be realized on much thinner drift layers than in Si or GaAs. High breakdown voltage with lower on-resistance can be achieved due to the high critical electric field of SiC. So far good results have been demonstrated with a steady improvement in performance. An important figure of merit (i.e. BFM in Table 2.2 in Chapter 2) for high voltage devices is to calculate the specific on-resistivity, which allows the calculation of the forward voltage drop and on-state power losses. As seen in section 2.1.2, the specific on-resistivity can be given as

\[ R_{\text{on}} = \frac{W}{q\mu_n N_D} = 4V_B^2/eE_C^3. \]

Considering about 10 times higher \( E_C \) than in Si, the specific on-resistivity could potentially be 1000 times smaller for a SiC device. However, due to the smaller electron mobility and the slightly smaller dielectric constant, the actual gain is lower. Since the specific on-resistance is dependent on the blocking voltage of the device, the values of breakdown voltage squared over the on-resistance \( (V_B^2/R_{\text{ON}}) \) are compared in general, as shown in Table 5.1. In Fig. 5.1, the results are plotted with the ideal on-resistance of Si, 6H SiC and 4H SiC devices. So far diodes have been more successful in terms of the ideal on-resistance. Due to the low on-resistance through conductivity modulation, the highest breakdown voltages are from bipolar devices.
Fig. 5.1 On-resistance versus breakdown voltage for some recent high-voltage devices.

Table 5.1 On-resistances and breakdown voltages for some recent high-voltage devices.

<table>
<thead>
<tr>
<th>Device (Polytype)</th>
<th>$V_{BD}$ [kV]</th>
<th>$R_{ON}$ [m$\Omega$cm$^2$]</th>
<th>$V_{BD}^2/R_{ON}$ [MW/cm$^2$]</th>
<th>Group</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>pin Diode (4H)</td>
<td>19.5</td>
<td>65</td>
<td>5850</td>
<td>Kansai-CREE</td>
<td>[12, 133]</td>
</tr>
<tr>
<td>pin Diode (4H)</td>
<td>4.5</td>
<td>42</td>
<td>482</td>
<td>RPI</td>
<td>[134]</td>
</tr>
<tr>
<td>JBS Diode (4H)</td>
<td>2.8</td>
<td>8</td>
<td>980</td>
<td>KTH-ABB</td>
<td>[135]</td>
</tr>
<tr>
<td>Schottky Diode (4H)</td>
<td>4.9</td>
<td>43</td>
<td>558</td>
<td>Purdue</td>
<td>[136]</td>
</tr>
<tr>
<td>DMOSFET (4H)</td>
<td>2.4</td>
<td>42</td>
<td>137</td>
<td>CREE</td>
<td>[137]</td>
</tr>
<tr>
<td>SIAFET (4H)</td>
<td>6.1</td>
<td>732</td>
<td>51</td>
<td>Kansai-CREE</td>
<td>[138]</td>
</tr>
<tr>
<td>SEMOSFET (4H)</td>
<td>5</td>
<td>88</td>
<td>284</td>
<td>Kansai-CREE</td>
<td>[139]</td>
</tr>
<tr>
<td>ACCUFET (4H)</td>
<td>1.4</td>
<td>15.7</td>
<td>125</td>
<td>Purdue</td>
<td>[140]</td>
</tr>
<tr>
<td>DMOSFET (6H)</td>
<td>1.8</td>
<td>46</td>
<td>70</td>
<td>Siemens</td>
<td>[141]</td>
</tr>
<tr>
<td>JFET (4H)</td>
<td>5.5</td>
<td>218</td>
<td>139</td>
<td>Kansai-CREE</td>
<td>[142]</td>
</tr>
<tr>
<td>VJFET (4H)</td>
<td>2</td>
<td>70</td>
<td>57</td>
<td>Hitachi</td>
<td>[143]</td>
</tr>
<tr>
<td>VJFET (4H)</td>
<td>3.5</td>
<td>25</td>
<td>490</td>
<td>SiCED</td>
<td>[134]</td>
</tr>
<tr>
<td>BJT (4H)</td>
<td>1.8</td>
<td>10.8</td>
<td>300</td>
<td>CREE</td>
<td>[144]</td>
</tr>
<tr>
<td>BJT (4H)</td>
<td>0.5</td>
<td>50</td>
<td>5</td>
<td>Purdue</td>
<td>[145]</td>
</tr>
</tbody>
</table>
Chapter 5. SiC Field Effect Transistors

Diodes
Schottky diodes have a very simple structure of metal-semiconductor and are relatively fast since no minority carrier injection is involved. The on-state voltage (≈Schottky barrier height) can be low compared to that of the p-n diode (≈built-in voltage).

PiN diodes with a very low-doped drift region (almost intrinsic) are used for higher voltages. These are generally slower than Schottky diodes due to the minority charge injection, but can block higher voltages with less leakage current. The junction Barrier Schottky (JBS) diode is a Schottky diode with an integrated p-doped grid. Cree Inc. have reported the highest breakdown voltage for a PiN diode to date with 19.2 kV and a forward voltage drop of 4.9 V at 100 A cm\(^{-2}\). SiC JBS diodes are interesting in the 600-3300 V blocking voltage regime. In JBS diodes, the switching frequency and the blocking voltage/surge current capabilities are the promising features compared to PiN and Schottky diodes. Moreover, SiC Schottky diodes suffer from a rather high reverse leakage current, which is suppressed in JBS diodes. Substrate related crystal imperfections (i.e. screw and edge dislocations, low angle grain boundaries and stacking faults or remaining impurities) in the SiC must be improved.

FETs
It is possible to connect field effect transistors in parallel because of their positive temperature dependence. In field effect transistors switching is very fast since there is no p-n junction in the current path and therefore the built-in voltage can be neglected. On the other hand, for higher blocking voltages the on-resistance of the drift region is too high, and bipolar devices are preferred. In 4H-SiC MOSFETs, the measured on-state performances have been rather poor due to the low effective channel mobility. Recently, however MOSFETs fabricated on 6H- and 15R- SiC as well as on the (1120) or (0338) surface of 4H-SiC showed impressive performances. Doped-channel 4H-SiC U莫斯FETs with a breakdown voltage (\(V_B\)) of 3 kV and an on-resistance (\(R_{ON}\)) of 121 mΩ cm\(^{2}\) were demonstrated. Double-implanted MOSFETs in 6H-SiC showed properties exceeding 30 times the Si theoretical limit with \(V_B\) of 1.85 kV and \(R_{ON}\) of 46 mΩ cm\(^{2}\). Static channel expansion MOSFETs with 5.0 kV and \(R_{ON}\) of 88 mΩ cm\(^{2}\) has been demonstrated in 4H SiC, using accumulated MOS gate and p-n Junction gate[139, 146].

JFETs, being unipolar devices without any Schottky or MOS interface, have advantages due to the higher barrier and inherent stability of the p-n junction gate and do not suffer from the low channel mobility of the MOSFETs. Thus they are suitable for applications in which the normally on characteristic is not a severe disadvantage. The best performance published to date in a SiC majority carrier active switch was in a vertical JFET with \(R_{ON}\) of 26 mΩ cm\(^{2}\) and with a 3.5 kV breakdown voltage[123, 134]. High temperature operation of JFETs has also been demonstrated[17, 18, 147, 148]. On the other hand, in general, it is difficult to make the p-n junction gate short and therefore for high-frequency applications MESFETs are used (see the next section).

BJTs
SiC BJTs, thanks to the 10 times reduced collector drift region, have less stored charge, which allows faster switching compared to Si for the same power handling. Most of the reported SiC BJTs have epitaxially grown emitter regions and a typical current gain of
around 5-10. Recently, BJTs with excellent performances have been reported ($V_B=1800\text{V}$, $R_{ON}=10.8\text{m}\Omega\text{cm}^2$, $\beta=20$), where control of the surface passivation may play an important role for further improvement[144].

### 5.1.2 High-frequency Devices

SiC devices have shown considerable improvement and superior RF power performance to those available from Si or GaAs devices. Better high frequency figures of merits are attributed to improved material properties such as bandgap, critical electric field, thermal conductivity as well as the saturation electron velocity, and also to a reduced capacitance from decreased device area (see chapter 3 as well). Recently demonstrated results on SiC RF power devices are listed in Table 5.2. There are several figures of merit for comparing high frequency devices, such as maximum operating frequency ($f_T$) or maximum frequency of oscillation ($f_{\text{max}}$). It is usual to scale the output power with the gate width when comparing devices with different dimensions at the operating frequency. Any device used in a circuit to measure the output power needs an $f_T$ and $f_{\text{max}}$ about ten times higher than the operating frequency as a rule of thumb (see Fig. 5.2).

#### Table 5.2 Output power density and operating frequency for some recent high frequency devices.

<table>
<thead>
<tr>
<th>Device (Polytype)</th>
<th>Frequency (GHz)</th>
<th>Power Density (W/mm)</th>
<th>Mode</th>
<th>Total Power (W)</th>
<th>Group</th>
<th>Ref.</th>
</tr>
</thead>
</table>
| IMPATT diode (4H) | 9.9            | 300mW                | Pulsed | 62            | Ioffe Inst. | [149]
| IMPATT diode (4H) | 7.2            | 9kA/cm$^2$           | Pulsed | 54            | CREE  | [151, 152]
| MESFET (4H)       | 3.5            | 5.2                  | Pulsed | 8             | Thomson | [153]
| MESFET (4H)       | 10             | 4.5                  | Pulsed | 54            | CREE  | [151]
| MESFET (4H)       | 2              | 4                    | CW    | 78            | CREE  | [151]
| SIT (4H)          | 1.3            | 1.67                 | Pulsed | 400           | Northrop Grumman | [154]
| SIT (4H)          | 2.9            | 1.51                 | Pulsed | 78            | Northrop Grumman | [155]
| GaN HEMT          | 3.5            | 12.1                 | Pulsed | 145           | Cree  | [152]
| AlGaN HEMT        | 10             | 4.2                  | Pulsed | 50.1          | Cree  | [152]
| AlGaN HEMT        | 20             | 6.6                  | CW    | 1.32          | HRL Labs. | [156]
| MOSFET (Si)       | 3.2            | 1                    | CW    | 2             | Ångström Lab. | [157]
| MODFET (GaAs)     | 2.16           | 2.22                 | Pulsed | 200           | Matsushita | [158]
IMPATT Diodes
The RF Power available from an impact ionization avalanche transit time (IMPATT) diode in SiC is 100 times higher than in Si or GaAs. During the last few years promising devices have been demonstrated for IMPATT diodes with X-band operation and microwave power of 300mW\cite{149}. Despite its high power density the efficiency is very low, in the range of 1%.

MESFETs
SiC MESFETs are developed as power transistors for operating frequencies in the 1-10GHz range (from UHF through X-band). Cree Inc. is marketing MESFETs with a best performance of 5.2W/mm at 3.5GHz and 63% power added efficiency (PAE) for a 0.7µm×48mm device and monolithic microwave IC (MMIC) amplifiers based on these devices have also been demonstrated with a power of 36.3W, associated gain of 0.5dB, and PAE of 20.6\%\cite{152}.

SITs
Static Induction Transistors (SIT) are also unipolar devices with a $p$-$n$ junction or a Schottky-controlled gate. Normally, a SIT has a vertical channel structure for higher power density but is restricted to lower frequencies (UHF to C band) compared to MESFETs with a lateral channel.

HEMTs
Most high frequency work today is concentrated on improving the growth of nitrides, since HEMTs have showed much better high frequency characteristics than MESFETs. SiC would then be an ideal substrate in the absence of nitride substrates, due to better...
thermal conductivity than sapphire. High electron-mobility transistors (HEMTs) based on the AlGaN/GaN heterostructure show very promising device operation at frequencies of 10 GHz and higher. In this structure, a 5 times higher two-dimensional electron gas (2DEG) than in the AlGaAs/GaAs structures allows a higher current capability. However, conventional GaN devices on Sapphire substrates are not well suited due to a poor lattice match between GaN and Sapphire (13%) and thus high defect density ($10^{8}$/cm$^2$). By using a SiC substrate, the lattice mismatch can be decreased and the efficient heat sinking is possible due to higher thermal conductivity of SiC. Recently HEMTs with power densities of 10.7 W/mm at 10 GHz, 6.5 mW/mm at 20 GHz[156], and $f_T$ as high as 101 GHz have been reported.

5.1.3 High temperature devices

The wide bandgap of SiC results in very low intrinsic carrier concentration, which means that SiC devices could theoretically operate up to 1000 °C. This would allow the application of electronics in high temperature environments, such as in or close to combustion engines and other hot processes. Although both digital and analog circuits have been demonstrated using MOSFETs and JFETs, respectively, this does not seem to be a big market yet. One problem is the long-term reliability of devices and circuits, which will probably limit operation before the material itself. Packaging of high temperature electronics is another area in need of research. Finally, threshold voltages and operating points will shift with temperature, so the electronic circuit design will need to take this into account.

In this work, we have designed and fabricated, a buried-gate JFET with an additional MOS-gate on top, which operates with constant on and off current levels from room temperature up to 300 °C (Paper V).

An application that seems closer to actual use is catalytic gas sensors. The basic principle is to use a catalytic metal (Pt, Pa, Ir etc) as gate on a metal-oxide-semiconductor (MOS) structure. Some gases will crack or decompose on the catalytic metal, and hydrogen ions can be sensed on the gate by the shift in flatband voltage. Several devices based on this principle have been demonstrated in several different sensor applications for combustion processes[159]. Temperature sensors for higher temperatures are another possibility. Almost any electronic device can be used as a temperature sensor. It is mainly a question of finding a property that can be measured accurately in the temperature range and that preferably has linear temperature dependence. Reverse leakage current in diodes is one alternative. Using the change in a transistor parameter such as the current gain adds to the sensitivity if the amplification in the device can be used.
5.2 SiC Field Effect Transistors

5.2.1 Background of FETs

An analytical model is studied in this section to understand the basic principles of SiC FETs, which is useful for the device design and optimization. Two types of FETs, namely the JFET and the MOSFET are considered in this work. Both devices have a similar principle involved, as in the MESFET.

As shown in Fig. 5.3, the FETs may be divided into junction FETs (JFETs), metal-semiconductor FETs (MESFETs) and metal-oxide-semiconductor FETs (MOSFETs). Junction FETs are inherently depletion-mode devices, and are available in both $n$- and $p$-channel configurations. MOSFETs are available in both enhancement and depletion modes, and also exist as both $n$- and $p$-channel devices. The different FET groups depend on different phenomena for their operation.

The JFET involves a gate electrode separated from the source and drain by a $p$-$n$ junction, whereas the MOSFET has an insulating layer between the gate and the other electrodes. The Ferroelectric-FET is a special kind of MOSFET, where a ferroelectric layer is used as its gate dielectric instead of SiO$_2$.

The MOSFETs have several advantages and disadvantages compared to the JFETs. The insulation in the gate allows either polarity for the gate-source voltage for either $n$-channel or $p$-channel devices. By varying the channel doping we can obtain devices that normally conduct or normally do not conduct from drain to source (at $V_{GS} = 0$). There are four possible types in MOSFET devices.

![Fig. 5.3 Different types of FETs and electric symbols](image_url)
The field-effect transistor was first analyzed by W. Schokley in 1952[5]. Based on Schokley’s theoretical approach, the first fabricated FET was reported by Dacey and Ross in 1953[160]. Since then, the FET has been widely used in various electronic applications. The carrier transport in a FET is made up predominantly of the majority carriers (unipolar device), and thus the switching speed of FET is not limited by the minority carrier charge storage such as that in the bipolar junction transistor.

Typical cross-sections of an $n$-channel FET is shown in Fig. 5.4, where the gate is used to control the current and the gate voltage is negative with respect to the source. The JFET uses the depletion region of a reverse biased $p$-$n$ junction gate to modulate the cross-sectional area available for current flow, whereas MOSFET depletes the semiconductor under the oxide gate. The MESFET is conceptually the same as JFET but the gate is made of a Schottky junction. However, due to the semi-insulating layer and the small gate area, the parasitic capacitance can be reduced for MESFETs compared to JFETs, and therefore MESFETs are normally preferred for high frequency applications.

![Idealized cross section of $n$-channel (a) buried-gate JFET, (b) MESFET, and (c) depletion-type MOSFET](image)

Fig. 5.4 Idealized cross section of $n$-channel (a) buried-gate JFET, (b) MESFET, and (c) depletion-type MOSFET
The following analytical consideration can be applied to both the JFET and the depletion-mode MOSFET. The “long channel approximation” (="gradual channel approximation”) can be considered in order to analyze the FET characteristics. This approximation, first done by Shockley, essentially assumes that the channel is much longer than its width ($L >> a$), which allows the following assumptions[43, 97].

(i) The electric field in the depletion region varies only in the $y$-direction; i.e. the voltage doesn’t change rapidly in the $x$-direction.

(ii) The electric field in the channel region (neutral region) varies only in the $x$-direction; i.e. the gate field has no influence in this region.

These assumptions allow a one-dimensional solution of Poisson’s equation in the two regions. If the gate junction is a one-sided step junction, then the depletion layer width $W(x)$ is given depending on the device type and geometry.

If we assume a uniform channel ($n=N_D$, $dn/dx=0$; quasi neutrality), the current in the channel of the FET is only due to the drain potential and the conductivity is given by $\sigma(x)=qN_D\mu_n$ where $\mu_n$ is the electron mobility. Since the electric field is $\varepsilon(x)=-dV(x)/dx$, the current density can be represented as $J(x)=\sigma(x)\varepsilon(x)$. Thus the current in the channel is given by

$$I_D(x) = J(x)A = \sigma(x)\frac{dV(x)}{dx} A$$

$$= \sigma(x)\frac{dV(x)}{dx} [a - W(x)]Z$$

$$= q\mu_n N_D \frac{dV(x)}{dx} [a - W(x)]Z$$

[Eq. 5.1]

where $Z$ is the width of the channel in FET.

\[\text{Fig. 5.5 Ideal current-voltage characteristics of a FET}\]
The total current through the channel can be obtained by substituting \( W(x) \) into Eq. 5.1 and integrating from \( x=0 \) to \( x=L \).

\[
I_D = \frac{1}{L} \int_0^L I(x) \, dx
\]  
[Eq. 5.2]

At very low drain voltages, the drain current increases linearly with increasing drain voltage. (see Fig. 5.5) In this linear region, the FET exhibits a resistive characteristic with the resistance as a function of the gate voltage. This resistance can be obtained by differentiating Eq. 5.2 with respect to the drain voltage \((1/R = dI_D/dV_D)\). This equation only applies to the channel region, when the additional resistance contribution is excluded.

As shown in Fig. 5.5, the drain current \((I_D)\) increases with increase in the drain voltage \((V_D)\) and becomes saturated at the pinch-off point. The gain of the device, called transconductance, is given by

\[
g_{m} = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_{gs}=\text{const}}
\]  
[Eq. 5.3]

The transconductance represents the change of the drain current at a given drain voltage upon a change in gate voltage. A large transconductance is desirable to minimize the gate drive and provide high power gain.
5.2.2 Fabrication Process for SiC FETs

The fabrication process for the FETs fabricated in this work required 2- or 3- mask steps (see Fig. 5.6-5.8) for buried-gate JFETs and 5- to 7- mask steps (See Fig. 5.9-5.11) for JMOSFETs and FeFETs depending on the design. All the lithography was performed with a Cannon 4:1 mask aligner and the photoresist Shipley 1813 and 1818 have been mainly used, while an image-reversal photoresist AZ5214, which is similar to a negative photoresist, has been used if required.

![Fig. 5.6 Images of (a) the full mask layout and (b) the different JFET structures](image)

Fig. 5.6 Images of (a) the full mask layout and (b) the different JFET structures

![Fig. 5.7 Pictures of different JFETs showing (a) vertical wall with 2 mask steps and (b) sloped wall with 3 mask steps. The insets are SEM images. The dotted lines are for the cross-sections of the process flow in Fig. 5.8.](image)

Fig. 5.7 Pictures of different JFETs showing (a) vertical wall with 2 mask steps and (b) sloped wall with 3 mask steps. The insets are SEM images. The dotted lines are for the cross-sections of the process flow in Fig. 5.8.
Fig. 5.8 Schematic diagrams of SiC JFET process flow with 3-mask steps. Two different processes are shown from step 13, with (right) and without passivation (left). Note that in the case of the 2-mask process, the same mask can be used in step 7 and step 14.
Fig. 5.9 Images of (a) the full mask layout, (b) the different FET structures, and (c) a single FET for JMOSFETs and FeFETs.

Fig. 5.10 (a) a SEM image of a FeFET and (b) Optical images of different FeFETs
Fig. 5.11 Schematic diagrams for SiC FeFET process flow. Note that JMOSFET can also be fabricated in the same process by modifying step 17.
5.3 FET Characterization Results

5.3.1 JFETs

The schematic cross-sectional structure of the fabricated BG JFETs is shown in Fig. 5.12. A $p$-type SiC wafer of 4H-polytype from CREE Research Inc. with the epitaxial layers ($p^+$, $n$, and $n^+$) grown by chemical vapor deposition (CVD) at Linköping University has been used. The thickness of $p^+$, $n$, and $n^+$ epitaxial layers were 0.5, 5, and 0.5 $\mu$m, respectively. Approximate doping is indicated in Fig. 5.12.

After the mesa structures were defined for the device isolation, the channel regions were formed by dry etching of SiC in an inductively coupled plasma (ICP) chamber. ICP etching was performed with a RF coil power of 600 W and a platen power of 30 W in a mixture of SF$_6$ (21 sccm) and Ar (9 sccm). E-beam evaporated Ni was used as both dry-etch mask and front contacts, resulting in good etch selectivity, and sputtered TiW was used as a backside gate contact. The total fabrication process for the device required only 2 mask steps. Rapid thermal annealing was then performed at 950 °C for 30 s in 10 % H$_2$/Ar ambient for Ohmic contact formation. The JFETs have gate widths of 100 to 1200 $\mu$m, and various channel lengths ($L$) in the range of 5 to 25 $\mu$m. Different values of the channel thickness ($a$) of around 0.1-1.5µm have been characterized.

The $I$-$V$ characteristics of JFETs were measured in a Cascade probe station using a HP 4156A semiconductor parameter analyzer. Fabricated JFET devices generally exhibited well-saturated drain currents, which is close to the behavior of the one-dimensional gradual channel approximation (GCA)[3]: The drain current was proportional to the channel thickness ($a$) and inversely proportional to the channel length ($L$), except for a very small channel thickness ($a \leq 0.3$ µm). Due to the limitation of the assumptions in GCA, a closer agreement can be reached to the measurement by using ATLAS$^{TM}$ 2-dimensional numerical simulations of the devices. Different $I$-$V$ characteristics are observed between device A and B only for thin channels ($a \leq 0.3$ µm).

Fig. 5.12 Schematic cross-sections of the two different types of 4H-SiC buried-gate JFETs fabricated in this work (not drawn to scale).
The measured drain currents versus drain voltage ($I_{DS}-V_{DS}$) characteristics of a typical 4H-SiC BG JFET with a channel width of 100 µm are shown in Fig. 5.13. The gate voltage was varied from 0 to –25 V with –2.5 V per a step. The maximum measured transconductance ($g_m$) of the device was 2 mS/100 µm, which corresponds to 20 mS/mm. The breakdown voltage for this device was 225 V when measured in air without any surface passivation, which was far less than a simple theoretical calculation of the breakdown voltage (>700 V) considering the $n$-epitaxial layer doping thickness. The discrepancy between the calculation and the experimental results might be further reduced with improved $p$-$n$ junction quality as well as with proper passivation layer and termination in the fabricated structure.

**Fig. 5.13** Drain currents versus drain voltage curves of a typical 4H-SiC JFET

**Fig. 5.14** Measured (a) drain current vs. drain voltage and (b) drain current vs. gate voltage characteristics at different temperatures. The inset shows the variation of saturated drain currents and the calculated maximum transconductances ($g_m$) normalized to the room temperature values.
Fig. 5.14 shows the temperature dependence of the JFET \((W=100\, \mu\text{m})\) from 25°C to 300°C. Over this temperature range, the device maintains good saturation characteristics. The decrease of the drain current is attributed to the reduction in the carrier mobility for a temperature increase. As the temperature increases, the drain current and the maximum transconductance decreases to around 30% of the room temperature value at 300°C as shown in the inset of Fig. 3. This behavior is similar to low-voltage 4H-SiC JFETs with a shallower trench structure as reported by Scozzie et al[161].

However, as the channel thickness becomes smaller \((a\leq0.7\, \mu\text{m})\), the characteristics of device A do not agree with GCA and show poor saturation with linear behavior in the sub-threshold region of the \(I-V\) curves. Device B, on the other hand, maintained well-saturated \(I-V\) characteristics for very small channel thickness \((a\leq0.5\, \mu\text{m})\). Typical \(I-V\) characteristics of the thin channel JFET devices \((L=15\, \mu\text{m}, a=0.5\, \mu\text{m})\) are shown in Fig.5.15, together with the results from ATLAS simulations. Important physical parameters used in the simulations were adjusted according to recently reported data. It is shown that good agreement is reached between the measurements and the simulations for both types of devices. In device A, as the channel thickness decreases, even a small gate voltage in addition to the built-in potential of a \(p-n\) junction can locally deplete the channel under the trench edge. Therefore, the static induction transistor (SIT)-like characteristics, the so-called 'triode' regime[162], appear in the low drain voltage region of \(I-V\) characteristics of device A, until the drain-source voltage reaches a certain level.

**Fig. 5.15** Comparison of simulated and measured drain current vs drain-source voltage for different gate voltages in thin channel devices \((a=0.5\, \mu\text{m})\); Triangles and circles are measured from device A and device B, respectively, and solid lines are from 2-dimensional numerical simulations.
Fig. 5.16 shows the normalized potential distributions along the dotted lines (from P to Q) in the channel region of the 4 different simulated devices for a gate-source voltage (V$_{GS}$) of -0.5 V. The potential profiles of devices with trenching effect passing through the channel (see Fig. 5.16 (a) and (c)) indicate the existence of a local minimum value at X=1.0 for low drain voltages (V$_{DS}$=1 and 2 V), resulting in a potential barrier.

The channel potential is lower than the potential towards source (at point P in the inset of Fig. 5.16) and the input and output of these devices become isolated and the barrier prevents carriers from flowing towards the drain. Thus, for low drain voltages, SIT-like characteristics are obtained. If the applied drain voltage is high enough (V$_{DS}$=5, 10, and 30 V), the field in the conducting channel increases with increasing drain voltage, and the potential barrier is diminished and the carriers begin to flow. In devices without trenching effect (see Fig. 5.16 (b), and (d)), the channel potential does not show any potential barrier and the potential towards drain (at point Q) is higher than the potential toward source (at point P) for all the drain voltages given. As a result, the pentode-like characteristics of conventional JFETs are maintained.

![Fig. 5.16](image_url)

**Fig. 5.16** The channel groove region of the simulated (a) devices A and (b) device B, and the normalized potential (V/V(x=0)) profiles in (c) device A and (d) device B for V$_{GS}$=-0.5V along the dotted line from P to Q in the figure (a) and (b).
Switching measurements with inductive load were performed with the fabricated SiC JFET (W=1200 µm, L=8 µm, total pad area=0.12 mm²). The measurement circuit is schematically illustrated in Fig. 5.17. The inductive load has a SiC p⁺nn⁺ freewheeling diode [10]. A double pulse was used to obtain a constant current through the 100 mH load inductance (L_{load}) and the JFET is then turned rapidly off and on again. The gate drive circuit uses a power MOSFET and a gate resistance of 4.7 Ω, and 70 V is applied to MOSFET with its source connected to the JFET gate. The JFET is connected on wafer using probe tips on top of the source and drain pads and the gate bottom contact is pressed against a Cu plate. The sample is inside a bowl containing Fluorinert™ to avoid dielectric breakdown in the ambient.

Fig. 5.18(a) displays a measured turn-off of 0.22 A against 100 V (solid lines). A two-dimensional semiconductor simulation software program Medici™ is used for this investigation (dotted lines). Physical models for doping and electric field dependent mobility, incomplete ionization, SRH and Auger recombination, incomplete dopant ionization and Fermi-Dirac statistics have been used and external circuit elements are included in the simulation. A voltage pulse serves as model for the MOSFET switching and the JFET and p⁺nn⁺ diode are both simulated as finite element structures.

The simulator solves basic semiconductor differential equations based on the defined device structures of SiC JFET and SiC diode with boundary conditions including circuit configurations. Further device optimization can be based on the simulation results. The measured turn-off is very fast with a drain voltage rise-time of about 30 ns, which is still...
significantly slower than the simulation. This discrepancy suggests additional parasitic capacitances, which could be caused by sample holder and cables.

Fig. 5.18(b) shows the measured turn-on with a drain voltage fall-time of about 25 ns. A current peak of nearly 0.6 A during turn-on is caused by the reverse current peak in the freewheeling SiC p''nn'' diode which has an active area of 0.5 mm². A fast turn-on with a relatively low current peak is verified for the JFET together with the SiC p''nn'' diode. The performance can be further improved by the use of a SiC Schottky diode, which has both a lower on state voltage and a smaller reverse current during switching compared to the SiC p''nn'' diode. An increased device area could reduce the effects of parasitic capacitances and enable a more accurate comparison with simulations.

![Fig. 5.18](image)

Fig. 5.18 Turn-off (a) and turn-on (b) behavior of a JFET in the test circuit. Solid lines are measurements and dotted lines are simulations.
5.3.2 SiC JMOSFETs

While the high temperature performance of SiC transistors has been demonstrated so far, the current level at high temperatures is drastically reduced compared to that at room temperature. This variation of operating point makes it difficult to use the SiC devices at high temperatures. In order to improve the high temperature stability and the on-state resistance, we have designed a novel combination of junction-gated and metal-oxide-semiconductor field effect transistor (a so-called JMOSFET), which alleviates this problem. The high-temperature stable operation of JMOSFETs has been explored in terms of constant current levels in this work. A schematic cross-section of the fabricated transistor is shown in Fig. 5.19.

**Fig. 5.19** Schematic cross-section of the 4H-SiC Junction-MOS field-effect transistor with an n-channel.

**Fig. 5.20** Static drain current $I_D$ versus drain voltage $V_D$ characteristics of JMOSFET. By applying a proper bottom gate voltage $V_{BG}$, constant currents can be achieved for temperatures from RT up to 300°C. The inset shows different $V_{BG}$ for different temperatures.
The JMOSFET has a similar epi-structure as the buried-gate JFET but with additional MOS gate to deplete the channel from the top. Also in principle it can be fabricated in the same process steps as ferroelectric FET, which is described in the next section. From the backside buried gate, the channel of all devices on the same wafer can be easily controlled thereby allowing constant current level over different temperatures. The JMOSFETs have shown the feasibility for operating with constant on and off current levels from room temperature all the way up to 300 °C. This has been experimentally demonstrated in Fig. 5.20. By applying a properly chosen voltage on the backside buried gate $V_{BG}$, the channel of all devices on the same wafer can be simultaneously controlled, which thereby allows a virtually constant current level operation for different temperatures. The correspondingly chosen values of $V_{BG}$ to set the operation point for different temperatures, are shown in the inset of Fig. 5.20.

The results are also compared with numerical simulation by Dessis-ISE (see Fig. 5.21). Fig. 5.21 shows the normalized drain current $I_D/I_{D,\text{max}}$ as a function a temperature. The results are also compared with the results from a two-dimensional numerical simulator Desis from ISE AG. A monotonic decrease in $I_D$ for the temperature increase mainly attributed to the power-law degradation of electron mobility above room temperature. This allows for simple control using a feedback loop, which monitors the drain current, to apply a voltage to the buried backside gate, thereby maintaining constant drain current for all devices.

Other advantages of this device include the relatively high bulk channel mobility, compared to enhancement mode MOSFET which normally shows low inversion channel mobilities. Even higher bulk mobility than that of JFET can be achieved by accumulating the channel in JMOSFET. Typical gate characteristics are shown in Fig. 5.22.

![Normalized Drain Current vs Temperature](image)

**Fig. 5.21** The inset shows the comparison between numerical simulation and measurements for the saturated drain currents normalized to the room temperature values.
Fig. 5.22 The top-gate characteristics showing the variation of saturated drain currents and the calculated maximum transconductances \((g_m)\) normalized to the room temperature values at fixed bottom gate voltage of 0 V.

5.3.3 FeFETs

The ferroelectric field effect transistor (FeFET) structures were fabricated on \(p\)-type substrate of 4H-silicon carbide using \(n\)-type epitaxial layers and had a nominal gate width and a length of 100 \(\mu\)m and 10 \(\mu\)m, respectively. The nitrogen donor concentration in the \(n\)-type channel epitaxial layer was \(~2\times10^{16}\ \text{cm}^{-3}\) and the \(p\)-substrate was doped to \(~2\times10^{18}\ \text{cm}^{-3}\) with aluminium acceptors. The channel region and mesa isolation of transistors were formed by photolithography and dry etching of SiC. Around 200 nm-thick oxide was grown to passivate the surface and the source and drain contacts were electron beam evaporated Ni, which was patterned by photolithographic lift off process.

Fig. 5.23 Schematic cross-section of the 4H-SiC ferroelectric field-effect transistor. The transistor can be classified as depletion-type and has a PZT and \(\text{Al}_2\text{O}_3\) gate stack on top and a buried junction gate.
The backside contact was sputtered TiW and all these contacts were rapid thermal annealed at 950 °C for 1 min to form good Ohmic contacts. 5 nm Al$_2$O$_3$ layer was grown on SiC by pulsed laser deposition using a KrF excimer laser, prior to depositing 450 nm PZT layer. Al$_2$O$_3$ was used in order to allow single-phase growth of PZT on SiC and to act as a high bandgap buffer ($E_g \sim 9$ eV) between PZT ($E_g \sim 3.5$ eV) and SiC ($E_g \sim 3.2$ eV), according to Paper VI and Paper VII. A PbZr$_{0.52}$Ti$_{0.48}$O$_3$ ceramic target were used to deposit PZT at 580 °C and Au was evaporated and patterned to form gate electrodes. The cross-sectional schematics of the SiC field-effect transistor with ferroelectric PZT and Al$_2$O$_3$ gate stack is shown in Fig. 5.23. The fabricated transistors are normally-on, depletion-type devices since the modulation of the channel current is controlled by depleting or accumulating the channel from the ferroelectric gate. In this configuration, the channel-substrate junction can be used as an extra $p$-$n$ junction gate, enabling additional channel modulation.

The saturated drain currents $I_D$ as a function of gate voltage $V_G$ of the transistor are shown in Fig. 5.24. Dual directional sweeps of $V_G$ were performed at room temperature between −12 and +12 V, the drain voltage $V_D$ is kept constant at 10 V and the buried junction gate voltages were 0, -2, -4 V. In can be clearly seen that $I_D$–$V_G$ characteristics exhibited a memory effect; depending on the sweep direction, two different values of $I_D$ can be measured for the same gate voltage. The memory window of the transistor is 5.0 V, which agrees with the value reported earlier from $C$-$V$ measurements on the diode structure of PZT/Al$_2$O$_3$/SiC.

![Graph of drain current vs. top-gate voltage](image)

**Fig. 5.24** Gate transfer characteristics (drain current $I_D$ versus $V_G$) of the 4H-SiC ferroelectric field-effect transistor. The sweep direction is clockwise for all curves.
In the ideal case of ferroelectric field-effect transistors\cite{163} the hysteresis direction is opposite to what we observed, where the absence of interface states and bound charges could diminish the expected effect. These contribution to the different sweep results are: The charges can be injected from the semiconductor into the ferroelectric or interface traps and attracted by the remnant polarization and consequently become bound to the ferroelectric domains when the applied field is removed.

![Graph showing static drain current \( I_D \) versus drain voltage \( V_D \) characteristics with top-gate \( V_{TG} \) sweep after different \( V_{TG} \) of +12 and –12 V was applied on top.](image1)

**Fig. 5.25** Static drain current \( I_D \) versus drain voltage \( V_D \) characteristics with top-gate \( V_{TG} \) sweep after different \( V_{TG} \) of +12 and –12 V was applied on top.

![Graph showing top-gate characteristics for \( V_{TG} \) from +4 to –12 V with a fixed \( V_{BG} \) of 0 V. The inset shows the curves of the corresponding transconductance \( g_m \).](image2)

**Fig. 5.26** The top-gate characteristics for \( V_{TG} \) from +4 to –12 V with a fixed \( V_{BG} \) of 0 V. The inset shows the curves of the corresponding transconductance \( g_m \).
The drain current $I_D$ versus the drain voltage $V_D$ characteristics and gate characteristics of a transistor are shown in Fig. 5.25 to Fig. 5.28. In order to set a memory state of the channel conductance, different gate bias voltages $V_G$ of $-12$ V and $+12$ V were applied for 100ms prior to the measurements. Fig. 5.25 and 5.26 are the characteristics for different top gate voltages $V_G$. After applying $-12$ V and $+12$ V on the gate, the gate voltage $V_G$ was swept with a fixed $V_{BG}$ at 0 V. On the other hand, Fig. 5.27 and 5.28 show the measurements for different buried gate voltages $V_{BG}$. After a bias of $-12$ V or $+12$ V is applied on the gate, the buried gate voltage $V_{BG}$ is varied until it the channel is depleted.

![Fig. 5.27](image_url)  
**Fig. 5.27** Static drain current $I_D$ versus drain voltage $V_D$ characteristics with buried bottom-gate $V_{BG}$ sweep after different $V_{TG}$ of $+12$ and $-12$ V was applied on top.

![Fig. 5.28](image_url)  
**Fig. 5.28** The buried bottom gate characteristics for $V_{BG}$ from 0 to $-12$ V with a fixed $V_{TG}$ of 0 V. The inset shows the curves of the corresponding transconductance $g_m$. 


The top gate was biased at $V_G = 4 \text{ V}$, since that bias yields the largest difference between the two memory states. The results clearly demonstrate that the channel conductance of the transistor can be modulated with a maintained memory state set by the ferroelectric gate. Further depletion of the channel can be achieved by biasing either the ferroelectric gate on top $V_G$ or the backside junction gate $V_{BG}$.

Fig. 5.29 shows the drain current $I_D$ as a function of the retention time for different temperatures of 25 °C and 150 °C. A voltage pulse of $-12 \text{ V}$ or $+12 \text{ V}$ was initially applied for 100 ms, after which the gate voltage was kept at 0 V for the retention measurements. The retention was measured over an extended period of time. The high drain current state was found to be stable without serious change during $2 \times 10^4 \text{ s}$. The low drain current state more rapidly increases than the high current state does. However, it retains a state that can still be distinguished from the other state after the measured relaxation time.

This is attributed to a slow relaxation of the ferroelectric depolarisation. (There exists a “depolarization field” in the ferroelectric that reduces the ferroelectric polarization thereby decreasing the retention time.)

Nonvolatile ferroelectric field effect transistors has been demonstrated in semiconducting 4H silicon carbide. The low intrinsic carrier concentration of the wide-band gap silicon carbide allows high temperature stable operation of nonvolatile field effect transistor is with a retention time of more than 5 hours.

**Fig. 5.29** Retention properties of typical 4H-SiC ferroelectric field-effect transistor at 25 °C and 150 °C.
The main objective of the thesis work has been on the design, simulation, fabrication and characterization of field effect transistors in SiC to demonstrate the improved performance achievable using SiC. The project was focused on achieving a stable manufacturing process and on optimizing its performances by using numerical simulations and process development. Several different batches of devices have been successfully fabricated and the main achievements in the thesis by the author are described below:

**Process Technology Issues: Contacts and Oxides on ICP etched SiC**

It was demonstrated that by introducing a sacrificial oxidation step on the ICP-etched surface of SiC, the electrical properties could be effectively recovered for the Ohmic contacts and MOS capacitors on SiC.

For TiW Ohmic contacts, with etch damage caused by ICP, it has been found that the low-power (30 W) ICP-etching process did not affect the formation of ohmic contacts using the sacrificial oxidation. However, a medium platen power (60 W) etch gave damage that is hard to recover with sacrificial oxidation. AFM measurements have revealed that the specific contact resistance is highly related to the surface roughness.

Regarding the MOS structure, $C-V$ and $I-V$ measurements were performed and referenced to those of simultaneously prepared control samples without etch damage. The effective interface densities $N_{IT}$ and fixed oxide charges $Q_F$ of etch damaged samples have been found to increase while the breakdown field strength $E_{BD}$ of the oxide decreases. The barrier height $\phi_b$ at the SiC-SiO$_2$ interface, determined from a Fowler-Nordheim analysis, decreased for MOS capacitors on etch damaged surfaces. It has been found that a sacrificial oxidation treatment can improve the electrical characteristics of MOS capacitors on etch damaged SiC.
Design, fabrication, simulation and characterization SiC FETs

In this thesis several different FETs have been fabricated including buried-gate JFETs, JMOSFETs, and Ferroelectric FETs.

**JFETs**

Buried-gate JFET has its advantage in the relatively simple structure. In this work, two different structures of junction field-effect transistors in 4H-SiC, with and without trenching effect in the channel region, have been studied. The devices formed with a metal mask show a trenching profile after dry etching and exhibited static induction transistor (SIT)-like characteristics in the sub-threshold region of \( I-V \) curves as the channel thickness decreases. The devices without trenching effect have been processed by using a wet-etched oxide mask, resulting in a sloped dry-etch profile (\( \theta=30^\circ \)) in the channel, and consequently showed well-saturated drain characteristics for all the channel thicknesses. It has been shown that the trenching effect can induce SIT-like drain conduction for JFETs with small channel thickness, which can be improved for JFETs with sloped etch profile using an oxide mask for dry etching. The conduction mechanism in these JFETs was examined by analyzing the potential profiles from two-dimensional numerical simulations. 4H-SiC buried-gate JFETs have been fabricated using only 2- to 3-mask steps, depending on the etching profile. The switching performance of SiC BG JFETs in a test circuit with inductive load has been investigated and compared with numerical device simulations. During dynamic measurements, no significant difference has been observed between the different etching profile designs. The drain voltage rise/fall time of \(~30\) ns and \(25\) ns have been observed for turn-off and turn-on, respectively. The results have been compared to numerical mixed-mode circuit simulations with finite element structures. Further studies are required on the influence of the parasitic elements on the switching characteristics, which is expected to be improved with proper selection of the freewheeling diode and gate drive.

**JMOSFETs**

To improve the high temperature stability and the on-state resistance, we have designed a so-called JMOSFET, a novel combination of buried-gate JFET and MOSFET devices. The JMOSFETs have shown the feasibility for operating with constant on and off current levels from room temperature all the way up to \(300\) °C. Another advantage of this device is the improved channel mobility by accumulating the \(n\)-channel by MOS devices, which has been experimentally observed as well. Further optimization in terms of gate and source/drain contacts may be required for long term stability of this devices.

**FeFETs**

In realizing ferroelectric devices above room temperature and in severe environment, high temperature polarization behavior and retention of ferroelectric thin films are critical issues to be explored. SiC was shown to be a very attractive semiconductor material for these applications. In this work, we have examined different ferroelectric gate stacks on SiC and demonstrated working transistors at elevated temperature with non-volatile memory properties. We have found an optimum ferroelectric gate structure of PZT/Al\(_2\)O\(_3\)/4H-SiC diode structures: stable capacitance-voltage \(C-V\) loops with low conductance (<0.1 mS/cm\(^2\), tan \(\delta\) ~ 0.0007 at 400kHz) and memory window as wide as \(10\) V were obtained.
Based on this structure, different types of the metal-ferroelectric-silicon carbide FETs have been designed to operate in depletion or enhancement mode. The nonvolatile operation of ferroelectric-gate field-effect transistors in silicon carbide (SiC) has been shown at elevated temperatures. Depletion mode transistors were realized on $n$-type epitaxial channel layer and $p$-type substrates of 4H-SiC. Clear nonvolatile memory effect by the ferroelectric gate has been observed whereas the buried SiC $p$-$n$ junction gate independently controls the channel conductance without memory function. Memory windows as large as 5 V has been observed in drain current $I_D$ and ferroelectric gate voltage $V_G$ transfer characteristics. The transistor showed memory effect from room temperature up to 200 °C whereas stable transistor operation was observed up to 300 °C. The retention of nonvolatile properties was maintained after $2\times10^4$ seconds at 150 °C without applying bias on the gate. The low intrinsic carrier concentration of the wide-band gap silicon carbide allows for the high temperature stable operation of nonvolatile field effect transistor with retention of more than 5 hours.

**Future outlook**

The progress in SiC technology has resulted in research devices with highly promising performances being demonstrated. Despite several potentially advantageous markets for SiC electronics, the rate of commercialization has been rather slow and mostly limited by the material quality. While the material quality is still improving, there are still serious defect problems to overcome before large area devices can be economically viable. However, an encouraging fact is that development of the fabrication processes for SiC is at a relatively advanced stage and superior to most other wide bandgap semiconductors.

For example, JFETs and JMOSEFTs presented in this work do not have a very complicated structures but the improvement in the bulk and epitaxial growth as well as in ion-implantation may bring these SiC devices closer to the market besides the already-introduced MESFETs and Shottky diodes.

As shown in this thesis, the integration of ferroelectrics onto SiC presented is a unique work, which makes it interesting to study other ferroelectric materials and explore different properties such as piezoelectricity, pyroelectricity as well as ferroelectricity. These ferroelectric devices in SiC have potential applications for smart sensing and detecting devices operating at high temperature and in radiation-hard environment, or possibly even in high speed and with high power, depending on the design and process development.
References


References


