<http://www.diva-portal.org>

This is the published version of a paper published in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

Citation for the original published paper (version of record):

Colmenares, J., Sadik, D-P., Hilber, P., Nee, H-P. (2016)

Reliability Analysis of a High-Efficiency SiC Three-Phase Inverter.

IEEE Journal of Emerging and Selected Topics in Power Electronics, 4(3): 996-1006

<http://dx.doi.org/10.1109/JESTPE.2016.2551980>

Access to the published version may require subscription.

N.B. When citing this work, cite the original published paper.

Permanent link to this version:

<http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-192621>

Reliability Analysis of a High-Efficiency SiC Three-Phase Inverter

Juan Colmenares, *Student Member, IEEE*, Diane-Perle Sadik, *Student Member, IEEE*, Patrik Hilber, *Member, IEEE*, and Hans-Peter Nee, *Senior Member, IEEE*

Abstract—Silicon carbide as an emerging technology offers potential benefits compared with the currently used silicon. One of these advantages is higher efficiency. If this is targeted, reducing the on-state losses is a possibility to achieve it. Parallel-connecting devices decrease the on-state resistance and therefore reduce the losses. Furthermore, increasing the amount of components such as parallel connection of devices introduces an undesired tradeoff between efficiency and reliability, since an increased component count increases the probability of failure. A reliability analysis has been performed on a three-phase inverter rated at 312 kVA, using parallel-connected power modules. This analysis shows that the gate voltage stress has a high impact on the reliability of the complete system. Decreasing the positive gate-source voltage could, therefore, increase the reliability of the system approximately three times without affecting the efficiency significantly. Moreover, adding redundancy in the system could also increase the mean time to failure by approximately five times.

Index Terms—Inverter, Markov chain, motor drive application, power modules, reliability, silicon carbide (SiC), voltage source converter (VSC).

I. INTRODUCTION

SILICON carbide (SiC), as a wide bandgap material, offers three main potential benefits compared with the currently used silicon (Si). These benefits can be listed as higher efficiency, higher switching frequency, and higher temperature of operation [1]. The benefits of SiC technology have been identified in many applications, such as power factor correction [2], telecom [3], microgrids [4], wind power [5], high-voltage direct current transmission [6], modular multilevel converters [7], [8], inverters [9]–[11], automotive applications [12]–[14], solar power [16], and dc–dc converters [17], [18].

If high efficiency is targeted, the most important parameter that has to be controlled is the power losses. These power losses can be divided into mainly two components: 1) switching losses; and 2) conduction losses. In order to reduce the switching losses, it is important to ensure low-inductive gate

and commutation loops, permitting fast switching performance of the device. One possibility to reduce the conduction losses is either to connect discrete components in parallel [19]–[24] or to build power modules with several chips connected in parallel [24]–[27]. For the power module case, the so-called Miller effect may impair stable operation of the module [28]. In particular, this effect may cause cross-talk, which might induce accidental turn-ON and self-sustained oscillations. Different gate drive units have been proposed in order to solve this issue [29], [30]. Another possibility, which could result not only in reduction of the conduction losses, but also in a fast switching performance, is the parallel connection of lower current-rated power modules. This will result in low losses and higher power ratings. This has been proposed and tested in [31] and [32], where an efficiency higher than 99% has been reported in combination with a power rating higher than 300 kVA.

Nevertheless, increasing the amount of components, such as parallel connection of devices, has a negative impact on the reliability of the system. By introducing additional components, the probability of failure increases. Therefore, an undesired tradeoff between the high efficiency targeted and the reliability of the system is introduced. Several studies have been performed regarding the reliability performance of SiC devices. These studies have analyzed different modes of failure of the devices, such as short-circuit behavior and protection [33]–[37], long-term reliability [37]–[45], gate-oxide stability and threshold voltage instability [46]–[51], and high-temperature conditions [52]–[56].

However, these studies have been focused on the variation of the electrical internal parameters, such as the threshold voltage, of the devices. Therefore, it is the main focus of this work to analyze the reliability aspect of a SiC power electronic system using the information derived from reliability tests. An estimation of the life expectancy of a three-phase two-level voltage source converter (VSC) is performed. Additionally, important information about what parameters govern the reliability of the system is derived. Section II gives a description and experimental results of the system analyzed in this paper. In Section III, a reliability analysis is described and the results are discussed in Section IV. An analysis of the life expectancy regarding the gate voltage and number of power modules is also included in this section. Finally, the conclusions are drawn in Section V.

II. VOLTAGE SOURCE CONVERTER

The three-phase two-level VSC analyzed in this paper has a switching frequency of 20 kHz, an output current

Manuscript received December 10, 2015; revised February 18, 2016; accepted March 27, 2016. Date of publication April 7, 2016; date of current version July 29, 2016. Recommended for publication by Associate Editor Y. Xue.

J. Colmenares, D.-P. Sadik, and H.-P. Nee are with the Department of Electric Power and Energy Systems, KTH Royal Institute of Technology, Stockholm 100 44, Sweden (e-mail: juanco@kth.se; dianes@kth.se; hanssi@kth.se).

P. Hilber is with the Department of Electromagnetic Engineering, KTH Royal Institute of Technology, Stockholm 100 44, Sweden (e-mail: hilber@kth.se).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JESTPE.2016.2551980

Fig. 1. Photograph of the SiC power module.

Fig. 2. Photograph of the partially built VSC.

of 450 A rms, and a dc-link voltage of 650 V. Assuming a typical line-to-line output voltage of 400 V, the rated output power will be 312 kVA. It makes use of parallel-connection of power modules. This reduces the ON-state resistance, which will result in a reduction of the conduction losses. This is important when high efficiency is targeted. The power module used in this system is the Cree Inc. CAS100H12AM1 module (see Fig. 1). This is an all-SiC power module rated at 1200 V and 168 A. It has an ON-state resistance of 16 m Ω at room temperature (RT). Fig. 2 shows a photograph of the partially built VSC analyzed in this paper.

The requirements for high efficiency and current density are met when ten power modules are connected in parallel. This maintains the switching losses without a significant change, while reducing the conduction losses by a factor of ten. Moreover, distributed gate drive units per module will contribute in order to keep a certain switching performance. Additionally, a proper current density means that at rated load current, the current flowing through each of the power modules is sufficiently high to increase the junction temperature to the level where the ON-state resistance is well within the positive-temperature-coefficient range. Being in this range is an essential condition for the autobalancing mechanism of the current. This guarantees a uniform sharing of the current among the parallel-connected power modules. Moreover, an even number of power modules reduces the system complexity and is an important factor if a symmetrical placement is targeted [31].

A switching frequency of 20 kHz was chosen in order to reduce the size of the passive components, such as the dc-link capacitance. For this application, it was decided to use MKP capacitors (Metallized Polypropylene Film Capacitors), in particular MKP1848C66012JY5, which meet the

TABLE I
ELECTRICAL PARAMETERS OF THE THREE-PHASE INVERTER

Power Rating, S_n	312 kVA
Input Voltage	650 V DC
Output Line-to-Line Voltage	400 V RMS
Output Phase Current	450 A RMS
Switching Frequency, f_s	20 kHz
DC Capacitance, C	720 μ F
Blanking Time, T_D	600 ns

(a)

(b)

Fig. 3. Inverter waveforms during operation at nominal power of 207 kVA and switching frequency of (a) 4 and (b) 20 kHz.

requirement of voltage ratings and capacitance. Finally, a total dc capacitance of 720 μ F was found for the desired ripple of the dc-link voltage. Table I presents the electrical parameters of the VSC. A more detailed explanation of the methodology and construction process of this converter can be found in [32].

Fig. 3(a) and (b) shows the experimental results of the inverter operating at 4 and 20 kHz, respectively, supplying a motor drive. These results were obtained at more than 200 kVA. Symmetrical phase current with a motor drive as a load and closed-loop control are shown. The line-to-line voltage is also illustrated showing typical characteristics for pulsewidth modulation as expected. Table II shows the experimental results when driving an electrical machine while operating the inverter at an efficiency higher than 99%.

TABLE II
EXPERIMENTAL RESULTS OF THE THREE-PHASE INVERTER AT 20 kHz

Output Line-to-Line Voltage	397.88 V RMS
Output Phase Current	293.45 A RMS
Input Voltage	649.83 V dc
Input Current	153.44 A dc
Speed	2000 rpm
Torque	406.07 N/m
Efficiency, η	99.07 %

Fig. 4. (a) Photograph of the SiC power module. (b) Layout of the proposed VSC.

Furthermore, in order to perform a reliability analysis, it is important to extrapolate the mean time to failure (MTTF) from the accelerated tests of each component. It is important to note that the power module used to build the converter consists of parallel connection of single chips from the first generation of Cree devices. These components have evolved into a second generation and even a third where the reliability issues as well as performance have been investigated and improved [39]–[42]. Therefore, in this paper, the reliability calculations have been performed using the data from the second generation. A corresponding design, targeting high efficiency using parallel connection of power modules using the Cree Inc. CAS300M12BM2 [see Fig. 4(a)] power module rated at 1200 V and 300 A, with an ON-state resistance of 5 m Ω at RT, has been proposed for the calculations, as shown in Fig. 4(b). This power module is built using the parallel connection of six single-MOSFET chips and six antiparallel connections of diodes [57].

Using the information from the manufacturer available in [37] and [38] and considering the values for the rated application of the converter, Fig. 5 for the gate-source voltage (V_{GS}) stress of the MOSFETs, Fig. 6 for the drain-source voltage (V_{DS}) stress of the MOSFETs, and Fig. 7 for

Fig. 5. Extrapolated MTTF of 9.7×10^6 h at $V_{GS} = 20$ V. TDDb of gate oxide on 20 A for the Gen2 of SiC MOSFETs [38].

Fig. 6. Extrapolated MTTF of 6.5×10^7 h at $V_{DS} = 1000$ V. Accelerated field testing at 150 °C for the Gen2 of SiC MOSFETs [38].

Fig. 7. Extrapolated MTTF of 6×10^7 h at 175 °C for the SiC power diode [37].

the temperature stress of the diodes were plotted. The MTTF values have been derived for each failure mode in the case of the MOSFETs. Similarly, in [58], the MTTF value of the dc-link capacitor has been derived. Table III summarizes the MTTF (hours and years) and failure rate of the components at the rated condition, including the dc-link capacitors used for the construction of the inverter. It must be noted that the definition used for the failure rate is the reciprocal of the MTTF in years. Two failure modes have been identified, gate voltage stress and drain-source voltage stress.

The extrapolated values are related to the single chip. Therefore, a reliability calculation must be performed in order

TABLE III
MTTF AND FAILURE RATE OF THE COMPONENTS

Component	Rated Condition	MTTF [hours]	MTTF [years]	Failure Rate, λ
MOSFETs, V_{GS} Stress	20 V @ 150 °C	9.7×10^6	1.107×10^3	9.03×10^{-4}
MOSFETs, V_{DS} Stress	1000 V @ 150 °C	6.5×10^7	7.420×10^3	1.35×10^{-4}
Power Diode	175 °C	6×10^7	6.849×10^3	1.46×10^{-4}
DC-Link Capacitor	1000 V	10^8	1.142×10^5	8.76×10^{-5}

TABLE IV
MTTF AND FAILURE RATE OF THE SiC MOSFET POWER MODULE

Failure Mode	MTTF [years]	Failure Rate, λ
V_{GS} Stress	79.434	0.0126
V_{DS} Stress	296.80	0.0034

Fig. 8. Reliability block diagram for the SiC power module.

to obtain the MTTF and failure rate of the power module (see Table IV). This calculation basically consists of series connection of all the single chips used in order to build the power modules, as shown in Fig. 8. The failure rate for the power module considering both failure modes, the V_{GS} stress and the V_{DS} stress, was calculated using (1), where the subscript X represents each failure mode. Basically, in this scenario, all the failure rates, diode and MOSFETs, must be added for each failure mode (gate voltage stress and drain-source voltage stress). This is mainly due to the fact that all the chips must be on the safe state such that the module can operate properly. Accordingly

$$\lambda_{\text{Module}_X} = \sum_{i=1}^{12} \lambda_{\text{Diode}_i} + \sum_{i=1}^{12} \lambda_{\text{MOSFET}_{iX}}. \quad (1)$$

III. RELIABILITY ANALYSIS

In this paper, as shown in Tables III and IV, two failure modes have been analyzed. These are: 1) V_{DS} stress and 2) V_{GS} stress. Moreover, two cases of analysis have been performed. The first is a case of no redundancy; on the other hand, the second case takes advantage of the parallel connection of power modules and introduces the so-called *active redundancy*.

A. No Redundancy

When no redundancy is considered, all the components of the system are connected in series for the reliability analysis

Fig. 9. Reliability block diagram for the high-efficiency SiC three-phase inverter without redundancy.

TABLE V
MTTF AND FAILURE RATE OF THE HIGH-EFFICIENCY SiC THREE-PHASE INVERTER WITHOUT REDUNDANCY

Failure Mode	MTTF [years]	Failure Rate, λ
V_{GS} Stress	6.57	0.1521
V_{DS} Stress	24.11	0.0415

as shown in Fig. 9. This means that all the components must be working properly to consider that the system is working. Table V shows the calculated MTTF, using (2), for each failure mode as well as the failure rate for the rated condition shown in Table I. It is possible to note that the life expectancy is dominated by the gate voltage stress, and it is approximately 6.57 years

$$\lambda_{\text{Inv}_X} = \sum_{i=1}^{12} \lambda_{\text{Cap}_i} + \sum_{i=1}^{12} \lambda_{\text{Module}_{iX}}. \quad (2)$$

B. Active Redundancy

When active redundancy is targeted, two possible scenarios could be considered. In the first case, no additional modules are considered for each phase leg, and the VSC has the same amount modules as in the no-redundancy case. On the other hand, also a second case is studied, where additional power modules are included in the design, permitting the inverter to continue operation at an efficiency higher than 99%. In order to achieve the targeted redundancy, additional components should be included in the switching loop, such as disconnectors. These components will add parasitic inductances that modify the switching performance and consequently the efficiency of the system. However, in this investigation, all these additional components are considered to be more reliable than the power modules and capacitors. Disconnectors such as the one described in [59] could be used in order to physically disconnect the power module (see Fig. 10). This will allow the remaining electrical power modules continue their operation. Traditionally, if a power module fails, the removal or replacement of the respective power modules is a complicated procedure that requires the inverter to stop its operation, therefore, increasing the down time of the VSC. The described disconnector in [59] is based on the idea that disconnecting a failed power module can be realized automatically by means of a remote controllable trigger signal. This automatic disconnection can be realized within a short time period.

1) *No Additional Power Modules*: For this case of active redundancy, the VSC required only half, i.e., two power modules per phase in order to operate at the rated conditions (see Fig. 11). However, in this case, the inverter efficiency will

Fig. 10. Schematic of the power module disconnecter proposed in [59]. (a) Power module disconnected. (b) Power module connected.

Fig. 11. Reliability block diagram for the high-efficiency SiC three-phase inverter with active redundancy and no additional power modules.

Fig. 12. Reliability block diagram for one phase of the high-efficiency SiC three-phase inverter with active redundancy.

drop to 98.7%, lower than the targeted 99% [31], [32]. In order to calculate the MTTF of the system, several calculations must be performed, considering the fact that the failure rate is not constant. For redundant systems, a higher reliability is expected for shorter mission times. Therefore, a failure rate dependent on time is expected. For each phase of the inverter, four different states are considered. These states are: 1) fully functional (all power modules working); 2) one failed (one power module failed); 3) two failed (two power modules failed); and 4) phase failed (more than two power modules failed).

Finally, the failure rate for each state must be calculated using the methodology for series and parallel system. For instance, for the first state 1), Fig. 12 shows the equivalent

Fig. 13. Markov diagram for one phase of the high-efficiency SiC three-phase inverter with active redundancy and no additional power modules.

system of a single phase, and using

$$\lambda_{\text{Phase}_x} = \frac{2\lambda_{\text{Module}_x}}{\sum_{i=1}^6 \frac{1}{i}} \quad (3)$$

the failure rate was calculated. Similarly, calculations were performed for each of the other states.

Consequently, by applying a Markov chain analysis, it is possible to introduce the several states of the system described above. This method made possible to calculate the probability of the system to be in this predefined states. These probabilities are calculated from the transition rates between the states, which in this case are the failure rates [60], [61].

Fig. 13 shows the transition between the considered states. The probabilities of failure with respect to the mission time were calculated for each state of the system and for each failure mode as seen in Fig. 14(a) and (b). From these probabilities, the failure rate of the phases could be calculated. The three phases are connected in series from the reliability perspective. Therefore, the failure rate of the system could be calculated as well as the probability density function, which contains the MTTF [see Fig. 14(c) and (d)]. It must be noted that the plots for V_{DS} stress and V_{GS} stress are extended to 400 and 100 years, respectively, in order to illustrate how the failure rate changes regarding the mission times. It must be noted how the probability of the system to fail increase with time as expected. The probability of the system to be in the first state, where all power modules are properly operating, rapidly falls with time. Furthermore, the failure rate of the system also increases with time and is not constant as in the no-redundancy case. Finally, active redundancy with no additional power modules increases the MTTF several times, approximately 34.38 years, as shown in Table VI.

2) *Additional Power Modules*: For this case of active redundancy, two additional power modules per phase are considered in the analysis; the VSC required four power modules per phase in order to operate at the rated conditions and efficiency (see Fig. 15). Furthermore, it is chosen to have two additional power modules in order to keep the symmetrical placement of the modules, which contributes to the proper current sharing between the modules. This current sharing is dependent of the parasitic elements such as the stray inductance in the bus bar.

In order to calculate the MTTF of the system, a similar methodology as in the previous case for redundant systems

Fig. 14. Probability of each state of Markov models and probability of system failure regarding the mission time for (a) gate-source voltage stress and (b) drain-source voltage stress. Failure rate and probability density function regarding the mission time for (c) gate-source voltage stress and (d) drain-source voltage stress.

is applied where a higher reliability for shorter mission times and failure rate dependent of time are expected. For each phase of the inverter, the same four different states are considered.

TABLE VI
MTTF AND FAILURE RATE OF THE HIGH-EFFICIENCY SiC
THREE-PHASE INVERTER WITH ACTIVE REDUNDANCY

Failure Mode	MTTF [years]
V_{GS} Stress	34.38
V_{DS} Stress	133.34

Fig. 15. Reliability block diagram for the high-efficiency SiC three-phase inverter with active redundancy with additional power modules.

TABLE VII
MTTF AND FAILURE RATE OF THE HIGH-EFFICIENCY SiC
THREE-PHASE INVERTER WITH ACTIVE REDUNDANCY

Failure Mode	MTTF [years]
V_{GS} Stress	18.56
V_{DS} Stress	70.95

These states are: 1) fully functional (all power modules working); 2) one failed (one power module failed); 3) two failed (two power modules failed); and 4) phase failed (more than two power modules failed). It is considered a failure of the system when three or more modules fail. This is mainly due to the fact that operating with four modules or less, the inverter is not able to keep the efficiency higher than 99%. Finally, the failure rate for each state must be calculated using the methodology for series and parallel system, as in the previous case. For instance, the failure rate of the first state 1) is calculated using the following. Similarly, the failure rate for each state has been calculated. Thus

$$\lambda_{\text{Phase}_X} = \frac{4\lambda_{\text{Module}_X}}{\sum_{i=1}^{15} \frac{1}{i}}. \quad (4)$$

Consequently, applying a Markov chain analysis and considering the three phases are connected in series from the reliability perspective as in the previous case. The failure of the system could be calculated as well as the probability density function. Finally, active redundancy with additional power modules also increases the MTTF several times, approximately 18.56 years, as shown in Table VII.

IV. DISCUSSION

As shown in the previous section, the gate-source voltage stress determines the life expectancy of the system. A more detailed description on how the MTTF varies regarding the gate voltage is shown in Fig. 16. Higher life expectancy is obtained by reducing V_{GS} . However, if active redundancy is included, a similar value of life expectancy could be achieved

Fig. 16. MTTF as function of gate voltage, no-redundancy (blue dashed line), and active redundancy (green solid line).

as in the case when V_{GS} is reduced, without reducing the gate voltage. Moreover, the failure rate of the diode, derived from the manufacturer data [37], has more influence at lower gate voltages where the failure rates of the MOSFETs are lower, than at higher gate voltages where the failure rates of the MOSFETs are greater.

Furthermore, reducing the gate-source voltage impacts on different parameters of the system such as the ON-state resistance and the switching speeds, thus affecting the total losses of the system. Using a simulation model of the power module, it is possible to estimate how these losses depend on the gate voltage. The simulation model of the investigated power module (CAS300M12BM2) was developed using ANSYS Simplorer and Q3D. Finally, the power module was simulated with LTSPICE including the parasitic elements derived from ANSYS [58]. Fig. 17(a) and (c) shows the experimental results and the simulation results, respectively, for the turn-ON transitions. Similarly, Fig. 17(b) and (d) shows the results for the turn-OFF transition. It can be noted that the simulation results fit the experimental results appropriately. Therefore, an estimation of how the total losses change regarding V_{GS} could be performed.

Using the developed simulation model, the transient performance at different gate voltages were analyzed and plotted in Fig. 18. It is possible to estimate how the switching losses as well as the conduction losses vary depending on the gate voltage. As expected, the lower V_{GS} , the higher the losses.

Therefore, reducing the gate voltage will affect the efficiency of the system as shown in Fig. 19. By decreasing the positive gate-source voltage by 3 V, the reliability of the system is increased approximately four times (solid line in Fig. 19) and the efficiency is reduced by approximately 0.1%. Nevertheless, the reduction of the efficiency is not significant compared with the MTTF improvement.

Moreover, decreasing the gate voltage will increase the losses of the system and, therefore, the junction temperature of the SiC chip will rise. One possibility so as to maintain the validity of this study is to recalculate the cooling system, such as the cooling block, in order to keep the junction temperature at 150 °C. However, this might lead to a more bulky system. On the other hand, if the temperature variation is considered

Fig. 17. (a) Turn-ON and (b) turn-OFF switching waveforms of the power module. Measured drain-source voltage of the SiC MOSFET (purple curve, 200 V/div), drain-source current of the SiC MOSFET (pink curve, 100 A/div), and gate-source voltage of the SiC MOSFET (yellow curve, 20 V/div) (time-base 50 ns/div). (c) Turn-ON and (d) turn-OFF transients of the simulated SiC MOSFET power module, drain-source voltage of the SiC MOSFET (blue curve, 100 V/div), and drain-source current of the SiC MOSFET (green curve, 50 A/div).

into the analysis, the MTTF will get affected as well. Using the so-called Arrhenius relation, the acceleration factor could be calculated with respect to the reference point at 150 °C.

Fig. 18. Conduction losses (blue line), switching losses (green line), and total losses (red line) regarding gate voltage.

Assuming water-cooling with a proper water flow rate in order to guarantee a turbulent flow, the junction temperature for each gate voltage can be calculated as

$$T_{Ji} = \frac{P_i}{P_{\text{Test}}} (T_{J\text{Test}} - T_w) + T_w \quad (5)$$

where

$$P_{\text{Test}} = Ah(T_{J\text{Test}} - T_w) \quad (6)$$

and

$$P_i = Ah(T_{Ji} - T_w) \quad (7)$$

where T_w is the average temperature of the cooling water between the input and output, $T_{J\text{Test}}$ is the junction temperature at the reference point, T_{Ji} is the junction temperature at each gate voltage, P_{Test} is the losses at the reference point, P_i is the losses at each gate voltage, A is the total area for heat dissipation, and h is the heat transfer coefficient.

Using Arrhenius relation [62], the acceleration factor which results from operating a device at an elevated temperature

$$A_F = e^{\frac{E_a}{k} \left(\frac{1}{T_{\text{Test}}} - \frac{1}{T_{Ji}} \right)} \quad (8)$$

is calculated, where k is the Boltzmann constant, T_{Test} is the junction temperature at the reference point, and E_a is the activation energy required to initiate a specific type of failure mode.

Finally, the new MTTF considering the temperature variations is calculated from

$$\text{MTTF} = \frac{1}{\lambda A_F} \quad (9)$$

Fig. 19 shows the modified MTFF (dashed line) with respect to the gate voltage.

It must be noted that decreasing the gate voltage could also lead to a lower reliability due to the high temperature of the junction. By decreasing the gate voltage, the power losses raise and therefore the junction temperature as well. This has a negative impact on the total reliability of the system. In this case, by decreasing the gate voltage 3 V, the MTTF increases approximately 2.5 times and the efficiency is reduced by approximately 0.1%.

Fig. 19. MTTF (blue line) and efficiency (green line) regarding gate voltage.

Fig. 20. MTTF (blue line) and efficiency (green line) regarding number of power modules per phase.

As described in Section I, parallel connecting devices will increase the amount of components and this has a negative impact on the reliability performance of the system. By introducing additional components, the probability of failure is increased. Therefore, an undesired tradeoff between the high efficiency targeted and the reliability of the system is introduced. Fig. 20 shows how the MTTF varies with respect to the amount of modules per phase. By having more modules connected in parallel, the conduction losses drop, and therefore, the efficiency increases. However, the MTTF decreases as the number of power modules increases.

Nevertheless, several assumptions have been made in order to perform the reliability study. First, when active redundancy is introduced, this implies that the power modules that fail during operation are disconnected. As soon as this occurs, the remaining power modules will conduct higher current in order to maintain the rated output power. By conducting higher current, the device temperature will increase affecting the reliability of the system. Nevertheless, the reliability calculations have been done using the extrapolated values at 150 °C, i.e., that the performed study is a worst case analysis. Also, during the blanking time, part of the current flows through the intrinsic body diodes of the MOSFETs. Several studies have been dealing with the reliability of the body diode [41]–[43]. These studies show a stable body diode performance under a 1000-h dc body diode stress of 22 A.

Additionally, the negative gate-source voltage, used in many applications, might apply more stress and therefore influences

the reliability of the complete system. Several studies have been performed already regarding this aspect [42]–[44]. These studies show stable threshold voltages for $V_{GS} = -15$ V of stress for 1000 h at 150 °C. The average threshold voltage shift for the devices under this stress was approximately -50 mV. However, it is the hypothesis of the authors that the use of the body diode of the device as well as the negative bias stress might impact the reliability of the system and could influence the life of the inverter. Therefore, this must be investigated in order to determine the failure rate and MTTF with respect to these conditions.

Moreover, the packaging itself could be the factor that determines the reliability of the system. However, for the power module analyzed in this paper, the package is similar to the one used for silicon Isolated Gate Bipolar Transistor (IGBT) power modules, which has been proved for several applications under different reliability standards. The reliability issues introduced due to the packaging will be the same as in the Si counterpart, and there will not be major differences between the two semiconductor cases. Therefore, the reliability issues from the packaging point of view do not have a major contribution in the analysis. The focus of this work is on the reliability aspects from the semiconductor point of view.

Finally, different strategies could be used so as to increase the reliability of a system, such as reducing the temperature. In order to do this, a lower current must flow through the power modules, i.e., more devices connected in parallel, which will not necessarily increase the reliability of the system. Instead, adding additional components might have a negative effect on the operating life of the system. Another possibility is to decrease the voltage level, which could also increase the reliability of the system. However, in this case, an additional transformer is needed so as to satisfy the rated conditions of the system. Nevertheless, the drain-source voltage stress does not determine the reliability of the system. Finally, higher quality components, i.e., better SiC chips, will also increase the final reliability.

V. CONCLUSION

A possible solution for higher efficiencies using SiC has been presented, using parallel connection of power modules. The experimental results of the proposed VSC driving a motor verify an efficiency exceeding 99%. A reliability analysis has been performed on a 312-kVA VSC. Parallel-connecting devices will increase the amount of components and this has a negative impact on the reliability performance of the system. By having additional power modules connected in parallel, the conduction losses drop and, therefore, the efficiency increases. However, the MTTF decreases as the number of power modules increases. Two different failure modes have been studied, the V_{GS} stress and the V_{DS} stress. Additionally, two possible cases were analyzed: 1) no redundancy and 2) active redundancy. This analysis has shown that the gate-source voltage stress determines the reliability and MTTF of the complete system. Nevertheless, decreasing the positive gate-source voltage could increase the reliability of the system approximately 2.5–4 times without affecting the efficiency significantly. Moreover, adding redundancy to

the system could also increase the MTTF by approximately three to five times. Finally, an undesired tradeoff between the high efficiency targeted and the reliability of the system is introduced. By having more modules connected in parallel, the conduction losses drop and therefore, the efficiency rises. However, the MTTF decreases as the number of power modules increases.

REFERENCES

- [1] J. Rabkowski, D. Pefitis, and H. P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.
- [2] R. L. Kelley *et al.*, "Power factor correction using an enhancement-mode SiC JFET," in *Proc. IEEE Power Electron. Specialists Conf. (PESC)*, Jun. 2008, pp. 4766–4769.
- [3] D. Aggeler, J. Biela, and J. W. Kolar, "Controllable dv/dt behaviour of the SiC MOSFET/JFET cascode an alternative hard commutated switch for telecom applications," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2010, pp. 1584–1590.
- [4] Q. Zhang, R. Callanan, M. K. Das, S.-H. Ryu, A. K. Agarwal, and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.
- [5] H. Zhang and L. M. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan. 2011.
- [6] M. Chinthavali, L. M. Tolbert, and B. Ozpineci, "SiC GTO thyristor model for HVDC interface," in *Proc. IEEE Power Eng. Soc. General Meeting*, vol. 1, Jun. 2004, pp. 680–685.
- [7] D. Pefitis *et al.*, "High-power modular multilevel converters with SiC JFETs," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 28–36, Jan. 2012.
- [8] H. Mirzaee, A. De, A. Tripathi, and S. Bhattacharya, "Design comparison of high-power medium-voltage converters based on a 6.5-kV Si-IGBT/Si-PiN diode, a 6.5-kV Si-IGBT/SiC-JBS diode, and a 10-kV SiC-MOSFET/SiC-JBS diode," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2728–2740, Jul./Aug. 2014.
- [9] J. Rabkowski, D. Pefitis, and H.-P. Nee, "Design steps toward a 40-kVA SiC JFET inverter with natural-convection cooling and an efficiency exceeding 99.5%," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1589–1598, Jul. 2013.
- [10] S. Round, M. Heldwein, J. Kolar, I. Hofsjager, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Proc. Conf. Rec. 14th IAS Annu. Meeting*, vol. 1, Oct. 2005, pp. 410–416.
- [11] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An all-SiC three-phase buck rectifier for high-efficiency data center power supplies," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2662–2673, Nov./Dec. 2013.
- [12] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 912–921, Mar./Apr. 2011.
- [13] B. Wrzecionko, J. Biela, and J. W. Kolar, "SiC power semiconductors in HEVs: Influence of junction temperature on power density, chip utilization and efficiency," in *Proc. 35th Annu. Conf. IEEE Ind. Electron. (IECON)*, Nov. 2009, pp. 3834–3841.
- [14] T. Evans, T. Hanada, Y. Nakano, and T. Nakamura, "Development of SiC power devices and modules for automotive motor drive use," in *Proc. IEEE Int. Meeting Future Electron Devices, Kansai (IMFEDK)*, Jun. 2013, pp. 116–117.
- [15] B. Wrzecionko, D. Bortis, and J. W. Kolar, "A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2345–2358, May 2014.
- [16] Y. Hinata, M. Horio, Y. Ikeda, R. Yamada, and Y. Takahashi, "Full SiC power module with advanced structure and its solar inverter application," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 604–607.
- [17] H. Akagi, T. Yamagishi, N. M. L. Tan, S. I. Kinouchi, Y. Miyazaki, and M. Koyama, "Power-loss breakdown of a 750-V, 100-kW, 20-kHz bidirectional isolated DC-DC converter using SiC-MOSFET/SBD dual modules," in *Proc. Int. Power Electron. Conf. (IPEC)*, May 2014, pp. 750–757.

- [18] G. Tolstoy *et al.*, "An experimental analysis on how the dead-time of SiC BJT and SiC MOSFET impacts the losses in a high-frequency resonant converter," in *Proc. 16th Eur. Conf. Power Electron. Appl. (EPE)*, Aug. 2014, pp. 1–10.
- [19] M. Chinthavali, P. Ning, Y. Cui, and L. M. Tolbert, "Investigation on the parallel operation of discrete SiC BJTs and JFETs," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2011, pp. 1076–1083.
- [20] D. Pefitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy, and H.-P. Nee, "Challenges regarding parallel connection of SiC JFETs," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1449–1463, Mar. 2013.
- [21] J. Rabkowski, D. Pefitsis, and H.-P. Nee, "Parallel-operation of discrete SiC BJTs in a 6-kW/250-kHz DC/DC boost converter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2482–2491, May 2014.
- [22] D.-P. Sadik, J. Colmenares, D. Pefitsis, J.-K. Lim, J. Rabkowski, and H.-P. Nee, "Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, 2013, pp. 1–10.
- [23] R. Fu, A. Grekov, J. Hudgins, A. Mantooth, and E. Santi, "Power SiC DMOSFET model accounting for nonuniform current distribution in JFET region," *IEEE Trans. Ind. Appl.*, vol. 48, no. 1, pp. 181–190, Jan./Feb. 2012.
- [24] J. K. Lim, D. Pefitsis, J. Rabkowski, M. Bakowski, and H. P. Nee, "Modeling of the impact of parameter spread on the switching performance of parallel-connected SiC VJFETs," in *Mater. Sci. Forum*, vols. 740–742, pp. 1098–1102, 2013.
- [25] J. B. Casady, "SiC power devices and modules maturing rapidly," *Power Electron. Eur.*, vol. 1, no. 1, pp. 16–19, Jan. 2013.
- [26] A. Dutta, S. Wang, J. Zhou, S. S. Ang, J.-C. Chang, and C.-S. Chen, "The design and fabrication of a 50 KVA 450 A silicon carbide power electronic module," in *Proc. 4th IEEE Int. Symp. Power Electron. Distrib. Generat. Syst. (PEDG)*, Jul. 2013, pp. 1–5.
- [27] P. Ning, F. Wang, and D. Zhang, "A high density 250 °C junction temperature SiC power module development," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 415–424, Sep. 2014.
- [28] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, Oct. 2013.
- [29] J. Colmenares, D. Pefitsis, J. Rabkowski, D.-P. Sadik, and H.-P. Nee, "Dual-function gate driver for a power module with SiC junction field-effect transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2367–2379, May 2014.
- [30] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
- [31] J. Colmenares, D. Pefitsis, J. Rabkowski, and H.-P. Nee, "Switching performance of parallel-connected power modules with SiC MOSFETs," in *Proc. Int. Power Electron. Conf. (IPEC)*, May 2014, pp. 3712–3717.
- [32] J. Colmenares, D. Pefitsis, D.-P. Sadik, G. Tolstoy, J. Rabkowski, and H.-P. Nee, "High-efficiency 312-kVA three-phase inverter using parallel connection of silicon carbide MOSFET power modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 4664–4676, Nov./Dec. 2015.
- [33] X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. J. Baliga, "Short-circuit capability of 1200 V SiC MOSFET and JFET for fault protection," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 197–200.
- [34] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikiara, "Short-circuit tests on SiC power MOSFETs," in *Proc. IEEE 10th Int. Conf. Power Electron. Drive Syst. (PEDS)*, Apr. 2013, pp. 1297–1300.
- [35] D.-P. Sadik *et al.*, "Short-circuit protection circuits for silicon-carbide power transistors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, Apr. 2016.
- [36] J. A. Schrock *et al.*, "High-mobility stable 1200-V, 150-A 4H-SiC DMOSFET long-term reliability analysis under high current density transient conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2891–2895, Jun. 2015.
- [37] A. Ward. (Mar. 2006). *SiC Power Diode Reliability*. [Online]. Available: <http://www.prochip.ru/cms/f/325747.pdf>
- [38] S. Allen. (Mar. 2013). *Silicon Carbide MOSFETs for High Powered Modules*. [Online]. Available: <http://www.psm-a.com/sites/default/files/uploads/tech-forumpackaging/presentations/2013-apec-111-silicon-carbide-mosfets-high-powermodules.pdf>
- [39] D. A. Gajewski, S. H. Ryu, M. Das, B. Hull, J. Young, and J. W. Palmour, "Reliability performance of 1200 V and 1700 V 4H-SiC DMOSFETs for next generation power conversion applications," *Mater. Sci. Forum*, vols. 778–780, pp. 967–970, Feb. 2014.
- [40] R. A. Wood and T. E. Salem, "Long-term operation and reliability study of a 1200-V, 880-A all-SiC dual module," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion (SPEEDAM)*, Jun. 2012, pp. 1520–1525.
- [41] A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, "A new degradation mechanism in high-voltage SiC power MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 587–589, Jul. 2007.
- [42] B. Hull *et al.*, "Reliability and stability of SiC power MOSFETs and next-generation SiC MOSFETs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2014, pp. 139–142.
- [43] D.-P. Sadik, J.-K. Lim, P. Ranstad, and H.-P. Nee, "Investigation of long-term parameter variations of SiC power MOSFETs," in *Proc. 17th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2015, pp. 1–10.
- [44] R. Green, A. Lelis, and D. Habersat, "Application of reliability test standards to SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2011, pp. EX.2.1–EX.2.9.
- [45] T. Ueda, "Reliability issues in GaN and SiC power devices," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Jun. 2014, pp. 3D.4.1–3D.4.6.
- [46] T.-T. Nguyen, A. Ahmed, T. V. Thang, and J.-H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.
- [47] M. A. Anders, P. M. Lenahan, and A. J. Lelis, "Negative bias instability in 4H-SiC MOSFETs: Evidence for structural changes in the SiC," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2015, pp. 3E.4.1–3E.4.5.
- [48] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.
- [49] T. Santini, M. Sebastien, M. Florent, L.-V. Phung, and B. Allard, "Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications," in *Proc. IEEE ECCE Asia Downunder (ECCE Asia)*, Jun. 2013, pp. 385–391.
- [50] A. J. Lelis *et al.*, "Time dependence of bias-stress-induced SiC MOSFET threshold-voltage instability measurements," *IEEE Trans. Electron. Devices*, vol. 55, no. 8, pp. 1835–1840, Aug. 2008.
- [51] A. J. Lelis, R. Green, D. Habersat, and N. Goldsman, "Effect of threshold-voltage instability on SiC DMOSFET reliability," in *Proc. IEEE Int. Integr. Rel. Workshop*, Oct. 2008, pp. 72–76.
- [52] L. A. Lipkin and J. W. Palmour, "Insulator investigation on SiC for improved reliability," *IEEE Trans. Electron. Devices*, vol. 46, no. 3, pp. 525–532, Mar. 1999.
- [53] D. Watt. (2012). *Cree SiC Diodes High Temperature Reliability Trials*. [Online]. Available: <http://products.sem-elabtt.com/pdf/diode/siliconcarbide/SiCDiodesReliabilityStudy.pdf>
- [54] S. Tanimoto and H. Ohashi, "Reliability issues of SiC power MOSFETs toward high junction temperature operation," *Phys. Status Solidi A*, vol. 206, no. 10, pp. 2417–2430, 2009.
- [55] T. Thomas, K.-F. Becker, T. Braun, M. van Dijk, O. Wittler, and K.-D. Lang, "Assessment of high temperature reliability of molded smart power modules," in *Proc. Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Sep. 2014, pp. 1–7.
- [56] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of SiC MOSFETs: A technology for high-temperature environments," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Dec. 2010.
- [57] D.-P. Sadik, K. Kostov, J. Colmenares, and H.-P. Nee, "Analysis of parasitic elements of silicon carbide power modules with special emphasis on reliability issues," in *Proc. 31st IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2016, paper T-21-1018.
- [58] V. Roederstein, *Metallized Polypropylene Film Capacitor DC-Link Capacitor*, document MKP1848C DC-Link, Sep. 2015.
- [59] T. S. Thomsen, "Automated mechanical disconnection of an electrical converter module in a frequency converter arrangement," U.S. Patent 8 564 963, Oct. 22, 2013.
- [60] M. Rausand and A. Høyland, *System Reliability Theory: Models, Statistical Methods, and Applications*. New York, NY, USA: Wiley, 2004.

- [61] Y. A. Rozanov, *Introductory Probability Theory*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1969.
- [62] K. J. Laidler, "The development of the Arrhenius equation," *J. Chem. Edu.*, vol. 61, no. 6, pp. 494–498, 1984.

Juan Colmenares (S'12) was born in Maracaibo, Venezuela, in 1989. He received the Diploma degree in electronics engineering from Universidad Simon Bolivar, Caracas, Venezuela, in 2012. He is currently pursuing the Ph.D. degree with the Department of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden.

His current research interests include gate-driver design for SiC power modules and SiC power converters.

Diane-Perle Sadik (S'12) was born in Lausanne, Switzerland, in 1988. She received the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology in Lausanne, Lausanne, in 2012. She is currently pursuing the Ph.D. degree with the Department of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden.

Her current research interests include converters with SiC devices, protection circuits for SiC devices, and reliability analysis of SiC MOSFETs.

Patrik Hilber (S'02–M'08) was born in Stockholm, Sweden, in 1975. He received the M.Sc. degree in systems engineering and the Lic.Tech. and Ph.D. degrees in electric power systems from the KTH Royal Institute of Technology, Stockholm, in 2000, 2005, and 2008, respectively.

He has been a Research Leader with the RCAM Group, Department of Electromagnetic Engineering, KTH Royal Institute of Technology, since 2008. He is currently the Deputy Director with the Swedish Centre for Smart Grids and Energy Storage, Stockholm. In 2014, he was appointed as an Associate Professor (docent) with the School of Electrical Engineering, KTH Royal Institute of Technology. In 2014, he Co-Founded H2L Grid Solutions AB, Stockholm, a research spin-off company from the KTH Royal Institute of Technology. He is also involved in a number of boards, including two educations. His current research interests include maintenance optimization, reliability modeling of power systems, and probabilistic models for age and maintenance.

Hans-Peter Nee (S'91–M'96–SM'04) was born in Västerås, Sweden, in 1963. He received the M.Sc., Licentiate, and Ph.D. degrees from the KTH Royal Institute of Technology, Stockholm, Sweden, in 1987, 1992, and 1996, respectively, all in electrical engineering.

He became a Professor of Power Electronics with the KTH Royal Institute of Technology in 1999, where he is currently the Head of the Electrical Energy Conversion Laboratory. His current research interests include power electronic converters, semiconductor components, and control aspects of utility applications, such as flexible ac transmission systems and high-voltage dc transmissions, and variable-speed drives.

Dr. Nee was a recipient of several awards for his research. He is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. He was on the Board of the IEEE Sweden Section for several years, and served as its Chairman from 2002 to 2003. He is a member of the European Power Electronics and Drives Association, involved with the Executive Council and the International Scientific Committee.