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Flying Capacitor Hybrid Modular Multilevel Converter with Thyristor Director Valves

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Abstract

This thesis focuses on the field of HVDC transmission systems, specifically exploring the modular multilevel converter (MMC) topology. A new variation, the Flying Capacitor Hybrid Modular Multilevel Converter (FC-HMMC), is proposed. While the original topology utilizes IGBT devices, these components are prone to fail due to high voltage and current during turn-on, leading to latch-up or avalanche breakdown. In contrast, thyristors typically short due to physical or electrical abuse, with very few failing open. However, integrating thyristors into the FC-HMMC topology presents new challenges that require a thorough investigation into the commutation process. The significance of this work lies in its contribution to analyzing and proposing solutions to the problems. The project involves building a detailed simulation model of the FC-HMMC from the ground up using PSCAD, analyzing its operating principles, and proposing a modified control algorithm to enable the replacement of IGBTs with thyristors. The proposed method is implemented and validated through simulation, with results demonstrating its effectiveness. This work provides new insights into converter design and control, paving the way for future research and practical applications in high-voltage power electronics.

Keywords

Flying Capacitor, High-Voltage Direct Current, Hybrid Modular Multilevel Converter, IGBT and Thyristor, PSCAD Simulation

Sammanfattning

Denna masteruppsats fokuserar på området för HVDC-transmissionssystem, med särskild inriktning på topologin för modulära multinivåomriktare (MMC). En ny variation, den flygande kondensator hybrida modulära multinivåomriktaren (FC-HMMC), föreslås. Den ursprungliga topologin använder IGBT-komponenter, vilka är benägna att gå sönder vid höga spänningar och strömmar under påslagning, vilket kan leda till latch-up eller lavinartad nedbrytning. Å andra sidan kortsluts tyristorer vanligtvis på grund av fysisk eller elektrisk överbelastning, medan många får gå sönder med öppen krets. Att integrera tyristorer i FC-HMMC-topologin medför dock nya utmaningar som kräver en noggrann undersökning av kommuteringsprocessen. Betydelsen av detta arbete ligger i dess bidrag till att analysera och föreslå lösningar på dessa problem. Projektet innefattar att bygga en detaljerad simuleringsmodell av FC-HMMC från grunden i PSCAD, analysera dess funktionsprinciper och föreslå en modifierad styralgorithm för att möjliggöra ersättning av IGBT:er med tyristorer. Den föreslagna metoden implementeras och valideras genom simulering, med resultat som visar dess effektivitet. Detta arbete ger nya insikter i omriktardesign och styrning, och banar väg för framtida forskning och praktiska tillämpningar inom högspänd kraftelektronik.

Nyckelord

Flygande Kondensator, Högeffektiv Likströmsöverföring(HVDC), Hybrid Modulär Multinivåomriktare (HMMC), IGBT och Tyristor, PSCAD-simulering.

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Chapter 1

Introduction

In this thesis, the Flying Capacitor Hybrid Multilevel Modular Converter (FC-HMMC) is investigated in detail. The study presents a comprehensive analysis of the converter's operating principles, supported by circuit modeling and closed-loop control implementation using simulation software. A novel approach involving the replacement of conventional switching devices with thyristors is proposed, and the feasibility of the proposed modifications is evaluated through simulation, and the results are thoroughly analyzed to validate the converter's performance.

1.1 Background

The Modular Multilevel Converter (MMC) in Figure 1.1 has emerged as one of the most widely adopted topologies for medium- and high-voltage applications, owing to its advantages in modularity, scalability, and reliability [1][2][3]. By adjusting the number of series-connected submodules (SMs) in each arm, the MMC can be configured to achieve virtually any desired voltage level [4]. This flexibility eliminates the need for series-connected semiconductor devices and significantly reduces the size of bulky output filters. Furthermore, the modular architecture inherently supports redundancy, thereby enhancing system reliability and fault tolerance [5].

The topology of the Hybrid Modular Multilevel Converter (HMMC) was first introduced in [7] and further reviewed in [8]. Since then, several variations have been proposed to enhance the original MMC architecture. A common approach involves replacing a portion of the low-voltage (LV) submodules (SMs) with high-voltage (HV) switches. This modification aims to reduce the overall system footprint and cost while maintaining performance. The



Figure 1.1: MMC valve hall from Hitachi Energy [6]

remaining SMs form a chain-link (CL) that is responsible for shaping the AC output voltage, thereby preserving low voltage distortion comparable to that of a conventional MMC.

Among all the Hybrid Modular Multilevel Converter (HMMC), the Flying Capacitor Hybrid Modular Multilevel Converter caught the interests. This is because the FC-HMMC offers notable advantages in terms of reduced device count and lower submodule (SM) capacitance requirements. These reductions contribute to a more compact converter design and lower overall system cost. Additionally, the high-voltage (HV) switches in the FC-HMMC benefit from natural soft-switching characteristics, which help minimize power losses and simplify the design of series-connected devices.

1.2 Problem Statement

Although Modular Multilevel Converter has various advantages, it still faces several limitations when compared to conventional two-level or multilevel voltage-source converters (VSCs) [3]. Firstly, the number of power devices in an MMC is significantly higher—doubled when using half-bridge (HB) submodules and quadrupled with full-bridge (FB) submodules, resulting in

increased conduction losses compared with other topologies such as neutral point clamped converter [9]. Additionally, the large number of submodules and associated components necessitates a substantial number of gate driver units and sensors, which adds complexity to the control system and increases implementation costs.

Secondly, MMCs require a considerable number of capacitors to store energy and suppress voltage ripple across the submodule DC-link capacitors. These capacitors can occupy more than 50 percent of the converter's total submodules' volume [10], posing challenges in terms of size, cost, and thermal management.

While the FC-HMMC offers many improvements over the standard MMC, it also presents challenges related to the series connection of Insulated-Gate Bipolar Transistor(IGBT) switches shown in the Figure 1.2. IGBTs are used [11] for their high power ratings and controllability, however, thyristors are considered due to low cost and high current long duration SCFM capability [12]. This leads to the consideration of using alternative devices such as the thyristor shown in the Figure 1.3.



Figure 1.2: An image of press pack IGBT module (IGBT) [13]

1.3 Goals

The primary objective of this thesis is to investigate the operating principles of the Flying Capacitor Hybrid Modular Multilevel Converter. A detailed



Figure 1.3: An image of thyristor from Hitachi Energy [14]

simulation model is therefore developed using Power Systems Computer-Aided Design(PSCAD) to analyze the converter's behavior under various operating conditions. In addition, this work focuses on the investigation of the feasibility of replacing insulated gate bipolar transistors with thyristors in the Flying Capacitor Hybrid Modular Multilevel Converter. Special attention is given to the commutation challenge introduced by this replacement, and potential solutions are explored and evaluated. To achieve these, the project is structured around the following sub-goals:

1. Analyze and demonstrate the fundamental operating principles of the FC-HMMC.
2. Develop and explain the closed-loop control strategy applied to the FC-HMMC.
3. Construct a complete FC-HMMC simulation model in PSCAD.
4. Propose a commutation method suitable for replacing IGBT valve with thyristors valve.
5. Validate the proposed commutation method through the time simulation model.

1.4 Structure of the Thesis

The structure of this thesis is organized as follows:

Chapter 2 introduces the fundamental operating principles of the FC-HMMC, including its circuit topology and mode of operation in both single-phase and three-phase configurations.

Chapter 3 presents the design and implementation of the closed-loop control strategy for the FC-HMMC, focusing on current allocation and voltage balancing between the chain links and the flying capacitor.

Chapter 4 explores the feasibility of replacing conventional IGBT switches with thyristors. It discusses the associated commutation challenges and proposes a suitable method to enable reliable thyristor operation within the FC-HMMC topology.

Chapter 5 details the development of a complete FC-HMMC simulation model in PSCAD, including the modeling of power components, control systems, and switching logic.

Chapter 6 presents the simulation results and performance analysis of the proposed converter.

Chapter 7 summarizes the key findings of the thesis and outlines potential directions for future research and development in the area of hybrid multilevel converters.

Chapter 2

FC-HMMC Working Principle

This chapter presents a comprehensive overview of the Flying-Capacitor Hybrid Modular Multilevel Converter (FC-HMMC). Section 2.1 introduces the circuit topology of the FC-HMMC. Section 2.2 details the operational principles of the converter under single-phase conditions. Section 2.3 extends this analysis to three-phase operation. Section 2.4 discusses the current distribution within the converter circuits. Section 2.5 addresses the mechanisms for power balancing between the AC grid and the DC sources. Section 2.6 outlines the methodology for determining the appropriate capacitance of the flying capacitor. Section 2.7 analyzes the power flow among the positive chain link, negative chain link, and the flying capacitor. Section 2.8 explores additional operational states that the circuit can achieve. Finally, Section 2.9 uses a table to compare the differences between MMC and FC-HMMC.

2.1 Circuit Topology of FC-HMMC

Compared to the conventional Modular Multilevel Converter (MMC), the Flying Capacitor Hybrid Modular Multilevel Converter (FC-HMMC) exhibits significant differences in circuit topology, as illustrated in Figure 2.1. In the FC-HMMC configuration, half of the submodules in each phase are replaced with controlled switches. This modification substantially reduces the total number of submodules required, thereby simplifying the overall system structure and potentially lowering implementation costs.

A key feature of the FC-HMMC is the inclusion of a flying capacitor, which connects the midpoint of the upper arm to the midpoint of the lower arm. This capacitor plays a crucial role in balancing the energy between the

two arms, contributing to stable and efficient operation. To ensure proper voltage withstand capability, the voltage across the flying capacitor, as well as the voltages of the upper and lower chain links, are each maintained at half of the total DC-side voltage. This voltage distribution strategy will be further analyzed and justified in the subsequent section.

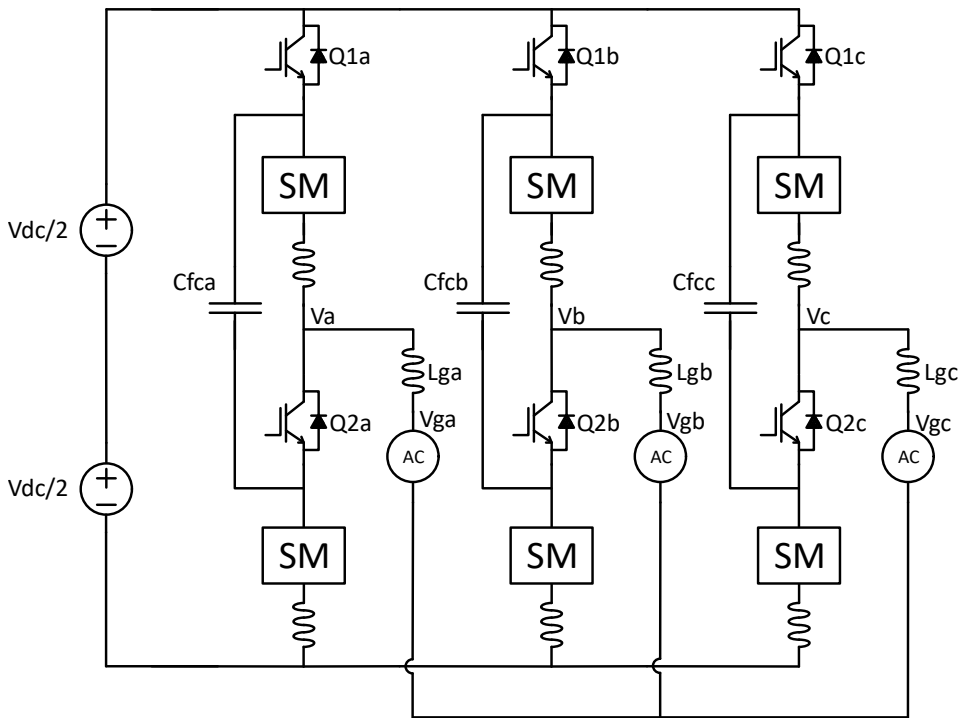


Figure 2.1: Topology of FC-HMMC

2.2 Single Phase Operation

A representative phase is selected in this section to elucidate the underlying operating principle of FC-HMMC. The work sequence of the upper arm switch and lower arm switch follows the voltage output polarity, which means when $v_a > 0$, the upper arm switch Q_{1a} turns on and the lower arm switch Q_{2a} turns off, and this state is called **P** state. During this state, the upper chain link will shape the output waveform with the reference, which will be demonstrated in the chapter 3, shown in the Figure 3.3. Simultaneously, the lower chain link connects with the flying capacitor to support the DC side voltage and control the current flowing through the capacitor. In contrast, when $v_a < 0$, the lower

arm switch Q_{2a} turns off and the lower arm switch Q_{2a} turns on, and this state is called the **N** state. During this state, the lower chain link shapes the output waveform with the reference shown in the figure. At the same time, the upper chain link connects with the flying capacitor to control the current and balance the energy between both. The voltage for upper and lower chain links during different state can be calculated as in Equation 2.1.

$$\begin{cases} v_{pa} = \frac{1}{2}V_{dc} - v_a, v_{na} = V_{dc} - v_{FCa} & (\text{P state}) \\ v_{pa} = v_{FCa}, v_{na} = \frac{1}{2}V_{dc} + v_a & (\text{N state}) \end{cases} \quad (2.1)$$

The voltage of the flying capacitor v_{FC} is set to half the DC link voltage, which means the maximum chain link voltage becomes half the DC link voltage as well, reducing the sub-module number to half, and it also means the maximum withstand voltage of both switches is half the DC link voltage.

Based on circuit topology and Kirchhoff's current law, different components' current can be expressed. The i_{pa} and i_{na} are the upper and lower chain link currents, and i_{FCa} represents the current flowing through the flying capacitor. The positive and negative DC bus currents are named as i_{dcpa} and i_{dcna} . The equations of current can be derived as Equation 2.2 based on different states shown in the Figure 2.2 and Figure 2.3. It can be observed that the composition of the i_{dcpa} and i_{dcna} is not symmetrical.

$$\begin{cases} i_{dcpa} = i_{pa} + i_{FCa}, i_{pa} = i_a, i_{FCa} = i_{na} = i_{dcna} & (\text{P state}) \\ i_{dcpa} = 0, i_{pa} = -i_{FCa}, i_{na} = i_{dcna} = -i_a & (\text{N state}) \end{cases} \quad (2.2)$$

Considering the AC grid is connected with the converter, detailed Kirchhoff's voltage equations can be derived based on the circuit topology. For example, the circuit loops are shown in the Figure 2.4 and Figure 2.5 during the P states. By applying the Kirchhoff's voltage law on the circuit, the Equation 2.3 and Equation 2.4 can be derived:

$$\frac{1}{2}V_{dc} = v_{pa} + (L_{pa} + L_{ga})\frac{di_a}{dt} + v_{ga} \quad (2.3)$$

$$V_{dc} = v_{fca} + v_{na} + v_{L_na} \quad (2.4)$$

where L_p and L_n are the inductances of the upper and lower arm reactors, and accordingly v_{L_n} represents the voltage drop on the lower arm reactor.

Same for the N state, the circuit loops are shown in the Figure 2.6 and Figure 2.7. By applying Kirchhoff's voltage law on the circuit, the Equation

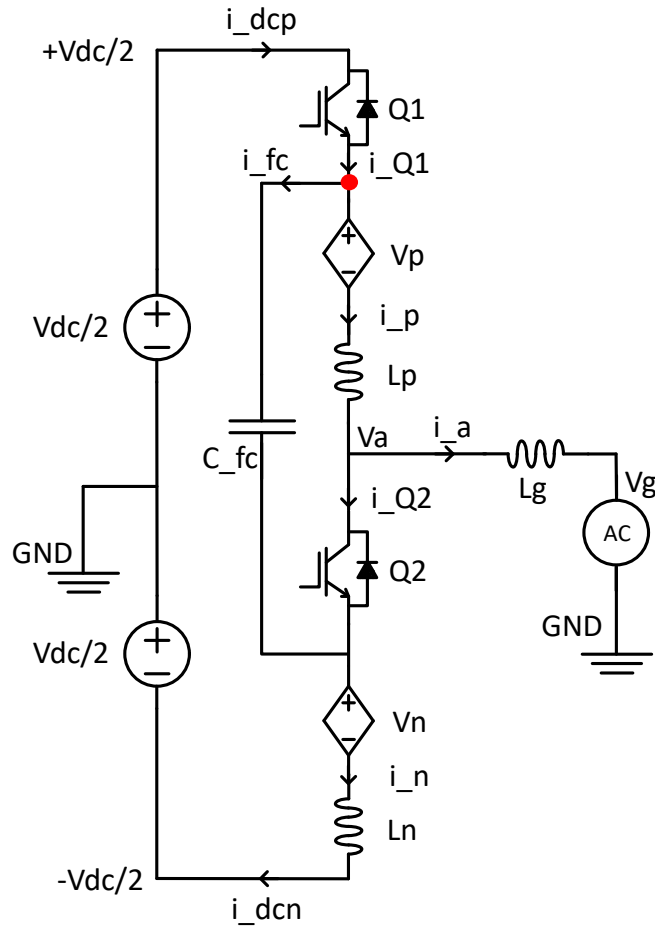


Figure 2.2: KCL equation 1

2.5 and Equation 2.6 can be derived:

$$-\frac{1}{2}V_{dc} = -v_{na} + (L_{na} + L_{ga})\frac{di_a}{dt} + v_{ga} \quad (2.5)$$

$$v_{fc} = v_{pa} + v_{L_{pa}} \quad (2.6)$$

2.3 Three Phases Operation

To operate the FC-HMMC, three phases should be controlled independently but synthesize together to generate the input and output waveforms. FC-HMMC is different from the MMC since the MMC has fixed electrical

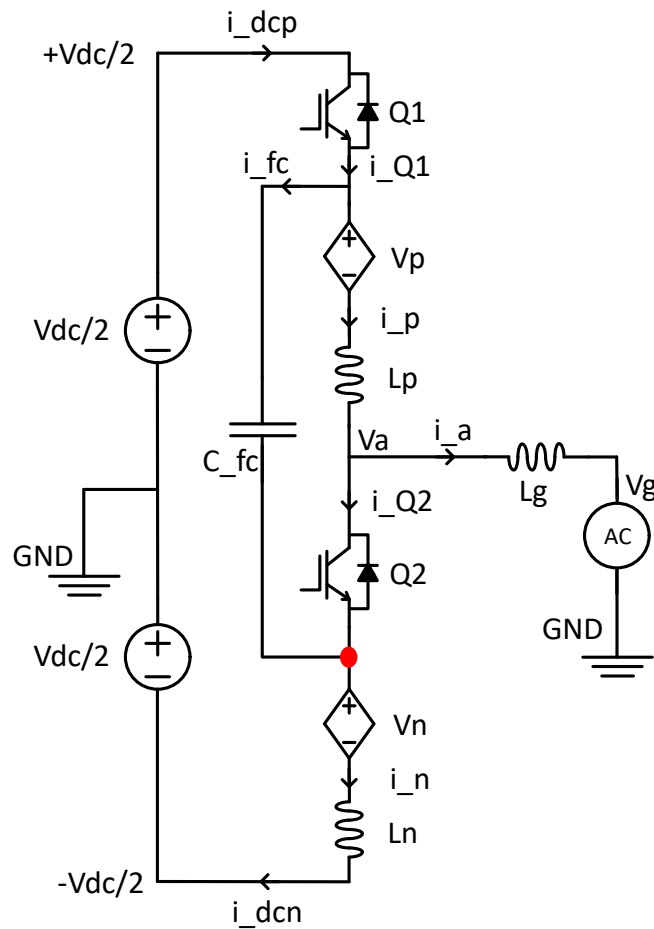


Figure 2.3: KCL equation 2

connections of converter arms throughout a fundamental cycle, while the FC-HMMC has different equivalent circuits based on the switching sequences of six director switches of six arms. Figures 2.8, 2.9, 2.10, 2.11, 2.12, 2.13 show all six states during normal working conditions. An appropriate power conversion and constant DC side current synthesis can only be achieved by coordinated control of three phases of FC-HMMC. To effectively eliminate the DC current ripple, the current allocation between each component is proposed, which will be further illustrated in the following section.

The six operational states are evenly distributed over a fundamental cycle, with each state occupying a duration of $T/6$ where T denotes the fundamental ac period. To facilitate a clearer understanding of the converter's working principle, a systematic naming convention is introduced for these states.

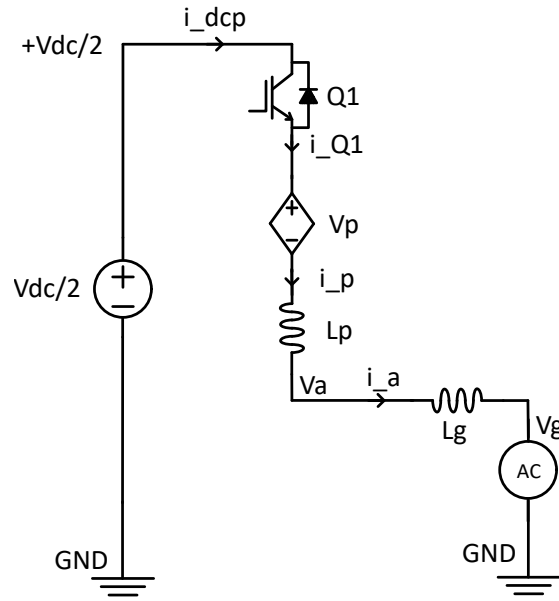


Figure 2.4: KVL equation 1

For example, PNP means phases a, b, and c are in P, N, and P states, respectively. Assuming that the phase A voltage angle progresses from 0 to 2π , each segment spans an angular duration of $\frac{\pi}{3}$. Accordingly, each state is named based on its corresponding angular segment. The six states follow the sequence outlined in Table 2.1, and their relationship with the output voltage waveform is illustrated in Figure 2.14.

Table 2.1: Working states

Time	Name
0 to $\frac{\pi}{3}$	PNP
$\frac{\pi}{3}$ to $\frac{2\pi}{3}$	PNN
$\frac{2\pi}{3}$ to π	PPN
π to $\frac{4\pi}{3}$	NPN
$\frac{4\pi}{3}$ to $\frac{5\pi}{3}$	NPP
$\frac{5\pi}{3}$ to 2π	NNP

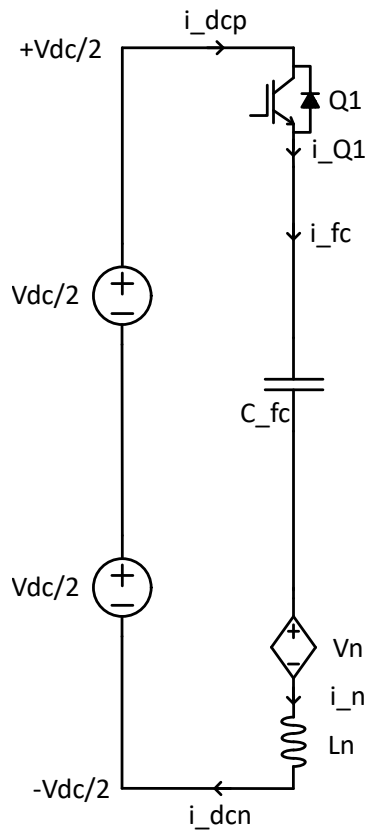


Figure 2.5: KVL equation 2

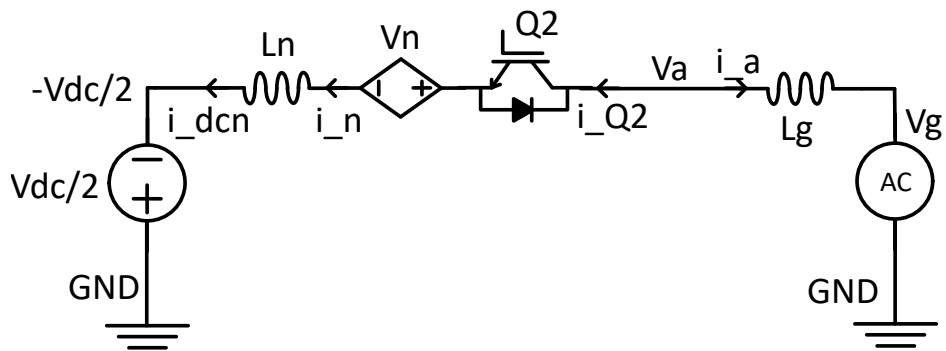


Figure 2.6: KVL equation 3

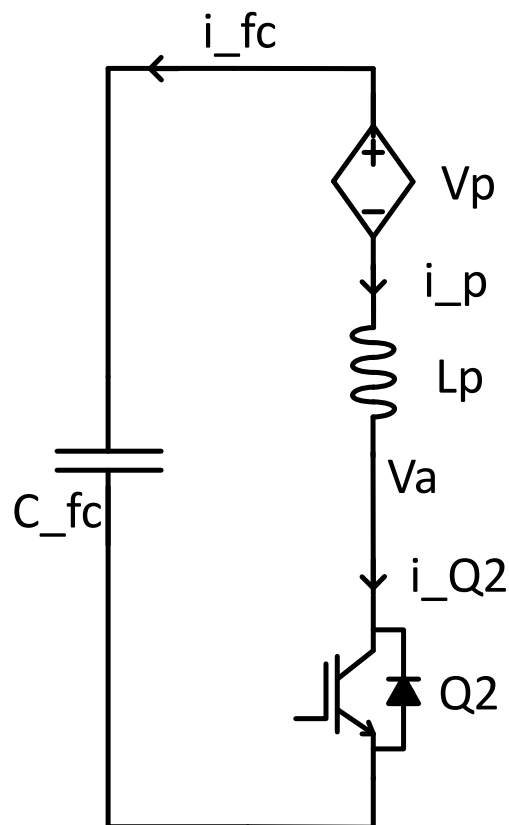


Figure 2.7: KVL equation 4

2.4 Current Allocation

Based on the working states listed in the Table 2.1, there are three states in which only one phase is connected with the positive dc pole, which are states PNN, NPN, and NNP. Other three states have the situation where the two phases are connected to the DC source's positive side, sharing the current. To effectively eliminate the harmonics of the DC current, the trapezoidal-shaped current [15][11] is used here to make sure the DC side current remains constant. In this case, the DC bus filter is no longer required in the circuit. The current formulae are followed by the Equation 2.7.

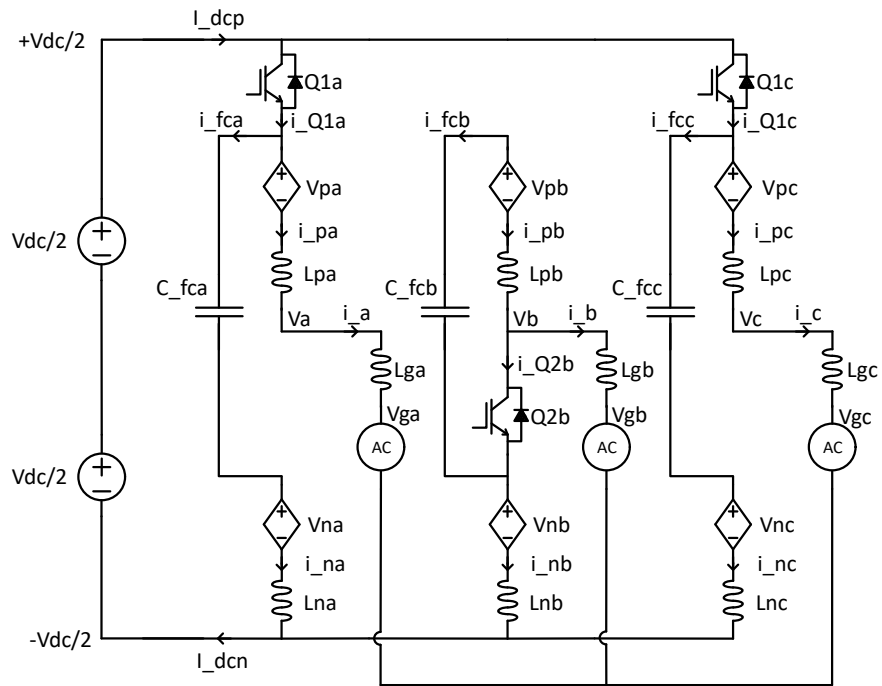


Figure 2.8: State PNP

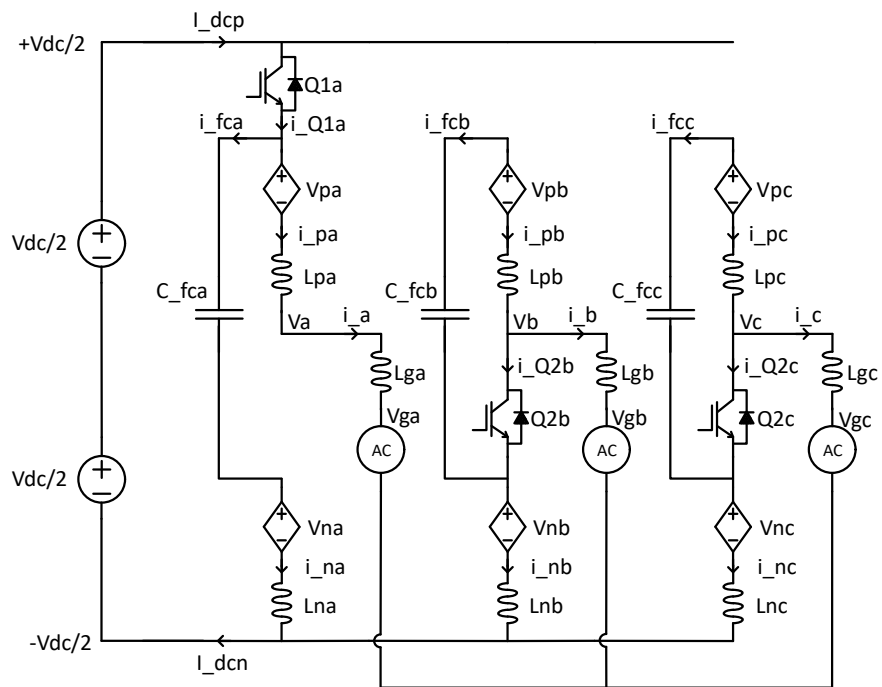


Figure 2.9: State PNN

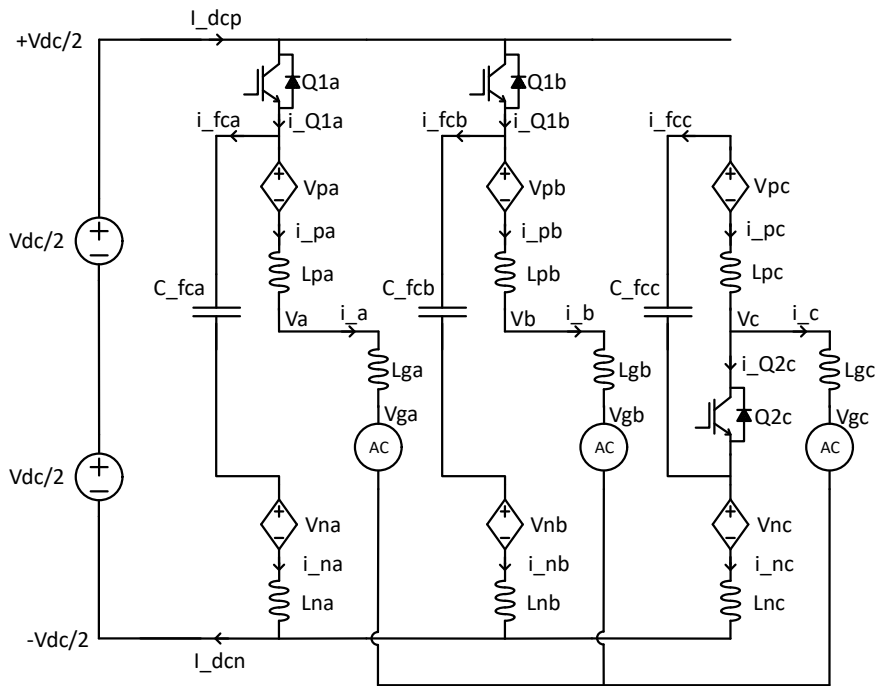


Figure 2.10: State PPN

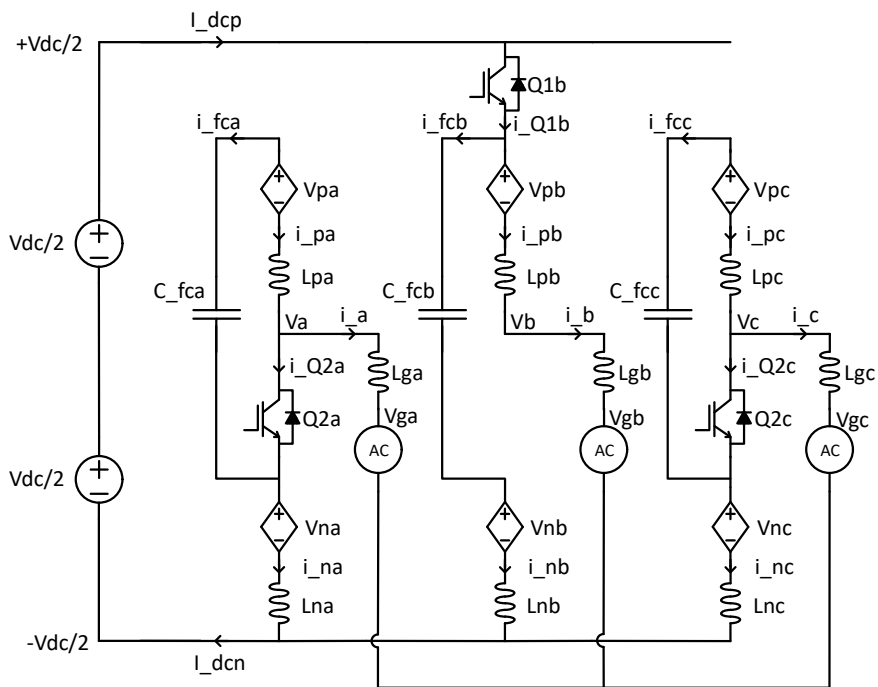


Figure 2.11: State NPN

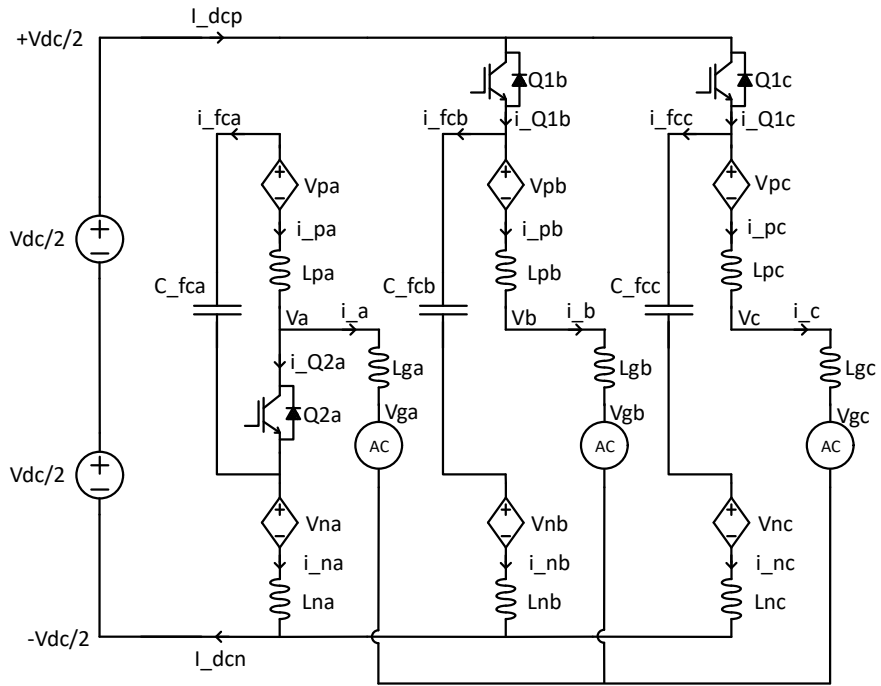


Figure 2.12: State NPP

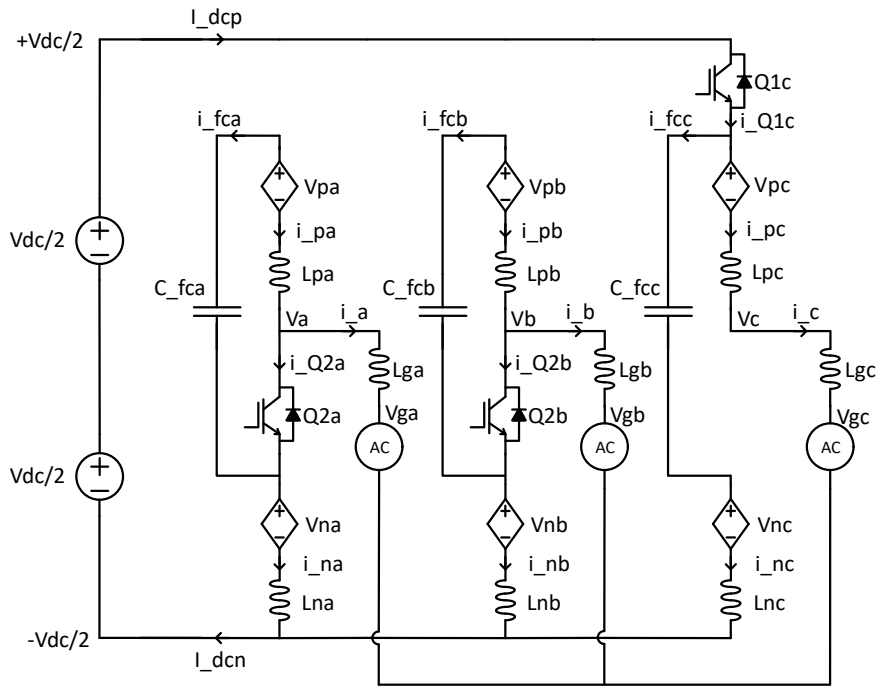


Figure 2.13: State NNP

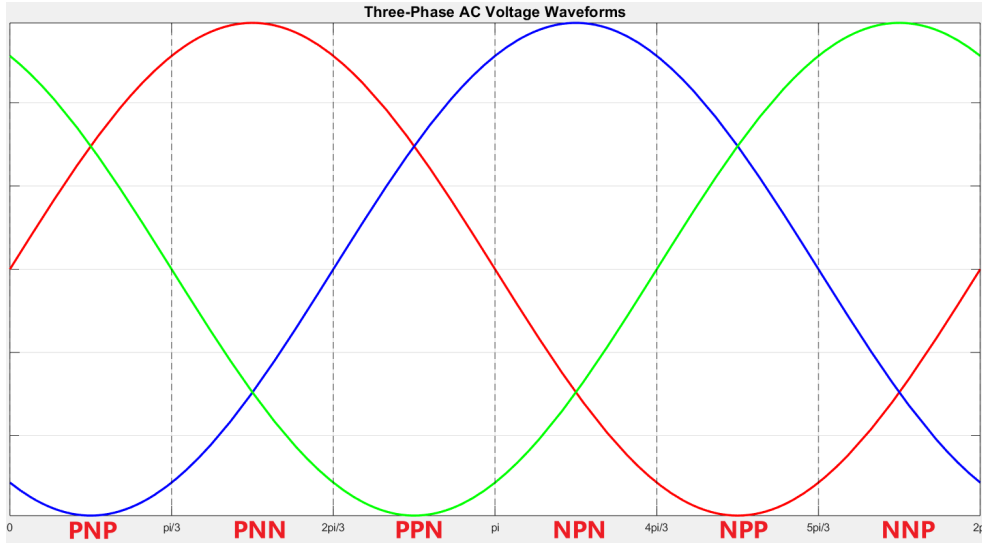


Figure 2.14: Six equivalent states in a fundamental cycle

$$\begin{cases} i_{dc} = i_{dcpc} + i_{dcpa} & (\text{PNP}) \\ i_{dc} = i_{dcpa} & (\text{PNN}) \\ i_{dc} = i_{dcpa} + i_{dcpb} & (\text{PPN}) \\ i_{dc} = i_{dcpb} & (\text{NPN}) \\ i_{dc} = i_{dcpb} + i_{dcpc} & (\text{NPP}) \\ i_{dc} = i_{dcpc} & (\text{NNP}) \end{cases} \quad (2.7)$$

The current of the flying capacitor and chain link is then derived by the Equation 2.2. During the P state, the positive chain link current is ac sinusoidal current, while the flying capacitor or negative chain link current, is the difference between the ac grid sinusoidal current and the trapezoidal current. During the N state, the positive chain link carries subtracted current while the negative chain link carries the sinusoidal ac grid current. An example of the current and voltage shape when the converter works with unit power factor is shown in the Figure 2.15.

2.5 Power Balancing

With proper current allocation, the DC current value can be calculated by the power flow balancing equation. The plateau voltage level of the trapezoidal waveform in PNN, which is the DC current value as well, can be derived with

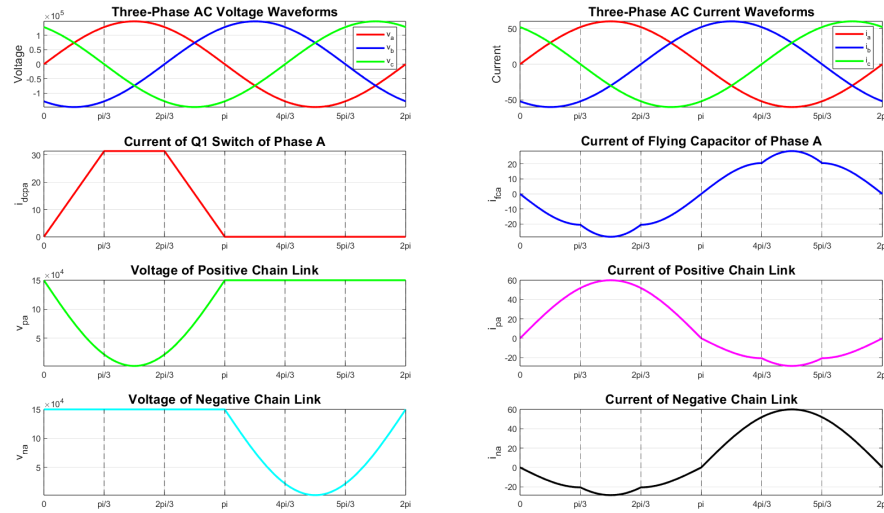


Figure 2.15: Current allocation in unit power factor

the following Equation 2.8.

$$V_{dc}I_{dc} = \frac{\hat{V}_{ac}\hat{I}_{ac}}{2}\cos\phi \quad (2.8)$$

where \hat{V}_{ac} and \hat{I}_{ac} are the ac-side peak voltage and current, respectively, and ϕ represents the the phase angle between voltage and current. If the modulation index is defined as the Equation 2.9:

$$M = \frac{\hat{V}_{ac}}{\frac{1}{2}V_{dc}} \quad (2.9)$$

Then the expression of DC current can be simplified to Equation 2.10:

$$I_{dc} = \frac{MI_{ac}\cos\phi}{4} \quad (2.10)$$

2.6 Flying Capacitor Sizing

Another difference between FC-HMMC and normal MMC topology is that one flying capacitor is connected from the middle point of the upper submodules and switches and the middle point of the lower submodules and switches. The flying capacitor holds half the dc link voltage thus helping in

reduction of number of SMs and their capacitance size, which means both the converter size and cost are reduced. The flying capacitor size is one of the crucial parameters to ensure the FC-HMMC works in the steady state. Based on the characteristic equations of the capacitor, Equation 2.11 is derived:

$$i_{fc} = C_{fc} \frac{dV_{fc}}{dt} \quad (2.11)$$

Considering the Equation 2.2, the flying capacitor current is the difference subtraction of the sinusoidal waveform and the trapezoidal waveform. Taking the state P as an example, during the time 0 to $\frac{T}{6}$, the trapezoidal current increases from 0 to I_{dc} , during the time $\frac{T}{6}$ to $\frac{T}{3}$, the trapezoidal current reaches the plateau and remains at I_{dc} , during the time $\frac{T}{3}$ to $\frac{T}{2}$, the trapezoidal current decreases to zero. Here, the sinusoidal waveform part is the output current, which is decided by the active power reference P and the reactive power reference Q .

If the reactive power reference Q is zero, this means the phase shift between the current and voltage is zero, and the converter works in unit power factor mode, which is shown in Figure 2.15. Then the voltage ripple on the flying capacitor can be calculated with the following Equation 2.12:

$$\begin{aligned} \Delta V_{fc} &= \frac{1}{C_{fc}} \int_0^{\frac{T}{2}} i_{fc}(t) dt \\ &= \frac{1}{C_{fc}} \int_0^{\frac{T}{2}} (i_a(t) - i_{dcpa}(t)) dt \end{aligned} \quad (2.12)$$

When the converter is not working in unit power factor mode, which is shown in Figure 2.16, the output current have a phase shift with the output voltage, the current flowing through the flying capacitor is higher, which gives a higher ripple of flying capacitor voltage V_{fc} .

The worst scenario would be the case when the power factor goes to 90 degrees or -90 degrees, at this time, all the AC current flows through the flying capacitor and creates the largest voltage ripple on the capacitor. In this case the voltage ripple can be calculated as in the Equation 2.13, and the worst-case current allocation is shown in the Figure 2.18 and Figure 2.19.

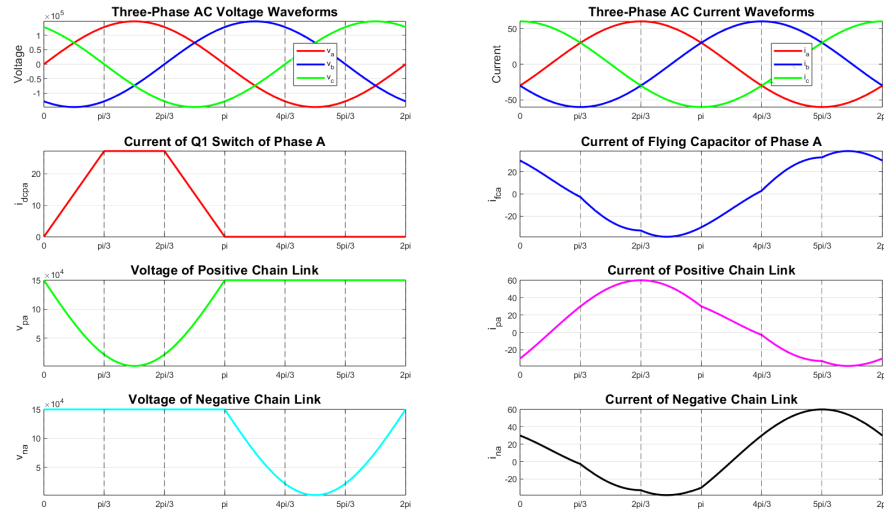


Figure 2.16: Current allocation 30 degree phase shift

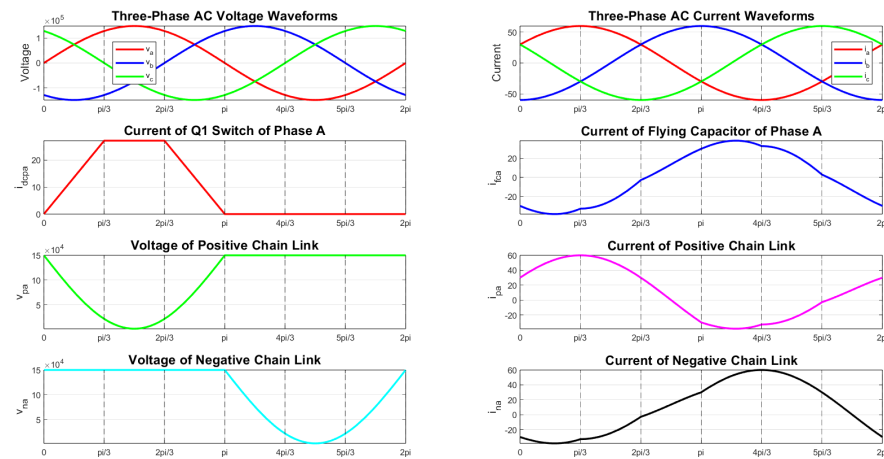


Figure 2.17: Current allocation -30 degree phase shift

$$\begin{aligned}
 \Delta V_{fcmax} &= \frac{1}{C_{fc}} \int_0^{\frac{T}{2}} i_{fc} dt \\
 &= \frac{1}{C_{fc}} \int_0^{\pi} \hat{I} \sin(t) dt \quad (2.13)
 \end{aligned}$$

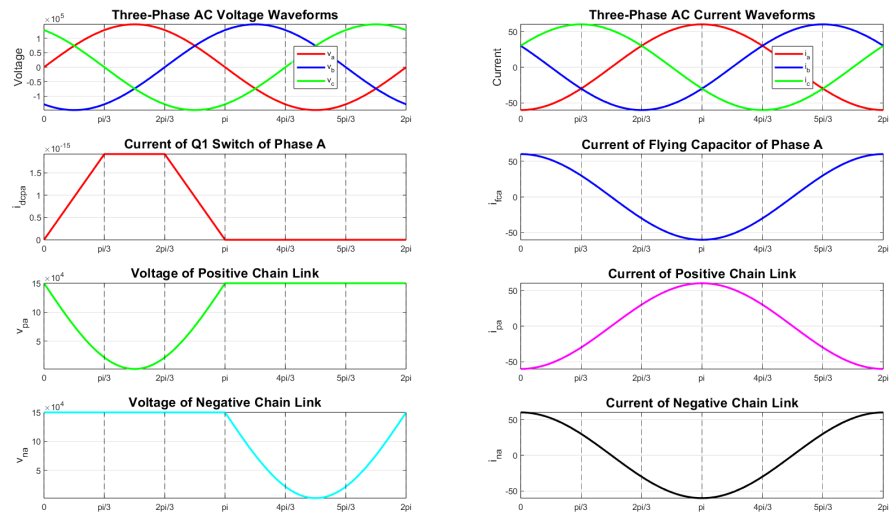


Figure 2.18: Current allocation 90 degree phase shift

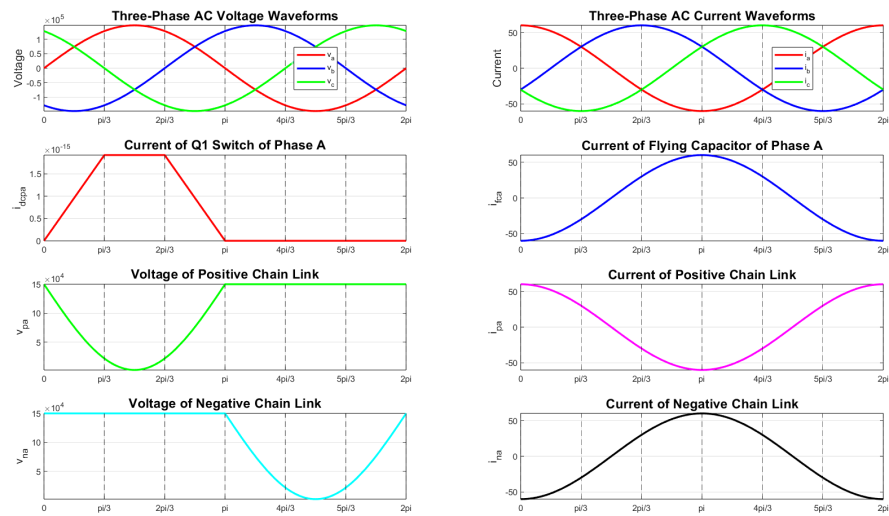


Figure 2.19: Current allocation -90 degree phase shift

2.7 Power Flow Analysis

Power flow analysis is important for understanding the power relationship between the upper chain link, lower chain link, flying capacitor, AC, and DC power flow. The current and voltage notations are shown in the Figure 2.20.

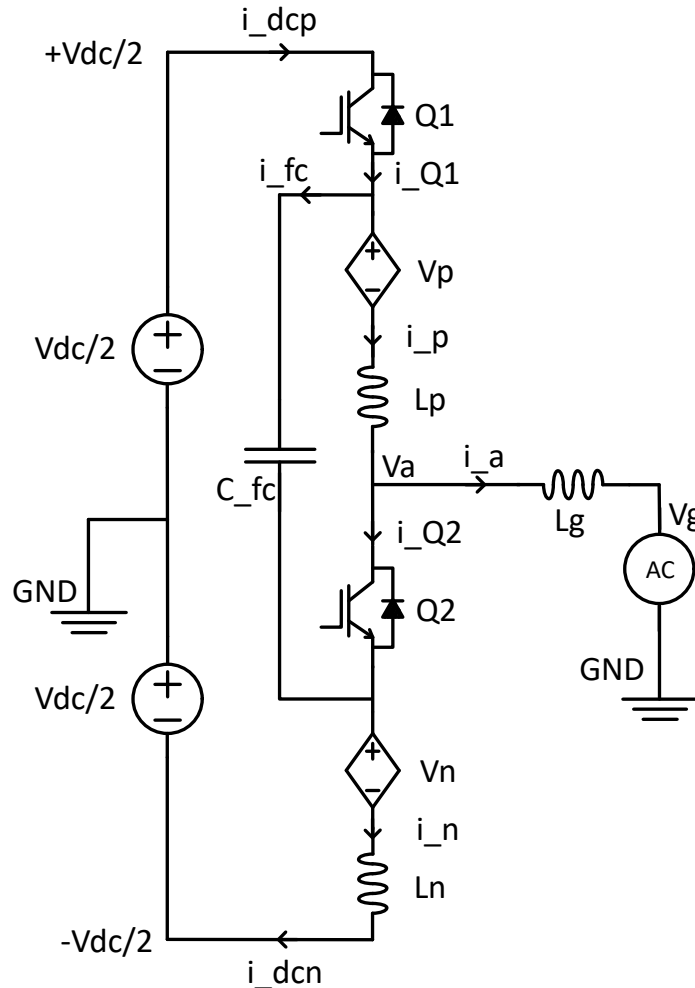


Figure 2.20: Power flow analysis

Taking inverter mode of converter as example, during the positive state, the DC side transfers the power to the upper chain link and the ac side directly through i_p , which is actually equal to i_a . Meanwhile, the current of the flying capacitor i_{fc} passes through the lower chain link, which equals i_n . In this case the equations of power flow can be developed as Equation 2.14, where P_{clp} , P_{fc} , and P_{cln} represent the power of positive chain link, flying capacitor and negative chain link.

$$\begin{aligned}
P_{clp} &= V_p i_a \\
P_{fc} &= V_{fc} (i_a - i_{dcp}) \\
P_{cln} &= V_n (i_a - i_{dcp})
\end{aligned} \tag{2.14}$$

During the negative state, the power analysis is done similarly to the positive state. The grid side current directly flows through the negative chain link i_n , which is equal to $-i_a$. Meanwhile, the current of the flying capacitor i_{fc} passes through the upper chain link, which is equal to $i_a + i_{Q2}$. The relationship can be developed as expressed in following Equation 2.15.

$$\begin{aligned}
P_{clp} &= -V_p (i_a + i_{Q2}) \\
P_{fc} &= V_{fc} (i_a + i_{Q2}) \\
P_{cln} &= V_n i_a
\end{aligned} \tag{2.15}$$

It is to be noted that the current i_{dcp} and i_{Q2} represent the trapezoidal current during the P state and the N state respectively, the value of the trapezoidal current plateau is I_{dcp} and I_{dcn} accordingly, these two parameters are the key parameters of power flow control and will be further discussed and developed in the chapter 3.

2.8 Redundant States

Except for the standard six states during the in steady-state normal working condition, there are some additional redundant states as well. Initially, we assumed that the upper arm and lower arm operated in a complementary manner. However, the switches can also operate simultaneously, creating neutral states.

When both the upper arm and lower arm switches turn on, which means both chain links are connected in series with the DC source, this state is named as **Z** state. When the upper arm and lower arm switch both turn off, which means both chain links are connected in series with the flying capacitor and load side, this state is named as **O** state. Mathematically, since each phase can have four states. Thus, there will be $4 * 4 * 4 = 64$ unique possibilities in total, a few special cases are plotted in the following Figures 2.21, 2.22, 2.23, and 2.24. These cases could be utilized during transient conditions, but this has

not been explored further in this thesis.

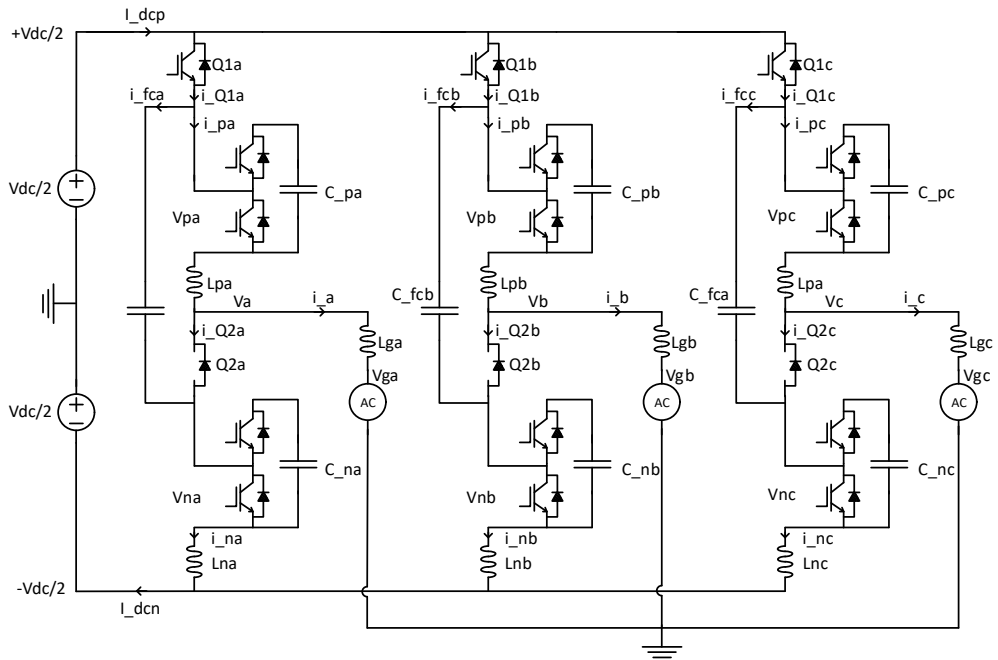


Figure 2.21: Equivalent converter circuit representing redundant state PPP

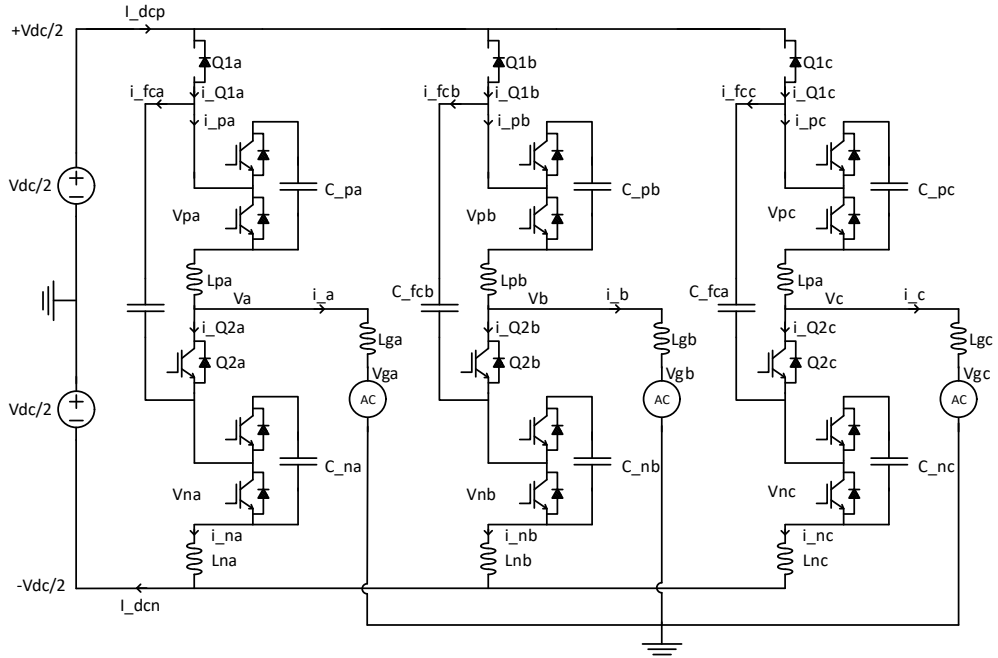


Figure 2.22: Equivalent converter circuit representing redundant state NNN

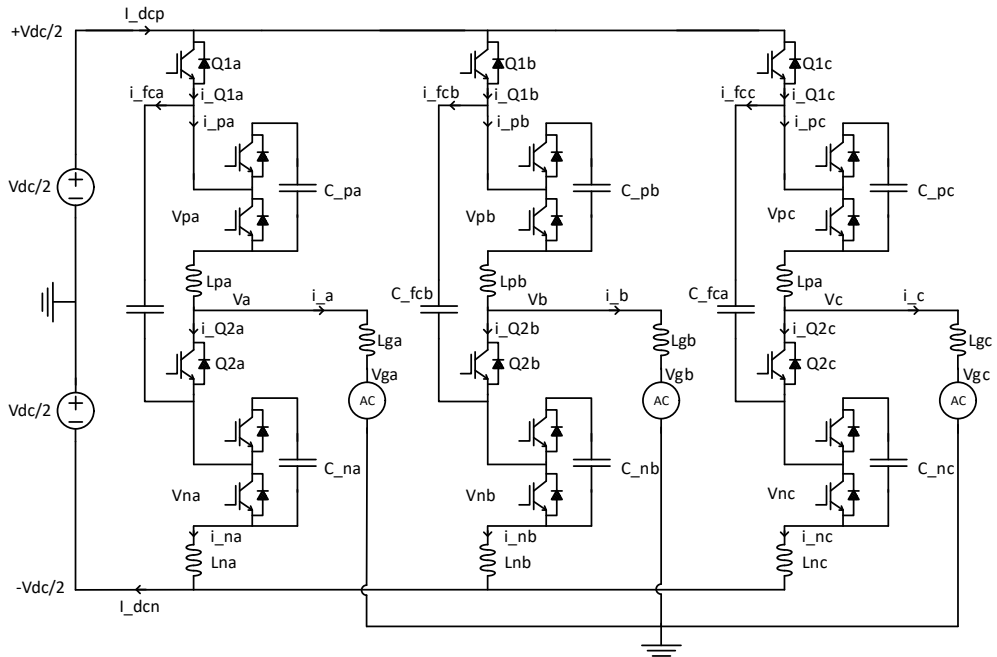


Figure 2.23: Equivalent converter circuit representing redundant state ZZZ

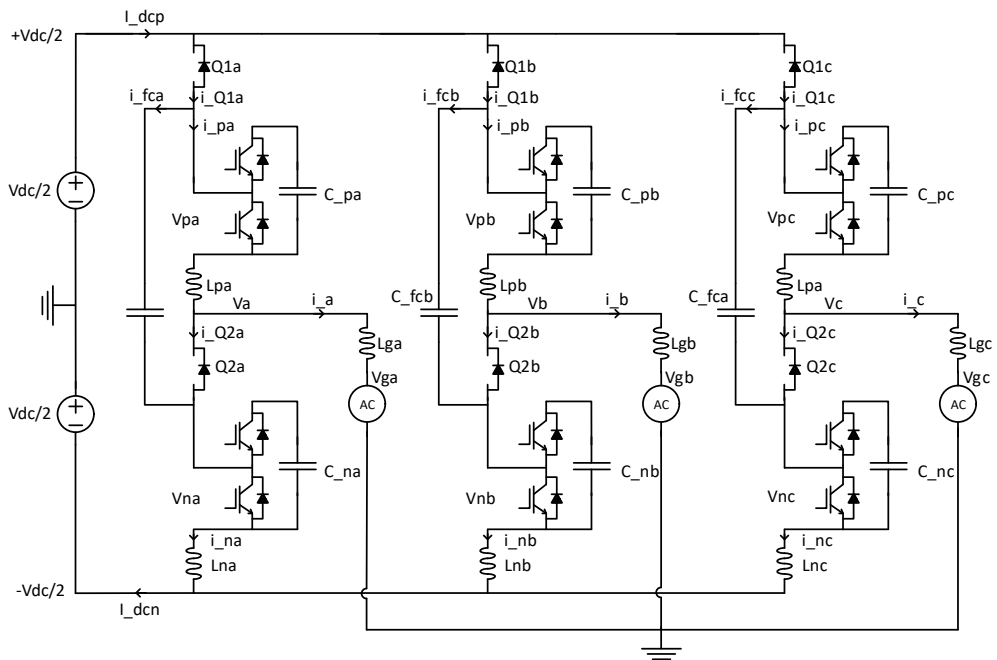


Figure 2.24: Equivalent converter circuit representing redundant state OOO

Another critical operational state that must be considered is the occurrence of a severe fault. To protect the components of the FC-HMMC during such events, it is essential to trip all submodules of the converter immediately. In this fault condition, all switches are opened to isolate the fault from the rest of the system. As a result, the converter transitions into a protective mode known as the blocked state, denoted as State **B**. The corresponding circuit configuration for this state is illustrated in Figure 2.25.

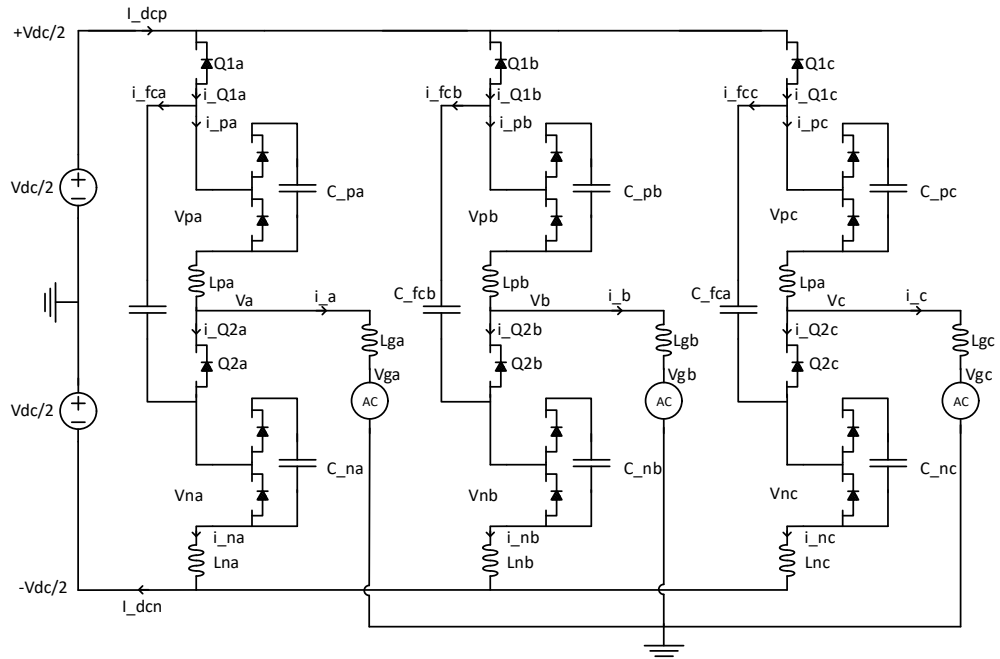


Figure 2.25: Equivalent converter circuit representing redundant state BBB

2.9 Comparison Between MMC and FC-HMMC

A comparison Table 2.2 previously presented in the study by Liu et al. [11] highlights various differences between the conventional MMC and the proposed FC-HMMC. Based on this table, clear advantages of the FC-HMMC can be identified and substantiated.

- The total capacitor voltage required in the FC-HMMC is lower than that in the conventional MMC.
- In the chain link configuration, the current level is higher compared to the standard MMC; however, in the switch and flying capacitor configurations, the current levels are both lower.
- For a single chain link, the voltage rating is halved compared to that of a conventional MMC.
- The number of chain links remains the same in both the FC-HMMC and MMC architectures.
- The total number of switches is reduced by 25 percent in the FC-HMMC, resulting in a lower cost.
- Conduction losses are also reduced, as fewer switches are inserted during operation.

Table 2.2: Comparison table between MMC and FC-HMMC [11]

Parameters	MMC	FC-HMMC
Capacitor energy storage	1 p.u.	0.63 p.u.
Chain link current (RMS)	1 p.u.	1.1 p.u.
Direct switch current (RMS)	1 p.u.	0.98 p.u.
Flying capacitor current (RMS)	1 p.u.	0.18 p.u.
Chain link voltage rating	1 p.u.	0.5 p.u.
Total switches number	1 p.u.	0.75 p.u.
No. of switches in conduction path	1 p.u.	0.75 p.u.

Chapter 3

FC-HMMC Closed Loop Control

The purpose of this chapter is to provide a comprehensive overview of the control strategies implemented in the Flying Capacitor Hybrid Modular Multilevel Converter. This chapter is arranged as; Section 3.1 introduces the overall closed-loop control framework, outlining its hierarchical structure and control objectives. Section 3.2 focuses on the regulation of the flying capacitor voltage to ensure energy balance and system stability. Section 3.3 presents the power control strategy, including active and reactive power regulation. Section 3.4 explains the synthesis control method used to generate the desired output voltage waveform. Section 3.5 describes the current regulation mechanism, which ensures accurate tracking of reference currents. Section 3.6 introduces the arm voltage feedforward technique to enhance dynamic response and reduce control delay. Finally, Section 3.7 discusses the control of the chain-link submodules, including voltage balancing and switching coordination to maintain waveform quality.

3.1 Closed Loop Control Overview

Given the asymmetric and complex nature of the FC-HMMC topology, it is essential to divide the control system into distinct functional blocks. This approach allows for a clearer understanding of each control mechanism and its role within the overall system. Therefore, each control block is individually illustrated and explained in detail throughout this chapter. The general structure of the closed-loop control system is depicted in Figure 3.1.

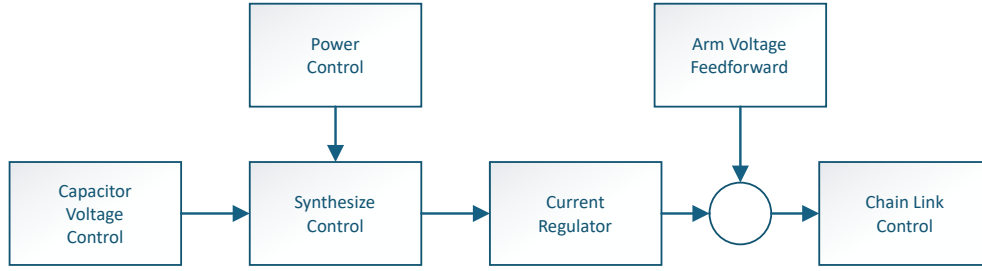


Figure 3.1: Closed loop control overview

3.2 Capacitor Voltage Control

Capacitor voltage control, shown in the Figure 3.2, is a critical component of the FC-HMMC control system, as it ensures energy balance among the upper chain links, lower chain links, and the flying capacitor within each phase. The figure only shows the control block of phase a, and the other two phases have the same control block structures. This control block is responsible for generating the DC current reference required to maintain the chain link voltage and current at their rated values. To achieve this, three closed-loop Proportional-Integral (PI) controllers are employed, each regulating a specific aspect of the energy distribution. The calculation of the basic DC bus current reference, denoted as I_{dc}^* , is calculated by the Equation 3.1.

$$I_{dc}^* = (k_{p1} + \frac{k_{i1}}{s})(V_{FC}^* + 2N_{SM}V_{SM}^* - v_{FC} - v_{Cpa} - v_{Cna}) \quad (3.1)$$

where coefficients k_{p1} and k_{i1} are the proportional and integral coefficients of the PI controller. Similarly, to balance the energy during the two different states, the P state and the N state, ΔI_{dcp}^* and ΔI_{dcn}^* are calculated by two different PI controllers from the equation 3.2 and 3.3.

$$\Delta I_{dcp}^* = (k_{p2} + \frac{k_{i2}}{s})(V_{FC}^* + N_{SM}V_{SM}^* - v_{FC} - v_{Cpa} - v_{Cna}) \quad (3.2)$$

$$\Delta I_{dcn}^* = (k_{p3} + \frac{k_{i3}}{s})(v_{FC} - \frac{V_{FC}^*}{N_{SM}V_{SM}^*}v_{Cpa}) \quad (3.3)$$

The amplitude of the trapezoidal waveform is calculated with I_{dc}^* , ΔI_{dcp}^* , and ΔI_{dcn}^* . For positive state trapezoidal amplitude, the value of I_{dcp}^* is the

sum of I_{dc}^* and ΔI_{dcp}^* , and for negative state trapezoidal amplitude, the value of I_{dcn}^* is the sum of I_{dc}^* and ΔI_{dcn}^* .

$$I_{dcp}^* = I_{dc}^* + \Delta I_{dcp}^* \quad (3.4)$$

$$I_{dcn}^* = I_{dc}^* + \Delta I_{dcn}^* \quad (3.5)$$

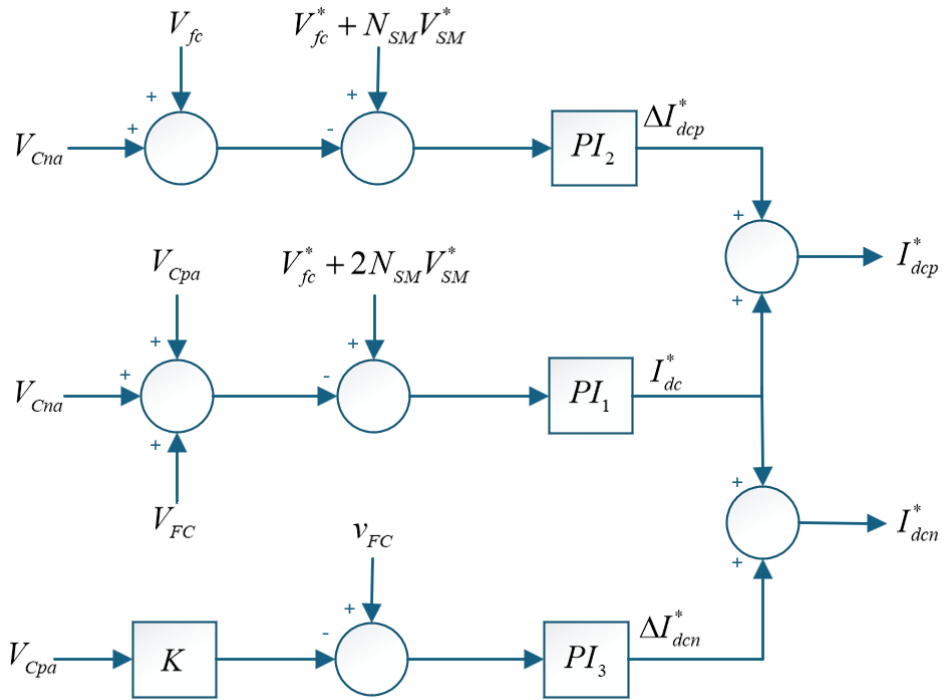


Figure 3.2: Capacitor voltage control block

3.3 Power Control

With reference to the real power and reactive-power controller of Figure 2.1, and based on the formula of power in the dq -frame [16], the real and reactive power delivered to the AC system or received from the AC system at the PCC point can be developed by the Equation 3.6:

$$\begin{cases} P(t) = \frac{3}{2}[V_d(t)i_d(t) + V_q(t)i_q(t)] \\ Q(t) = \frac{3}{2}[-V_d(t)i_q(t) + V_q(t)i_d(t)] \end{cases} \quad (3.6)$$

where V_d and V_q are the AC system dq -frame voltage components and cannot be controlled by the converter system. If the PLL is in a steady state, then $V_q = 0$ and the Equation 3.6 can be rewritten as Equation 3.7.

$$\begin{cases} P(t) = \frac{3}{2}V_d(t)i_d(t) \\ Q(t) = -\frac{3}{2}V_d(t)i_q(t) \end{cases} \quad (3.7)$$

Therefore, the active power P and reactive power Q can be calculated by the i_d and i_q components, respectively. If the control system provides fast reference tracking, then active power P and reactive power Q can be independently controlled by their respective reference commands.

3.4 Synthesize Control

The three-phase synthesized control is based on the Figure 3.3. The calculated parameters I_{dcn}^* and I_{dcp}^* from the Equation 3.4, and Equation 3.5 from capacitor voltage control, are used as the inputs for synthesized control block. These two parameters represent the amplitude of the trapezoidal waveform during the P and N state, which are the current waveforms of the upper switch and lower switch.

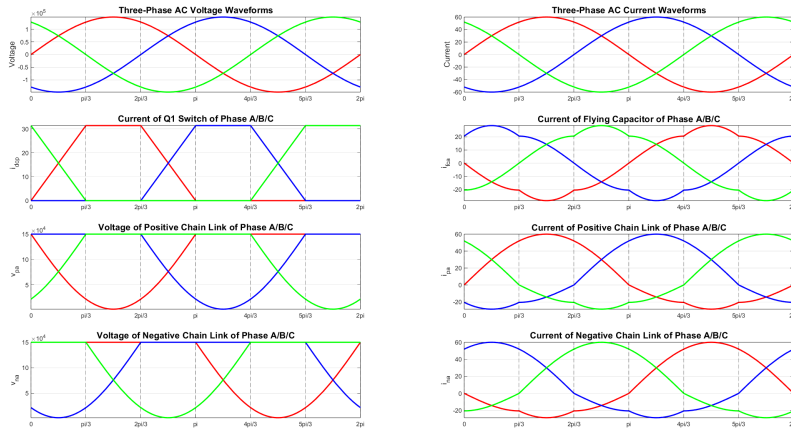


Figure 3.3: Synthesize control

The flower-shaped waveforms in Figure 3.6 are the current waveforms of the flying capacitors, they are calculated by Equation 2.2, which in fact is the difference of the ac sinusoidal output current from Figure 3.4 and the trapezoidal current of the director switch from Figure 3.5.

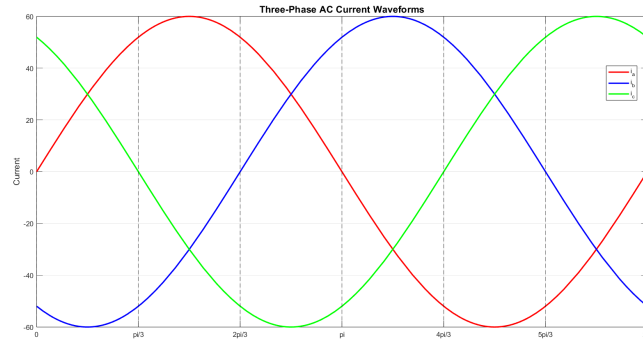


Figure 3.4: Synthesize control output current

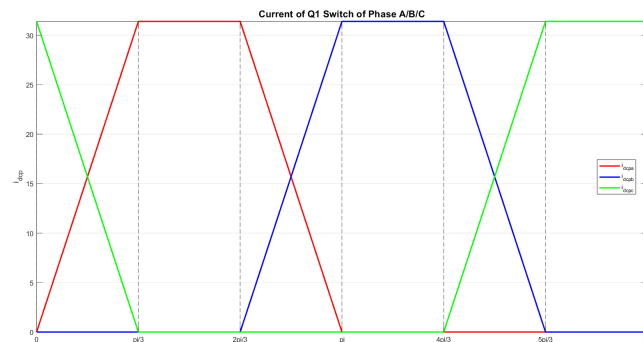


Figure 3.5: Synthesize control switch current

By deriving the current waveforms of the flying capacitor and switches, depending on the positive state or negative state, the current of the chain link can be derived based on the Equation 2.2. These two waveforms, shown in the Figure 3.7 and 3.8, are the current references for the upper and lower chain links and calculated in the current regulator control block.

3.5 Current Regulator

The current regulator is a simple PI controller. The error fed is the difference between the reference chain link current calculated from the synthesized

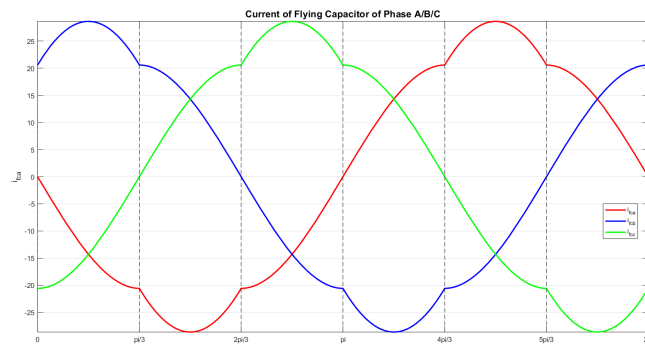


Figure 3.6: Synthesize control flying capacitor current

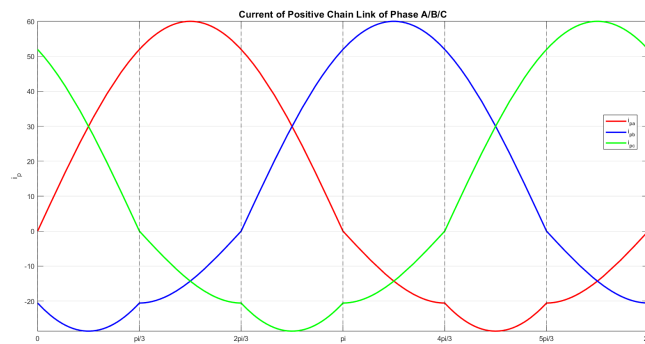


Figure 3.7: Synthesize control positive chain link

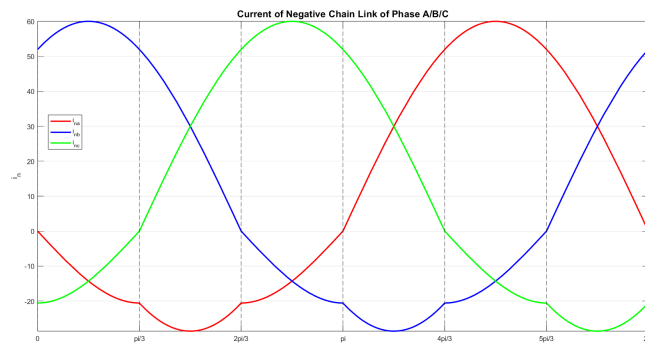


Figure 3.8: Synthesize control negative chain link

control in section 3.4 and the actual chain link current. If taking phase A upper chain link as an example, the error of chain link current is calculated by the Equation 3.8:

$$e_{pa} = i_{pa}^* - i_{pa} \quad (3.8)$$

With the PI controller, the v_{paD} can be calculated by the Equation 3.9, which is shown in the Figure 3.9.

$$v_{paD} = (k_p + \frac{k_i}{s})(i_{pa}^* - i_{pa}) \quad (3.9)$$

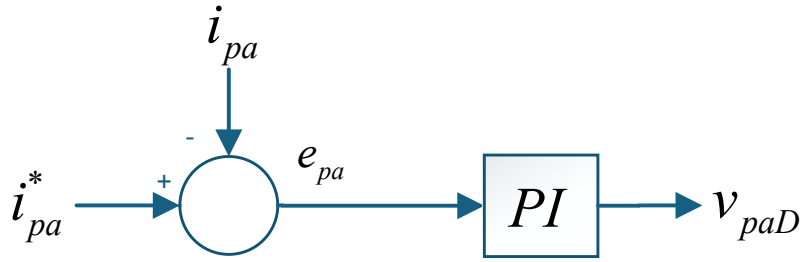


Figure 3.9: Current regulator control block

Similarly, the v_{naD} is calculated in the same way by the Equation 3.10

$$v_{naD} = (k_p + \frac{k_i}{s})(i_{na}^* - i_{na}) \quad (3.10)$$

3.6 Arm Voltage Feedforward

The control algorithm of arm voltage feedforward is based on the Equation 3.11, to give the preliminary voltage reference of the upper chain link and lower chain link. During the P state, the voltage reference of the upper chain link is the subtraction between half the DC source voltage value and the MMC output voltage, while the voltage reference of the lower chain link is the subtraction between the DC source voltage value and the flying capacitor voltage. During the N state, the upper chain link voltage reference is the flying capacitor voltage, while the lower chain link voltage reference is the sum of half the DC source voltage and the MMC output voltage. The upper and lower chain links are the voltage shapers for the output voltage during the P and N state.

$$\begin{cases} v_{paF} = \frac{1}{2}V_{dc} - v_a, v_{naF} = V_{dc} - v_{FCa} & (\text{P state}) \\ v_{naF} = v_{FCa}, v_{paF} = \frac{1}{2}V_{dc} + v_a & (\text{N state}) \end{cases} \quad (3.11)$$

3.7 Chain Link Control

The voltage references are calculated with the following Equation 3.12:

$$\begin{cases} v_{paR} = v_{paF} - v_{paD} & (\text{P state}) \\ v_{naR} = v_{naF} - v_{naD} & (\text{N state}) \end{cases} \quad (3.12)$$

After per-unitization, the voltage references v_{paR} and v_{naR} are transferred to the modulation index to determine how many submodules from an arm should be inserted. The standard MMC modulator and sorting algorithms are used here to control the chain links, thus further detailed control algorithms are not illustrated in this section [17].

Chapter 4

FC-HMMC with Thyristor Valve

The purpose of this chapter is to analyze the performance of the thyristor valve and to propose corresponding solutions. Section 4.1 introduces the characteristics of the thyristor, including its V-I curve. Section 4.2 analyzes the causes of commutation failure while using thyristors. Finally, Section 4.3 presents a solution aimed at resolving this issue without introducing significant current ripple.

4.1 Thyristor Characteristic

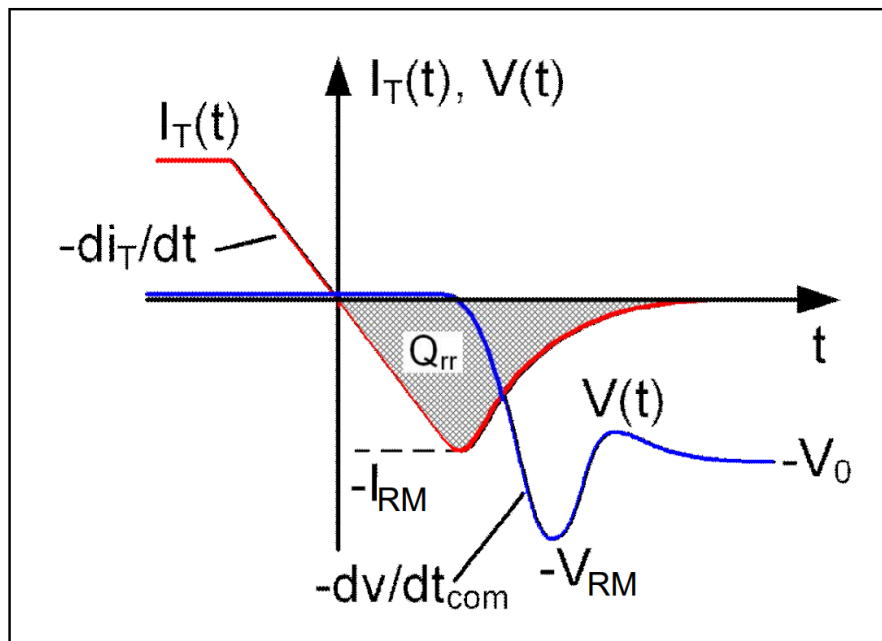
In thyristors, if a forward voltage is reapplied immediately after the forward anode current in a unidirectional thyristor is ceased, the device may unintentionally re-enter the conduction state [18]. This is due to the presence of residual charge carriers within the device structure. To ensure proper blocking of the reapplied forward voltage, a defined interval—known as the turn-off time—must elapse. This interval allows sufficient time for the removal of excess charge carriers from all regions of the p-n-p-n structure.

In many practical applications, the forward current is interrupted by a reversal of current by an external circuit. As the anode current decreases, it passes through zero and becomes negative. This reverse current initially peaks and then decays, facilitating the removal of stored charges and the re-establishment of the depletion region across the reverse-blocking junction. Only after this process is completed, thyristor can reliably block forward voltage.

A thyristor can be turned off not only by applying a reverse voltage but also by opening the external circuit or applying a reverse bias to the gate terminal. The fastest turn-off is achieved when the anode current is reversed

simultaneously with the application of a reverse gate current [18]. Initially, when only the anode current is reversed, the two outer junctions—previously forward-biased during conduction—become reverse-biased. The addition of a reverse gate current further accelerates charge removal, thereby reducing the overall turn-off time.

For demonstration purposes, a phase-controlled thyristor from Hitachi Energy [19] is selected to illustrate the voltage-current (V-I) characteristics during the turn-off process, as shown in Figure 4.1.



Current and voltage waveforms at turn-off

Figure 4.1: Thyristor V-I curve from Hitachi Energy thyristor datasheet [19]

When a positive voltage is applied across the thyristor and a gating signal is present, the device enters the conduction mode and behaves like a low-resistance switch, often referred to as being in the “on-state.” In this state, the thyristor conducts current similarly to a resistor, then reaches maximum conducting current and experiences a voltage drop. To turn off the thyristor, the gating signal must be removed first. Subsequently, a reverse voltage must be applied to force a negative current through the device. This reverse current is essential to fully clear the internal charge carriers and restore the thyristor to its blocking state. The quantity of charge that must be removed during this

process is represented by the shaded area in Figure 4.1.

4.2 Problem with Thyristor Turn-off in FC-HMMC

To enable the replacement of IGBTs with thyristors in the FC-HMMC circuit, it is essential to analyze the voltage and current characteristics of the switching devices during normal operation. Based on the synthesis control strategy described in Chapter 3.4, the voltage and current waveforms of the switches are examined to assess their suitability for thyristor implementation. These waveforms are illustrated in Figures 4.2 and 4.3, respectively.

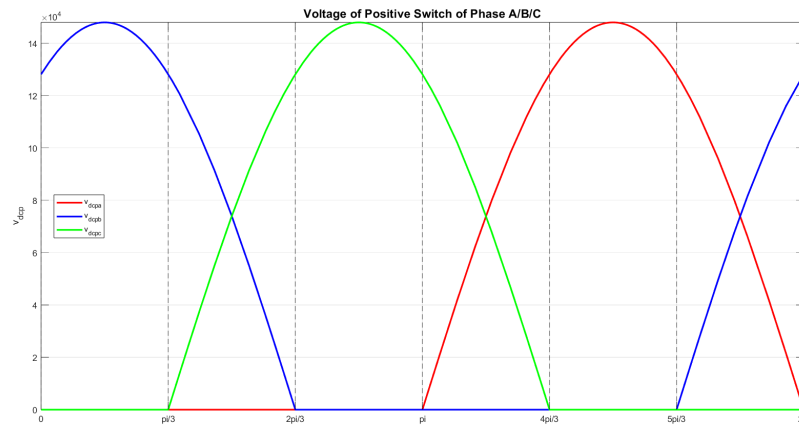


Figure 4.2: Synthesized switch voltage

Under normal operating conditions in inverter mode, both the phase voltages and phase currents remain positive. This indicates that there is no natural occurrence of reverse voltage or reverse current in the circuit. As a result, it is not possible to turn off the thyristors inherently, since thyristor commutation relies on the presence of reverse bias and negative current to fully extinguish conduction. Therefore, an external commutation strategy must be employed to ensure proper turn-off of the thyristors in this mode of operation.

4.3 Synthesize Control Modification

Based on the synthesis control strategy described in Chapter 3, Section 3.4, the core idea is to divide the output current into two distinct components. The first

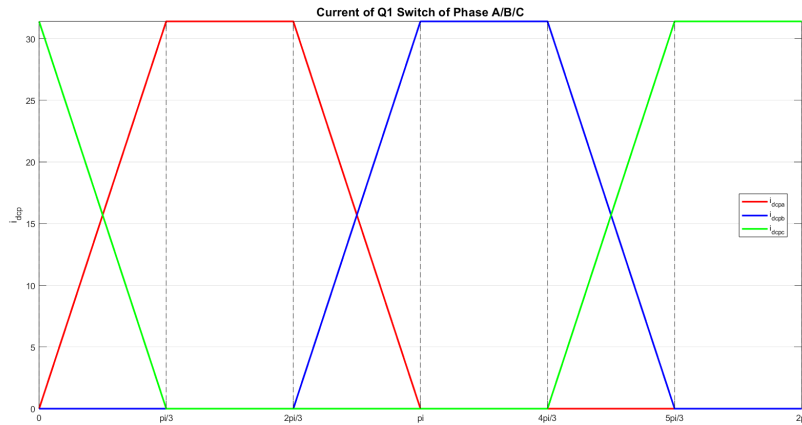


Figure 4.3: Synthesized switch current

component flows through the flying capacitor, while the second flows through the switching devices. The current through the switches is regulated by either the upper or lower chain link, depending on whether the converter is operating in the P or N state. Meanwhile, the current through the flying capacitor is distributed according to the designed control strategy, ensuring proper energy balancing and voltage regulation across the converter.

Taking one phase as an example, when the FC-HMMC operates in inverter mode, the phase current remains positive under normal conditions. In this scenario, the thyristor cannot turn off naturally during state transitions, as there is no reverse current or voltage to facilitate commutation. However, by redesigning the synthesized switch current waveform to include a brief negative current component, it becomes possible to force the thyristor to turn off. Since the current regulator is integrated into the control system, the chain link control block will respond by generating a modified voltage reference to track the new current reference produced by the adjusted synthesis control. Based on this concept, a new synthesized waveform can be designed to intentionally introduce a negative current interval, enabling controlled turn-off of the thyristor.

At the end of the switch's conduction period, a negative current bias is introduced into the synthesized current reference to generate a brief reverse current, enabling the turn-off of the thyristor, which is shown in the Figure 4.4. The duration of this turn-off interval, denoted as D_{thy} , is determined based on the specifications provided in the datasheet of the selected thyristor. The amplitude of the negative bias, denoted as M , is chosen to account for the

worst-case operating condition—specifically, when the power angle between voltage and current reaches ± 90 . Since the control system operates in per-unit (p.u.) values, a value of $-1.2p.u.$ is selected to ensure sufficient reverse current is generated for reliable thyristor turn-off.

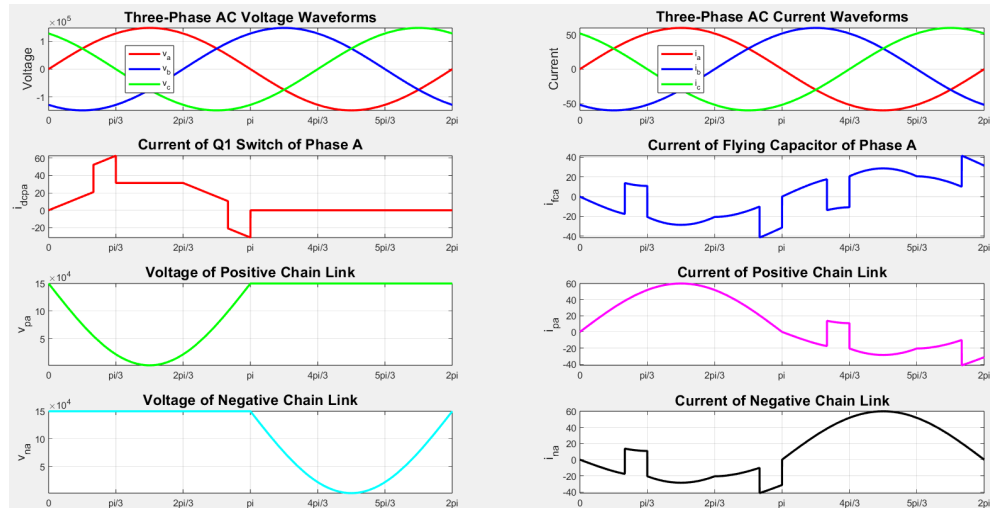


Figure 4.4: Synthesize control with thyristor

In Chapter 2, Section 2.3, there are three operating states in which the DC-side current is the sum of two phase currents. Taking phases A and B as an example, the DC-side current in these states can be expressed by Equation 4.1.

$$I_{dcp} = I_{dcpa} + I_{dcpb} \quad (4.1)$$

Based on the previous discussion, a trapezoidal-shaped current is employed to maintain a constant DC-side current, thereby minimizing current and voltage ripple, this is shown in the Figure 4.5. If the bias is applied only at the end of the thyristor conduction period, a significant current spike occurs on the DC side, necessitating a large filter to suppress the resulting ripple. To directly compensate for this ripple, an opposite current of same magnitude is introduced in another conducting phase for the same duration, denoted as D_{thy} , at the end of the first thyristor conduction segment. This approach ensures that the total dc current remains balanced, allowing the use of a smaller filter to eliminate minor spikes.

With the modified synthesized control algorithm, the thyristor replacement can be achieved.

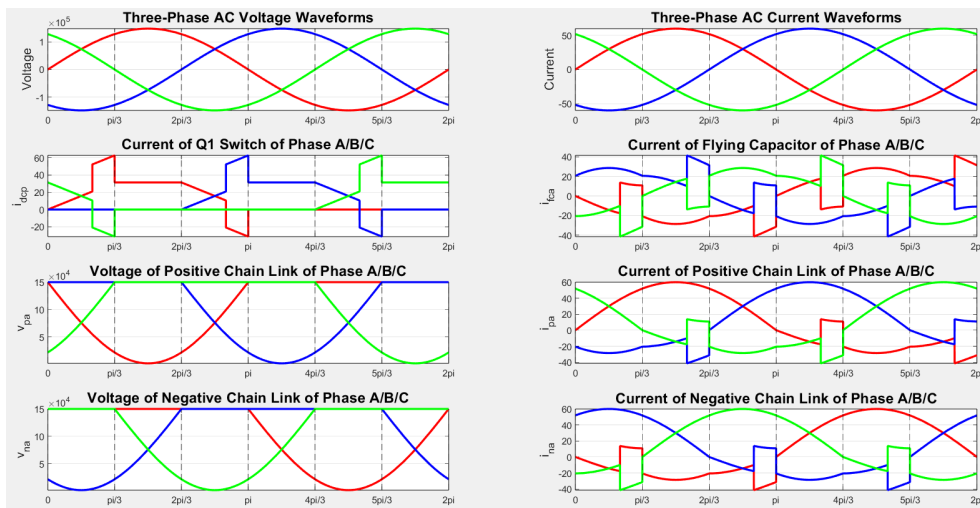


Figure 4.5: Synthesize control with thyristor in three phases

Chapter 5

FC-HMMC Simulation Model

This chapter provides a comprehensive demonstration of the simulation model developed using PSCAD. Chapter 5.1 offers a brief introduction to PSCAD and explains the rationale behind selecting this software for the study. Chapter 5.2 presents the detailed circuit model implemented in PSCAD, along with the corresponding parameters. Finally, Chapter 5.3 describes the control model in detail, illustrating how complex systems can be constructed and simulated within the PSCAD environment.

5.1 Introduction About PSCAD

Power Systems Computer Aided Design (PSCAD) is a widely used simulation software designed for the analysis of power system transients, which is particularly well-suited for studying electromagnetic transients in power systems, making it an essential tool for research and development in areas such as High Voltage Direct Current (HVDC) transmission, Flexible AC Transmission Systems (FACTS), renewable energy integration, and protection system design. Its ability to simulate detailed switching operations, control strategies, and nonlinear system behavior allows engineers and researchers to evaluate system performance under a wide range of operating conditions.

The software includes an extensive library of components, including power electronic devices, transformers, transmission lines, control blocks, and measurement tools. These components can be easily configured and interconnected within the graphical environment to build detailed system models. Additionally, PSCAD supports user-defined models and control logic through its embedded FORTRAN-based scripting environment, offering further customization and control.

In the context of this thesis, PSCAD is employed to model and simulate the proposed HVDC system. The software's capabilities are leveraged to analyze system dynamics, validate control strategies, and evaluate performance under various fault and load conditions. The following sections will detail the simulation setup, modeling approach, and key results obtained using PSCAD.

5.2 FC-HMMC Circuit Model on PSCAD

In this section, the detailed simulation model of the FC-HMMC circuit is presented. The discussion includes the construction of each circuit component and the specification of its respective parameters.

5.2.1 AC Grid Source

A three-phase symmetric AC voltage source shown in the Figure 5.1 is used in the circuit model, characterized by a line-to-line RMS voltage magnitude V_{ll} and a frequency f_{ac} . Each phase is connected in series with an inductor L_{ac} to represent the source impedance. Additionally, the voltage source includes a ramp-up time t_{ac} , during which the output voltage gradually increases from zero to its rated value.

Table 5.1: Grid source parameters

Parameters	Value
V_{ll}	387 kV
f_{ac}	50 Hz
L_{ac}	20 mH
t_{ac}	0.05 s

5.2.2 YnD Connection Transformer

A YnD transformer (also known as the star-delta transformer) is used in the model, which offers several key benefits, primarily in harmonic suppression and improving power quality. The delta winding connection prevents harmonic currents from propagating into the connected grid and causing issues

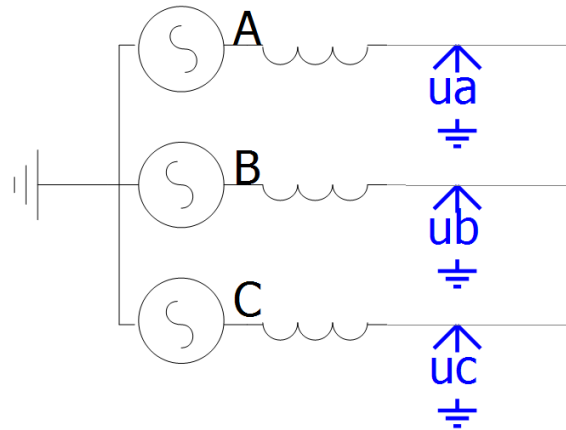


Figure 5.1: Three phase AC grid source

for other equipment. The secondary side of the transformer is connected to the AC grid, while the primary side is connected to the converter. The transformer is rated with a secondary-side voltage of V_{grid} and a primary-side voltage of V_{mmc} . It operates at the system frequency f_{ac} . And the core reactance of the transformer is named L_{tr} .

Table 5.2: Transformer parameters

Parameters	Value
V_{grid}	387 kV
V_{mmc}	181 kV
L_{tr}	0.2 pu
f_{ac}	50 Hz

5.2.3 Converter Switch

The switch block is illustrated in Figure 5.3, with the control signal shown on the left side and the corresponding circuit on the right. All switches remain in the blocked state before 0.1 seconds. After this point, they are controlled by the specified input signal. For simplification, both the thyristor and IGBT model have the same parameters, which are forward breakover voltage V_s , on-state resistance R_{on} , off-state resistance R_{off} , except the thyristor has the minimum

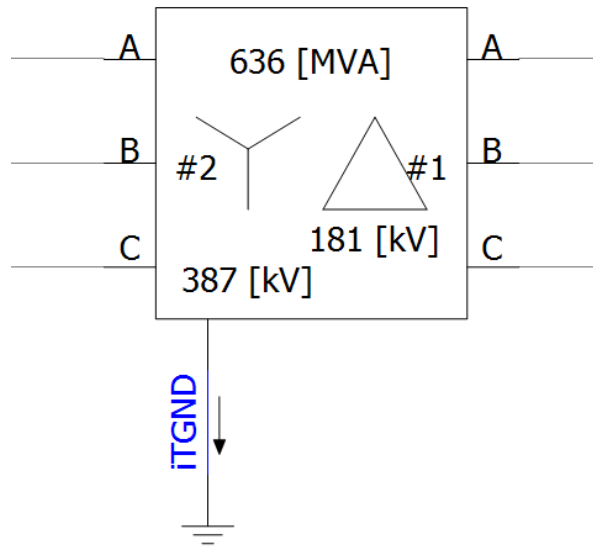


Figure 5.2: Transformer model

extinction time t_q . Either the thyristor or IGBT is inserted in the circuit to test the difference and keep others the same.

Table 5.3: Switch parameters

Parameters	Value
V_s	200 kV
R_{on}	$1 \times 10^6 \Omega$
R_{off}	$1 \times 10^{-2} \Omega$
t_q	0.7 ms

5.2.4 Flying Capacitor

The flying capacitor is shown in the Figure 5.4, with the capacitor value C_{fc} and rated voltage value V_{fc} . Since the startup process of the FC-HMMC is not the focus of this thesis, the flying capacitor is initially connected in parallel with an ideal voltage source having the same rated voltage as the capacitor. A breaker is closed during the first 0.05 seconds to allow the capacitor to charge to its rated value, after which the breaker is opened. This approach ensures

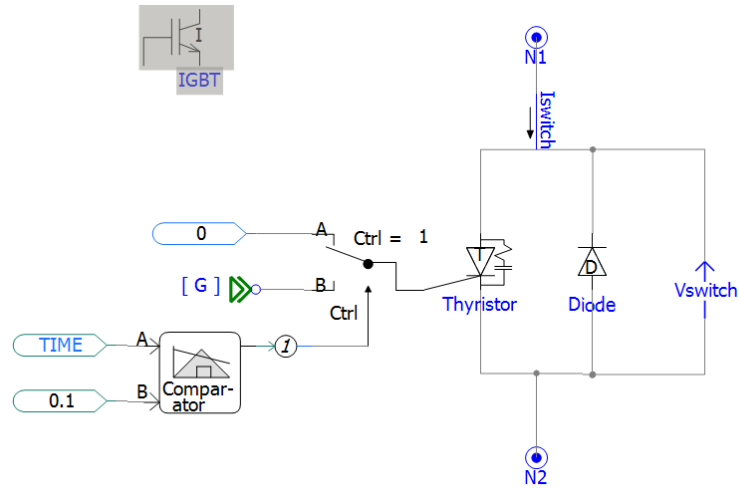


Figure 5.3: Semiconductor switch and its control blocks

that the converter operates under normal steady-state conditions, eliminating the need to model the startup charging process.

Table 5.4: Flying capacitor parameters

Parameters	Value
C_{fc}	0.416 mF
V_{fc}	150 kV

5.2.5 Chain Links

The upper and lower chain links are identical in circuit, therefore, only one chain link is selected for demonstration. Each chain link consists of twelve submodule cells N_{cl} , as illustrated in Figure 5.5. Each submodule cell is characterized by a capacitance C_{cl} and a rated voltage V_{cl} . Similarly the submodule capacitor is charged by an ideal voltage source in the first 0.05 seconds.

The arm inductor and arm resistance are connected in series with submodules. The arm inductance value is L_{arm} , and arm resistance value is R_{arm} . The connection is shown in the Figure 5.6.

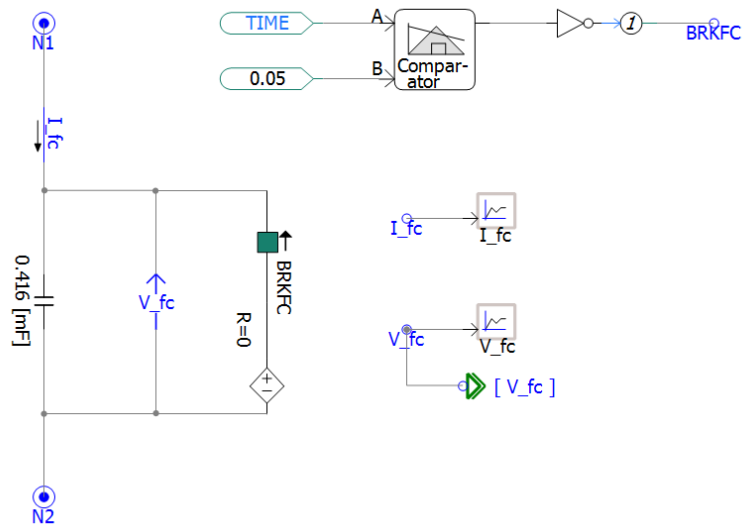


Figure 5.4: Flying capacitor block

Table 5.5: Submodule parameters

Parameters	Value
C_{cl}	5 mF
V_{cl}	15 kV
N_{cl}	12

Table 5.6: Chain link parameters

Parameters	Value
L_{arm}	30 mF
R_{arm}	0.204 Ω

5.2.6 DC Source Filter

As discussed in Chapter 4, the modified synthesized control introduces current spikes. To mitigate these spikes, a DC-side filter, shown in Figure 5.7, is implemented between the DC equivalent source and the MMC converter. This filter is designed to smooth out the current waveform and suppress high-

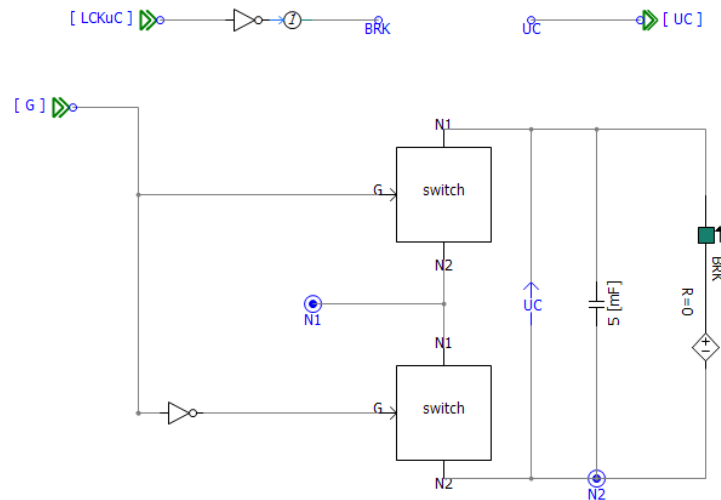


Figure 5.5: Submodule

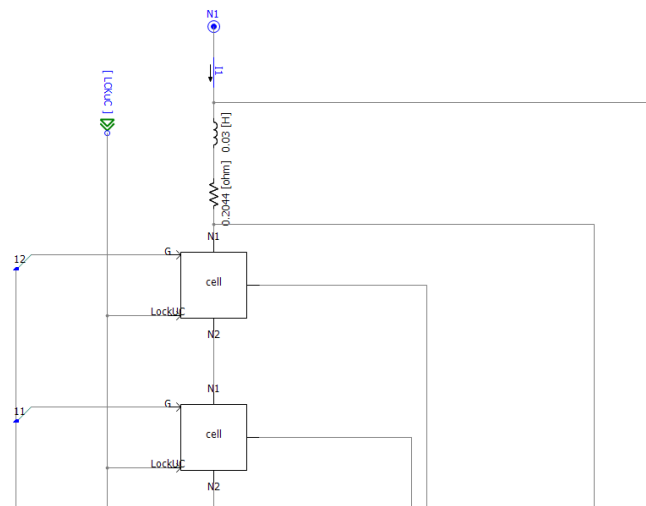


Figure 5.6: Chain link

frequency components caused by the control strategy. The DC filter capacitor C_{ft} is similarly precharged using a DC source and breaker, and the reactor inductance is L_{ft} .

5.2.7 DC Source

The ideal DC source is connected to the filter, and its voltage amplitude is V_{dc} , as shown in Figure 5.8.

Table 5.7: DC filter parameters

Parameters	Value
L_{ft}	20 mH
C_{ft}	1 mF

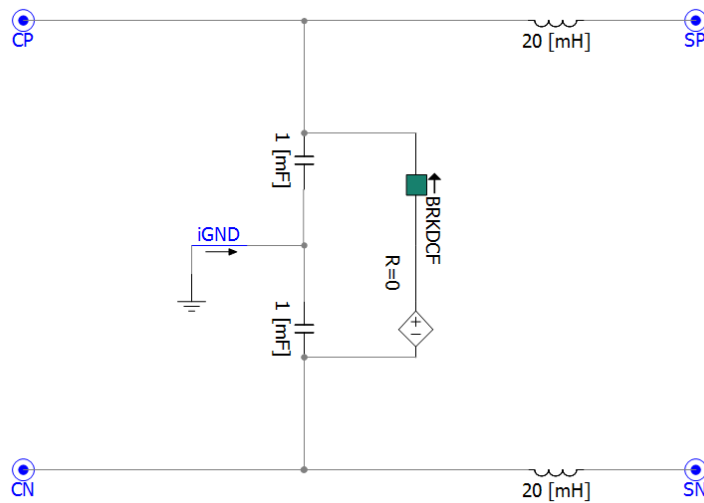


Figure 5.7: DC source filter

Table 5.8: DC source parameters

Parameters	Value
V_{dc}	300 kV
Power Rating	300 MVA

5.3 FC-HMMC Control Model On PSCAD

5.3.1 Switch Control

The core component of the control block is the switching logic for the three phases, as illustrated in Figure 5.9. In this block, the voltages of all three phases are first fed into a Phase-Locked Loop (PLL) controller, which tracks

5.3.2 Capacitor Voltage Control

The capacitor voltage control block shown in Figure 5.10 is based on the methodology described in Chapter 3, Section 3.2. In this control scheme, the voltages of the upper chain link, lower chain link, and flying capacitor are compared against their respective reference values. The resulting error signals are fed into PI controllers, which generate the amplitude of the trapezoidal waveform used for synthesis. It is important to note that the current flowing through all three components introduces voltage ripple that cannot be effectively compensated directly. To address this, a low-pass filter is applied to extract the DC component of each voltage signal. This filtered value is then used for comparison with the reference, ensuring stable and accurate control.

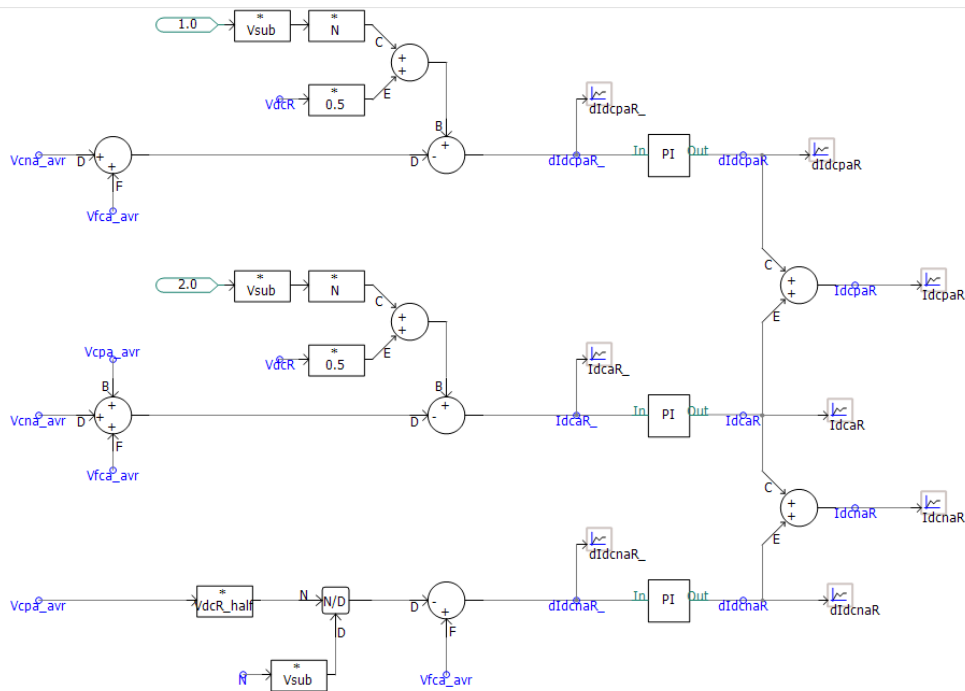


Figure 5.10: Capacitor voltage control

5.3.3 AC Power Control

As described in Chapter 3, Section 3.3, the power reference is generated by the control block shown in Figure 5.11. It is important to note that at the beginning of the simulation, the grid voltage amplitude starts from zero. This can lead to extremely large or undefined values during the d-q transformation. To avoid

this issue, the initial short period is ignored. After this transient phase, the measured values are used to generate the voltage amplitude reference for the three phases.

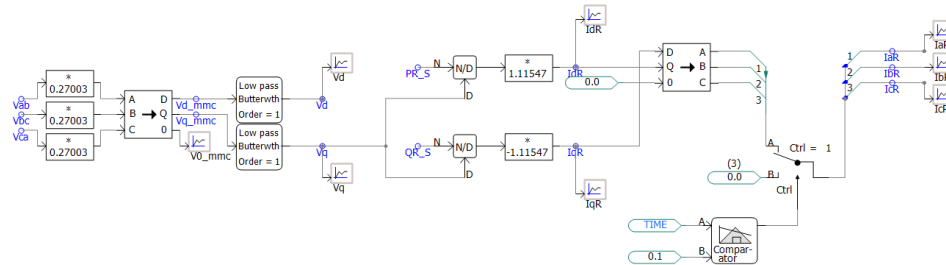


Figure 5.11: AC power control

5.3.4 Synthesize Control

The synthesized control method is presented in Chapter 3, Section 3.4, and its implementation in PSCAD is illustrated in Figure 5.12. A custom function block is defined within PSCAD, where the corresponding control algorithm is embedded. The source code for this function is provided in Appendix B.1 and B.2. Using this implementation, the appropriate voltage reference signals are generated and passed to the subsequent control blocks. A simplified flowchart illustrating the operation of the synthesized code is presented in Figure 5.13.

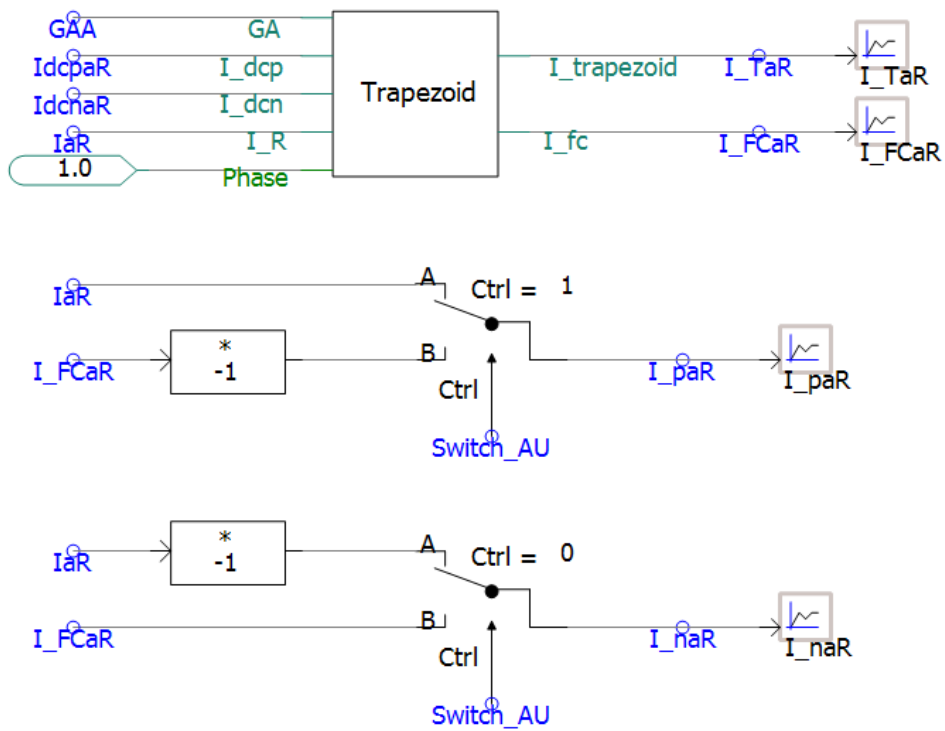


Figure 5.12: Synthesize control

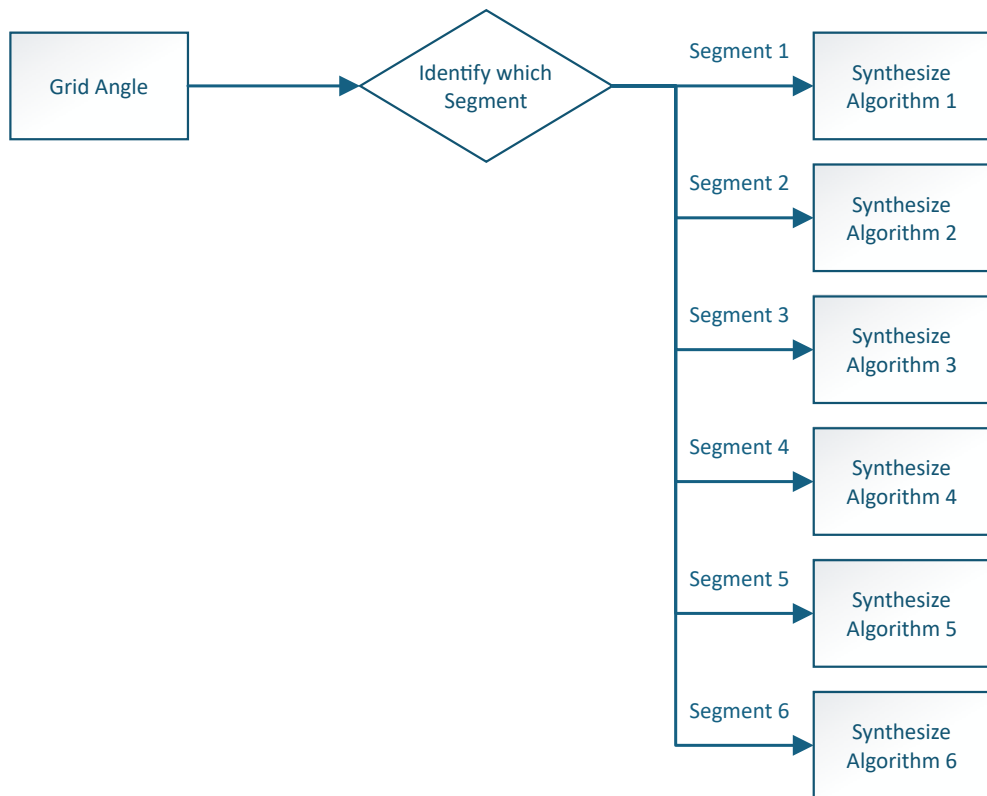


Figure 5.13: Director switches and chain links synthesis code flow chart

5.3.5 Other Control Parts

- Arm voltage forward
- Current regulator
- Chain link voltage reference

These three control blocks are based on straightforward mathematical calculations derived from the corresponding equations in the Chapter 2. Therefore, a detailed demonstration of implementation in PSCAD is not necessary.

Chapter 6

FC-HMMC Results and Analysis

As previously discussed, thyristors naturally turn off in rectifier mode, eliminating the need for simulation verification in that operating condition. Therefore, this chapter focuses on simulations conducted in inverter mode with thyristor replacement, with the results presented and analyzed accordingly. Section 6.1 presents two steady-state test cases in inverter mode, illustrating the corresponding current and voltage data. Section 6.2 analyzes a dynamic scenario in which the power reference increases to 300 MW. Lastly, Section 6.3 investigates the same steady-state conditions, but with the replacement of IGBTs by thyristors, allowing for a comparative analysis.

6.1 FC-HMMC Steady State Performance

Two case studies are presented in this section: one with an active power reference of $P=300$ MW and a reactive power reference of $Q=0$ MVar and another with an active power reference of $P=300$ MW and a reactive power reference of $Q=100$ MVar. Both cases operate in inverter mode.

6.1.1 $P=300$ MW, $Q=0$ MVar

When the FC-HMMC operates under steady-state conditions with an active power reference of 300 MW and a reactive power reference of 0 MVar, the system reaches steady state after approximately 2 seconds. As shown in Figure 6.1 and Figure 6.2, the actual power transferred from the DC side to the AC grid is approximately 290.5 MW of active power and 2.3 MVar MVar of reactive power. The steady-state error existed in the converter, and further fine-tuning should be achieved to reach zero steady-state error.

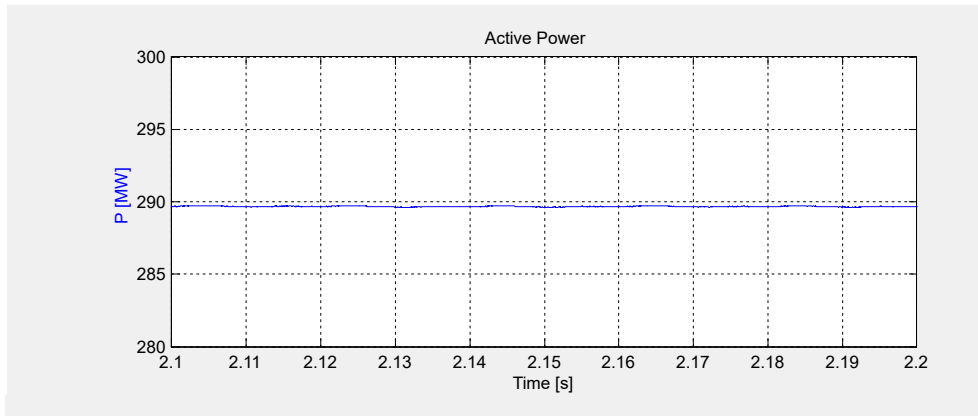


Figure 6.1: Waveform of active power in steady state [MW]

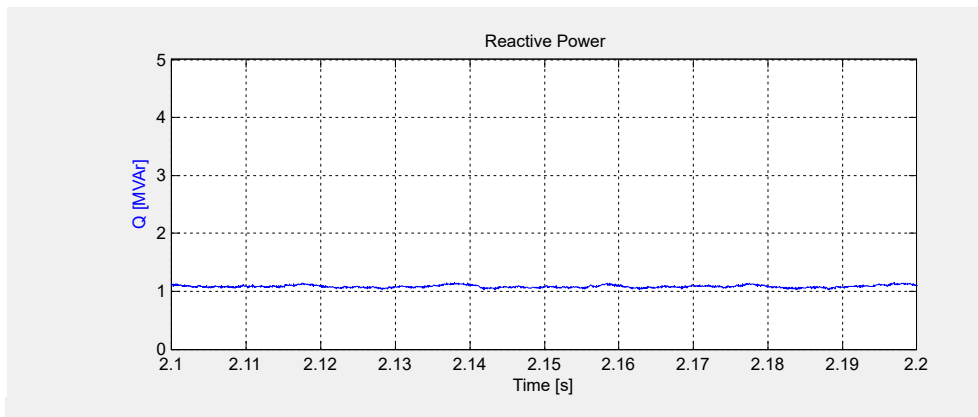


Figure 6.2: Waveform of reactive power in steady state [MVar]

The converter's AC voltage output is shown in Figure 6.3. For each phase, during both the P and N states, the FC-HMMC connects only one chain link between the DC grid and the AC grid, functioning as a voltage shaper. The ripple observed in the AC waveform can be further reduced by increasing the number of submodules in each chain link and by incorporating an AC filter at the converter output.

The upper chain link voltage and current waveforms are shown in Figures 6.4 and 6.5. As designed, the chain-link voltage clearly operates in two distinct states. In the P state, the voltage waveform is sinusoidal, while in the N state, it remains constant at half of the DC source voltage. Similarly, the current waveform also exhibits different characteristics in each state. During the P state, the current corresponds to the output current and follows a sinusoidal shape. In contrast, during the N state, the current is the result of subtracting a

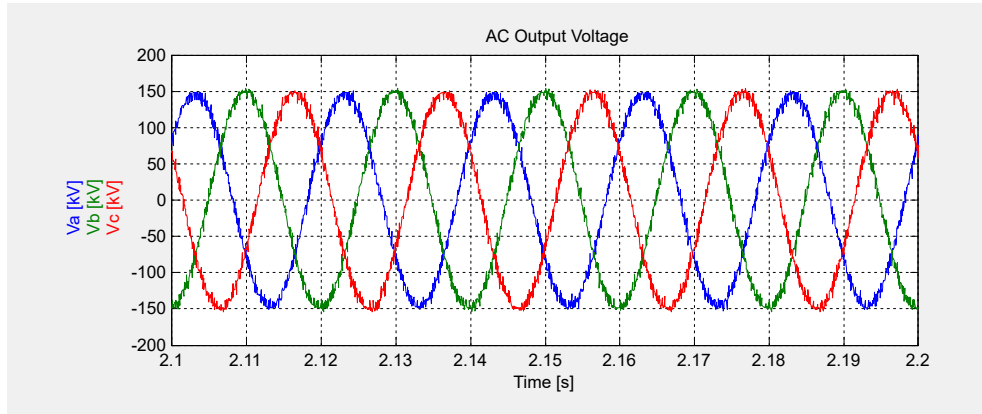


Figure 6.3: Waveform of AC output voltage in steady state [kV]

trapezoidal waveform from the sinusoidal one.

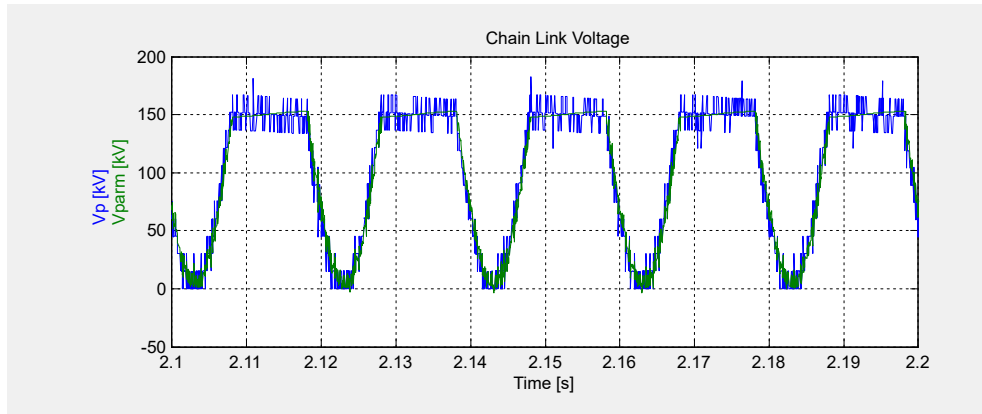


Figure 6.4: Waveform of one phase chain link voltage in steady state [kV] (Green line: Arm voltage, Blue line: Submodules total voltages)

The voltages of the upper submodules are shown in Figure 6.6. By applying sorting control to the submodule control system, the submodule voltages are effectively balanced as intended. The voltage ripple across the submodules ranges from 14.85 kV to 15.2 kV, with a nominal value of 15 kV. This variation remains within the safe operating range of the submodules.

The voltage and current waveforms of the upper switch are shown in Figures 6.7 and 6.8. According to the synthesized design, the voltage waveform should be sinusoidal during the N state, while the current waveform should exhibit a trapezoidal shape during the P state.

The flying capacitor current and voltage are shown in Figure 6.9 and Figure 6.10. During the P state, the flying capacitor current is obtained by subtracting

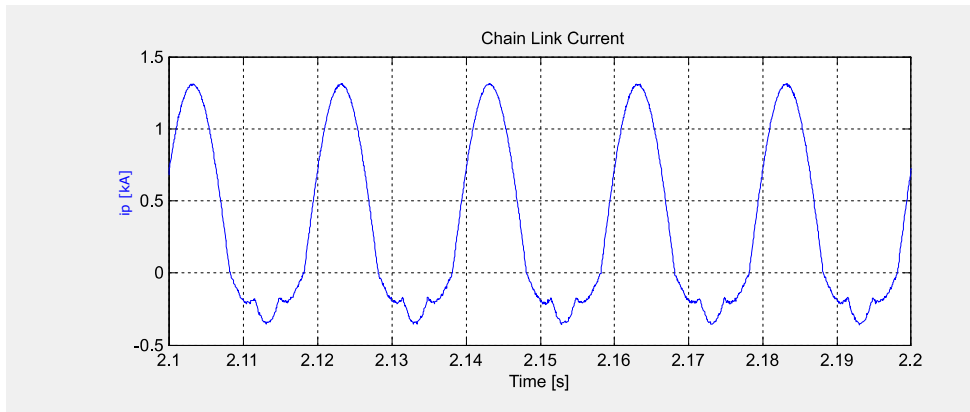


Figure 6.5: Waveform of one phase chain link current in steady state [kA]

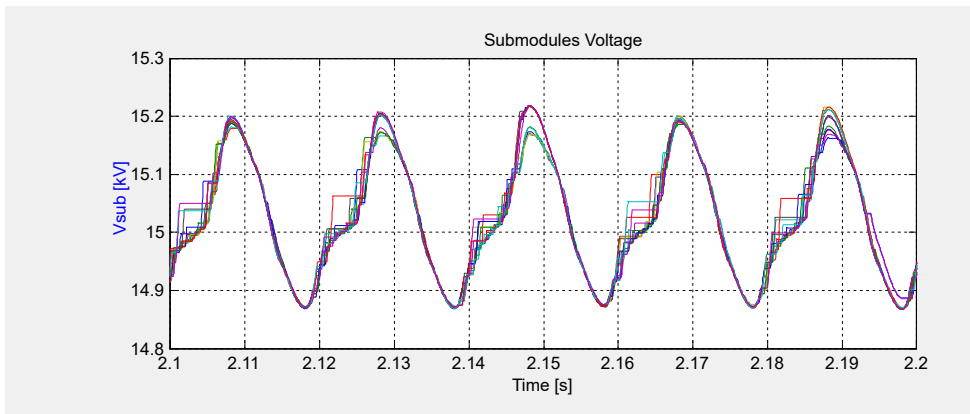


Figure 6.6: Waveform of one phase submodules voltage in steady state [kV]

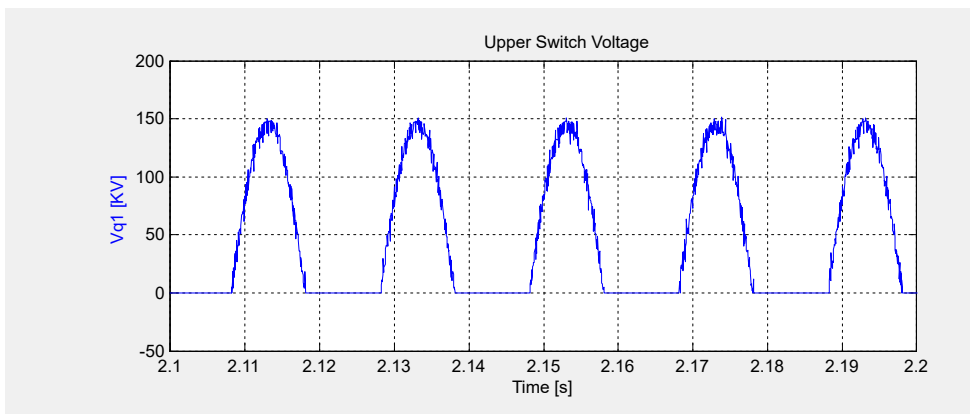


Figure 6.7: Waveform of one phase switch voltage in steady state [kV]

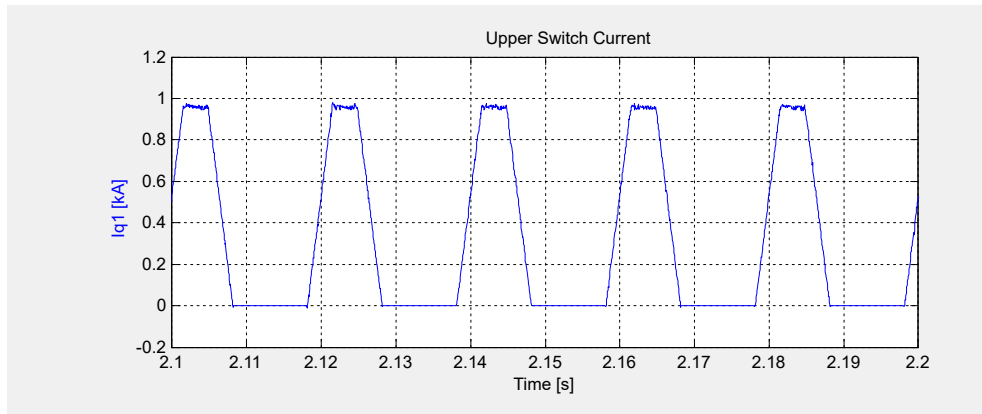


Figure 6.8: Waveform of one phase switch current in steady state [kA]

the upper switch current from the output current. In the N state, it is calculated as the difference between the output current and the lower switch current.

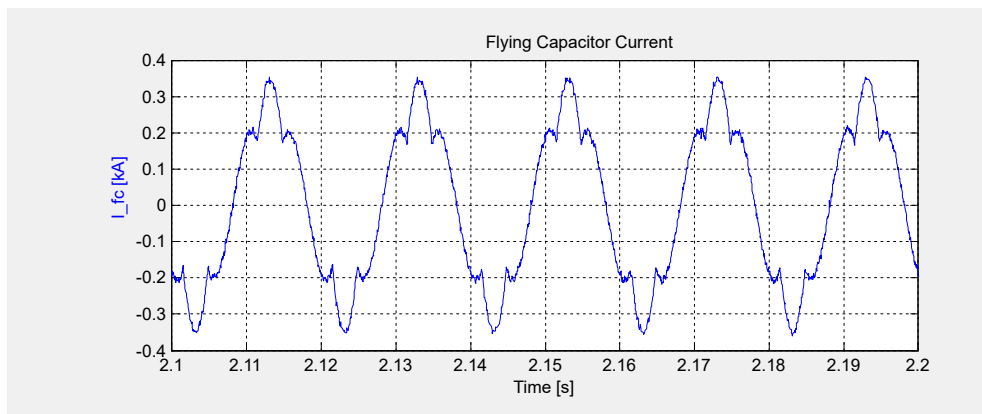


Figure 6.9: Waveform of one phase flying capacitor current in steady state [kA]

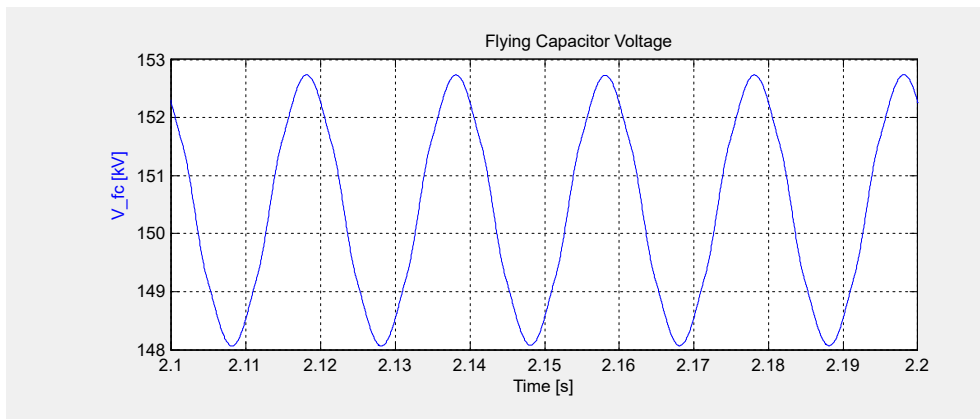


Figure 6.10: Waveform of one phase flying capacitor voltage in steady state [kA]

6.1.2 P=300 MW, Q=100 MVar

Another case, where the active power $P=300$ MW and the reactive power $Q=100$ MVar, is presented in Figures 6.11 and 6.12. From the figures, it can be observed that the converter operates at approximately $P=295$ MW and $Q=101$ MVar.

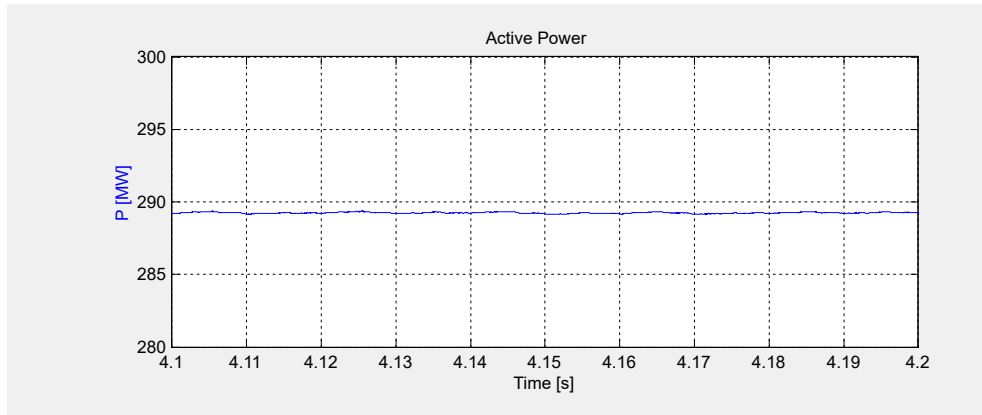


Figure 6.11: Waveform of active power in steady state [MW]

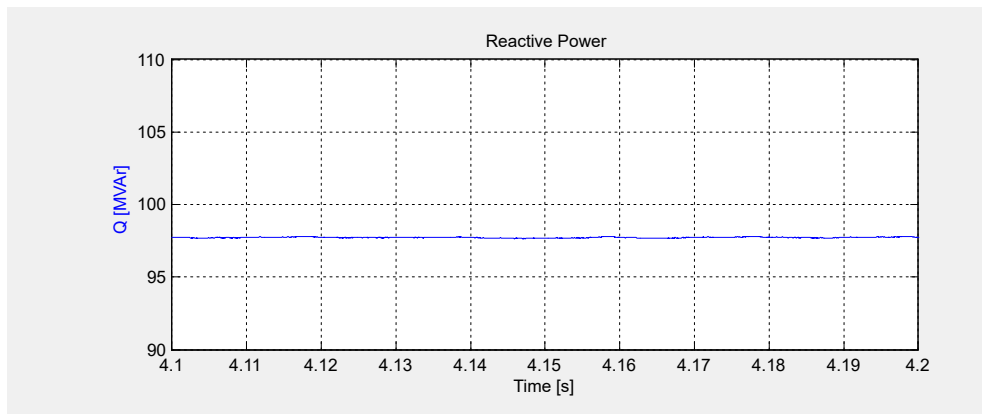


Figure 6.12: Waveform of reactive power in steady state [MVar]

The phase shift between the output voltage and current can be observed in Figure 6.13, where the current waveform lags behind the voltage waveform by approximately 19 degrees.

As a result, the waveforms of the chain-link current and flying capacitor current change accordingly, while the current waveform of the switch maintains its original shape. The chain-link and flying capacitor currents are illustrated in Figures 6.14 and 6.15, respectively.

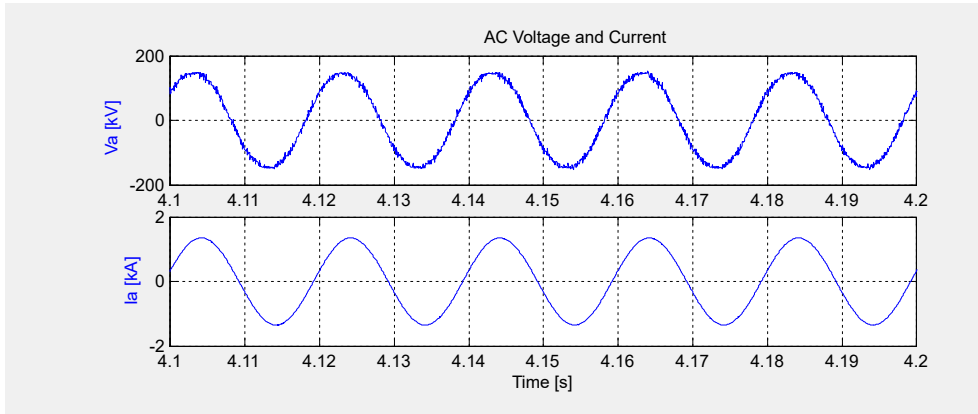


Figure 6.13: Waveform of one phase AC voltage and current in steady state [kA]

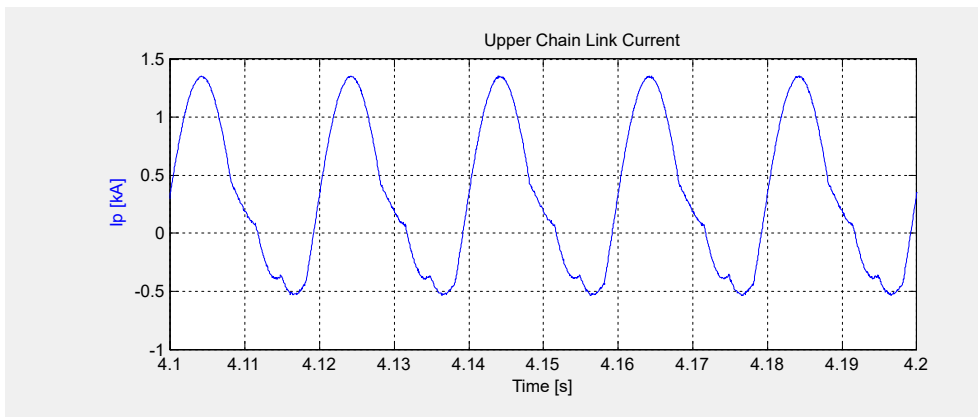


Figure 6.14: Waveform of one phase upper chain link current in steady state [kA]

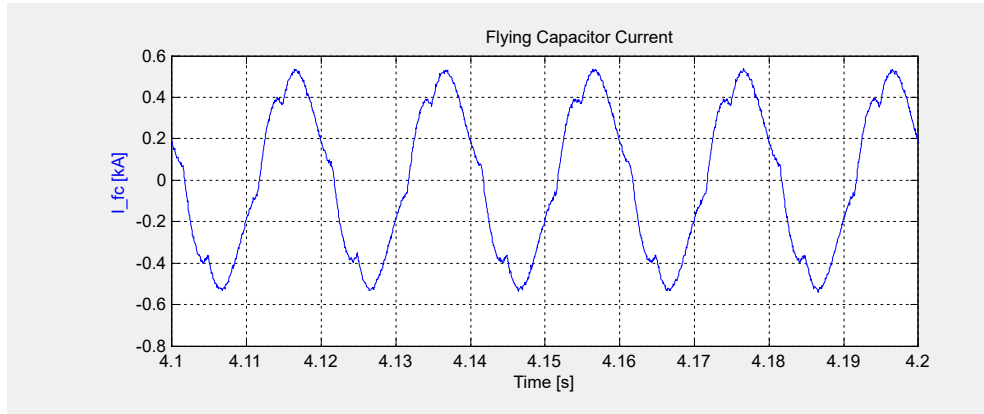


Figure 6.15: Waveform of one phase flying capacitor current in steady state [kA]

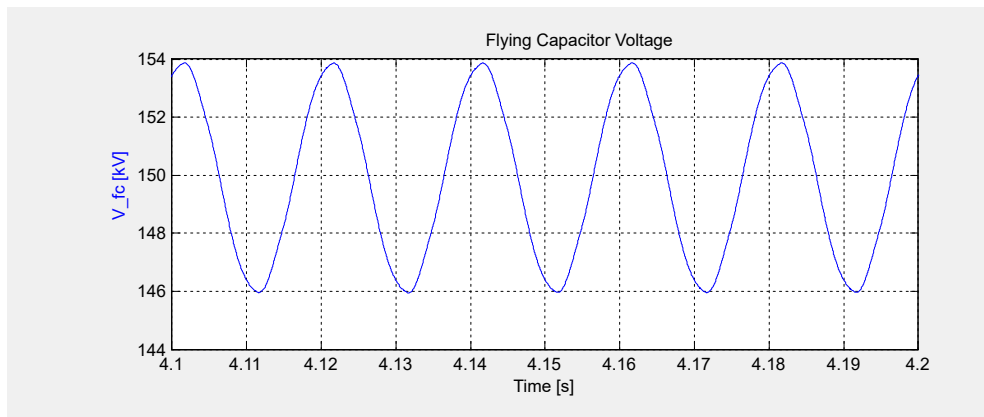


Figure 6.16: Waveform of one phase flying capacitor voltage in steady state [kV]

6.2 FC-HMMC Dynamic Performance

A dynamic case is also presented in this thesis, where the active power reference ramps from 0 MW to 300 MW within 0.5 seconds. This scenario is analyzed using the waveforms of active power, output AC current, switch current, chain-link current, and flying capacitor current, as shown in Figures 6.17, 6.18, 6.19, 6.20, and 6.21. The results demonstrate that the closed-loop control system accurately and steadily tracks the reference signal, with minimal error.

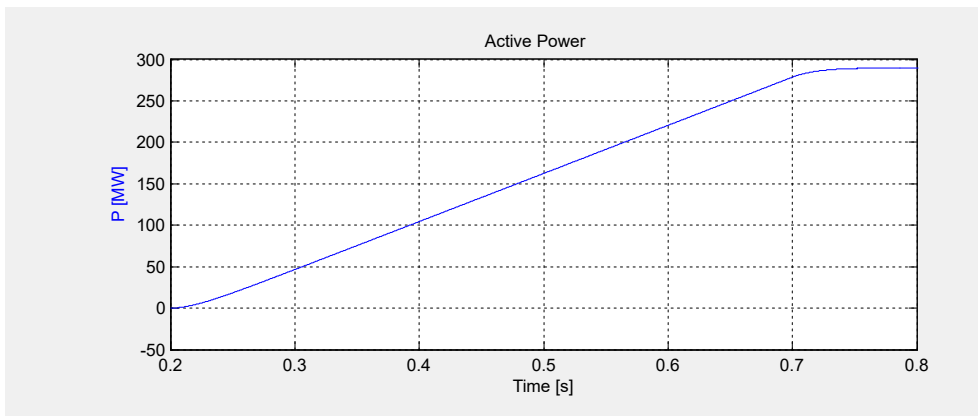


Figure 6.17: Waveform of dynamic active power [MW]

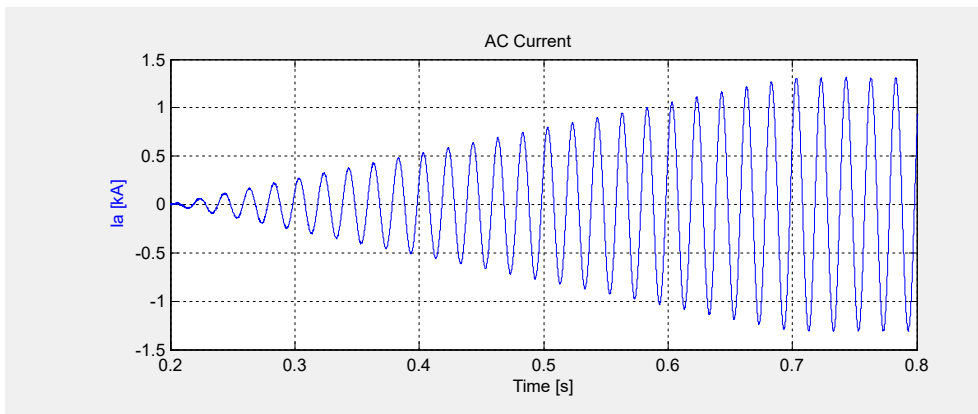


Figure 6.18: Waveform of dynamic AC current [kA]

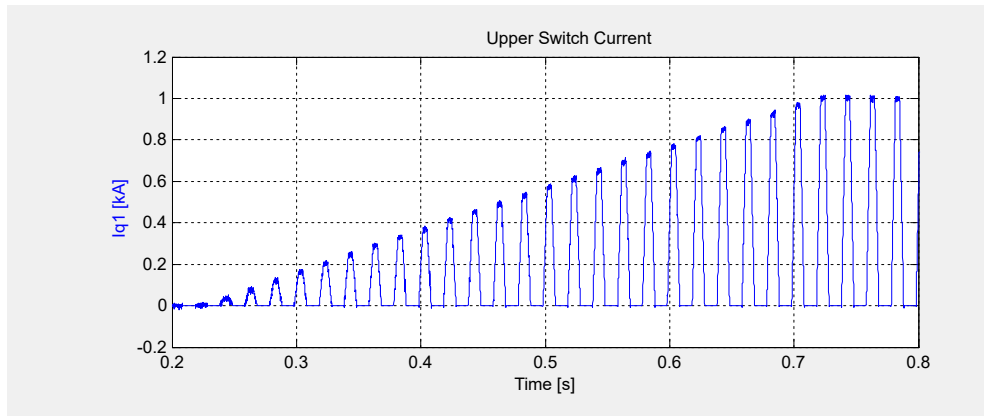


Figure 6.19: Waveform of dynamic switch current [kA]

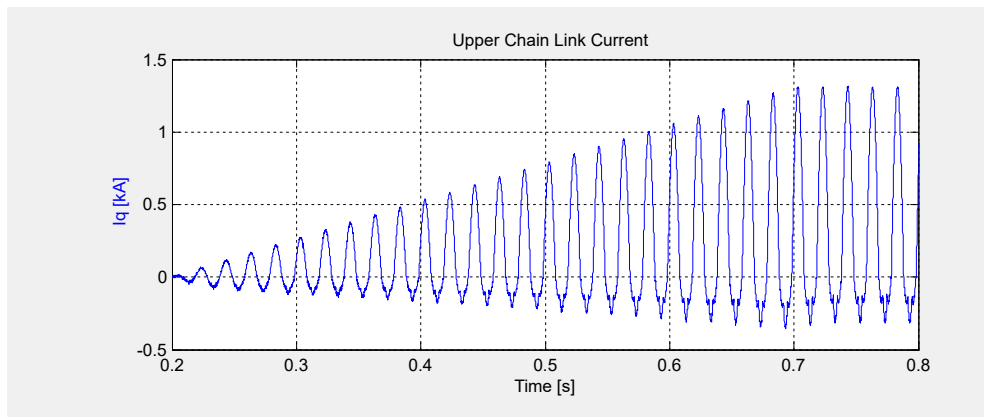


Figure 6.20: Waveform of dynamic chain link current [kA]

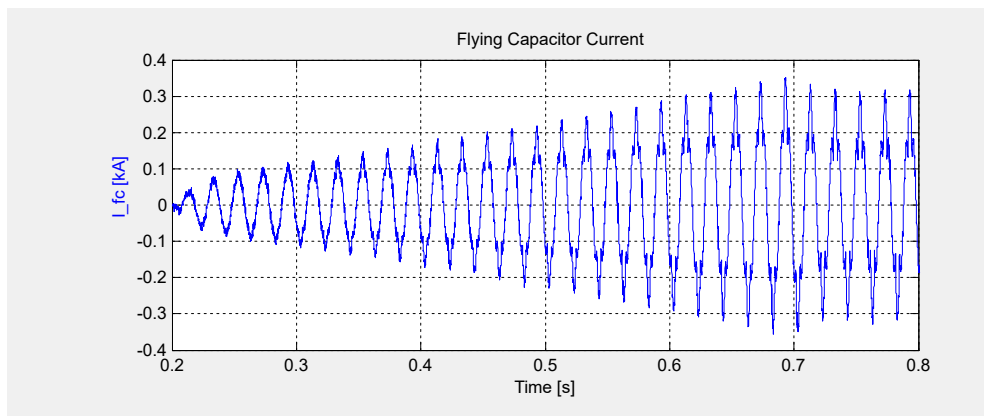


Figure 6.21: Waveform of dynamic flying capacitor current [kA]

6.3 FC-HMMC Steady State Performance with Thyristor

Similarly, two case studies using thyristors are presented in this section with the same settings as those used for the IGBT-based configuration, for comparison purposes. The first case uses an active power reference of $P=300$ MW and a reactive power reference of $Q=0$ MVar, while the second case uses an active power reference of $P=300$ MW and a reactive power reference of $Q=100$ MVar. Both cases operate in inverter mode.

6.3.1 $P=300$ MW, $Q=0$ MVar

This section presents the simulation results of the FC-HMMC system with thyristor replacement. The simulations are conducted under the same power setting of $P=300$ MW, while the reactive power $Q=0$ MVar is maintained to enable a clearer comparison between the thyristor-based and IGBT-based configurations. The active and reactive power profiles are illustrated in Figures 6.22 and 6.23, respectively. As shown in the figure, the actual active power reaches approximately 289 MW, while the reactive power is around 19.9 MVar.

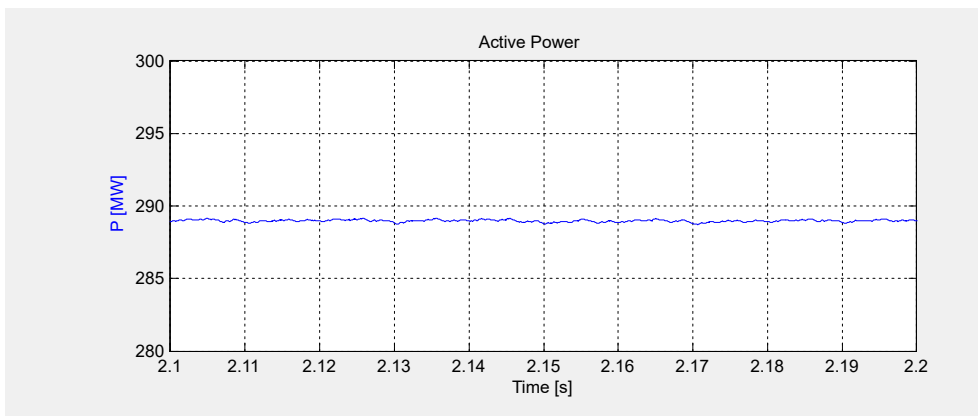


Figure 6.22: Waveform of active power with thyristor in steady state [MW]

The difference between the reference and actual reactive power is primarily attributed to the current modulation required for thyristor turn-off. The voltage and current waveforms of the thyristor in one phase are shown in Figures 6.24 and 6.25. From the current waveform, it can be observed that a bias current is introduced to compensate for the current spike occurring in other

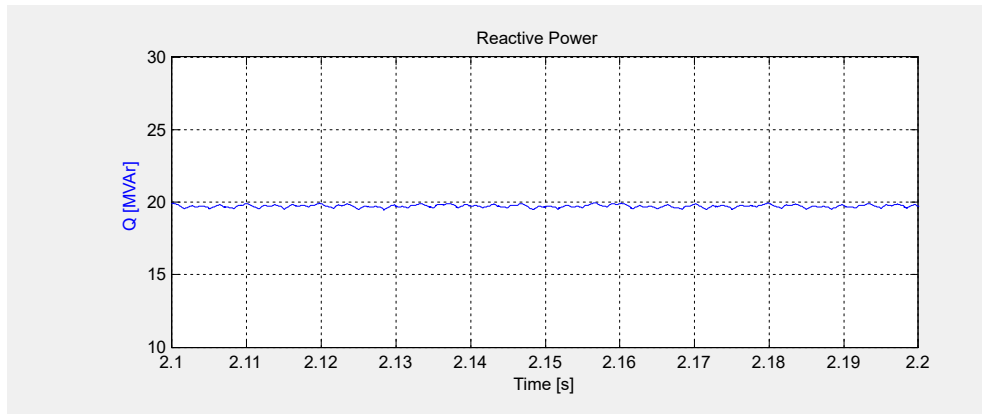


Figure 6.23: Waveform of reactive power with thyristor in steady state [MVAr]

phases during commutation. This bias is subsequently removed at the end of the cycle to facilitate the turn-off of the thyristor. The three-phase current is also shown in Figure 6.26, where the cancellation is designed to decrease the current ripple.

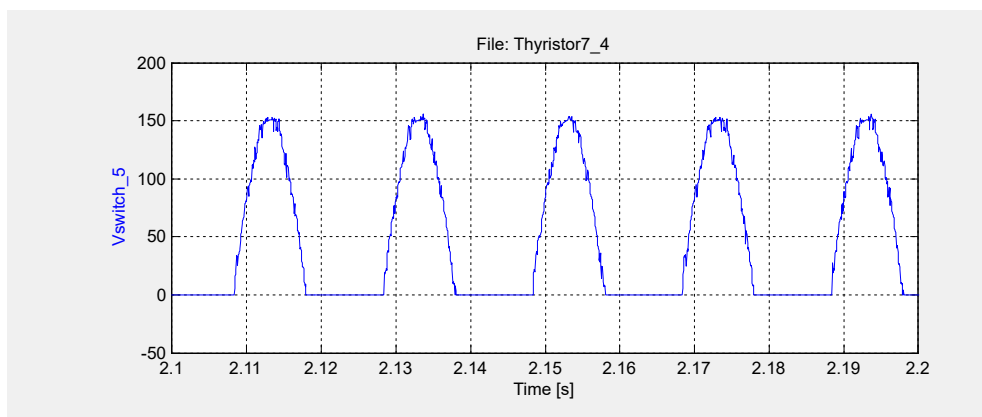


Figure 6.24: Waveform of switch voltage with thyristor in steady state [kV]

The voltages of the upper submodules are shown in Figure 6.27. Similarly, with sorting control applied to the submodule control system, the submodule voltages are effectively balanced as intended. The voltage ripple across the submodules ranges from 14.82 kV to 15.25 kV, and this variation remains within the safe operating range of the submodules.

The current waveform of the chain-link is shown in Figure 6.28. As illustrated, the current varies accordingly to the modified reference current, with a higher current spike meaning that the thyristor should withstand a higher current compared to the IGBT-based. In contrast, the voltage remains constant,

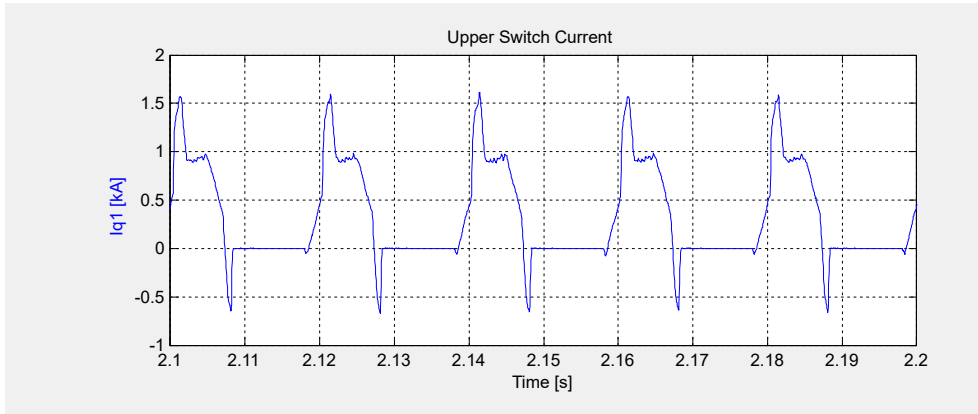


Figure 6.25: Waveform of switch current with thyristor in steady state [kA]

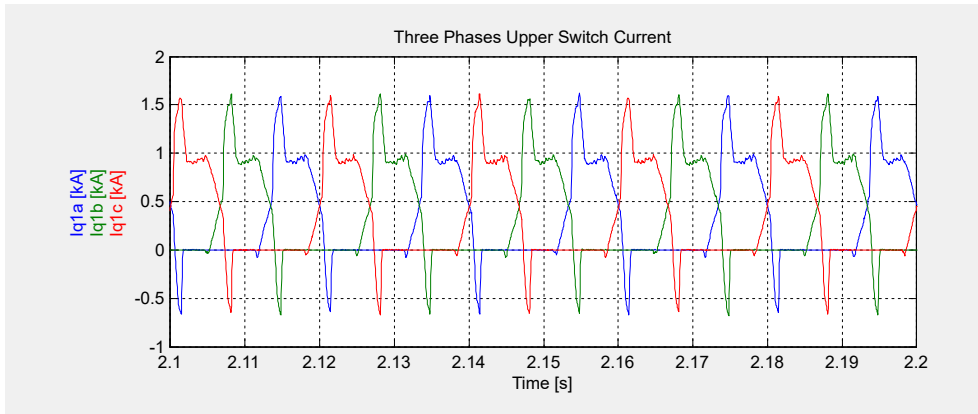


Figure 6.26: Waveform of three-phase switch current with thyristor in steady state [kA]

as the chain-link module functions primarily as a voltage shaper. This behavior is illustrated in Figure 6.29, which presents two waveforms: the blue curve represents the voltage across all submodules, while the green curve shows the voltage across both the submodules and the arm inductance.

The flying capacitor current and voltage are also illustrated in the Figure 6.30 and Figure 6.31. Compared to previous waveforms, the current no longer maintains its original shape and exhibits increased fluctuations. This change is primarily due to the modified synthesis algorithm applied during the simulation.

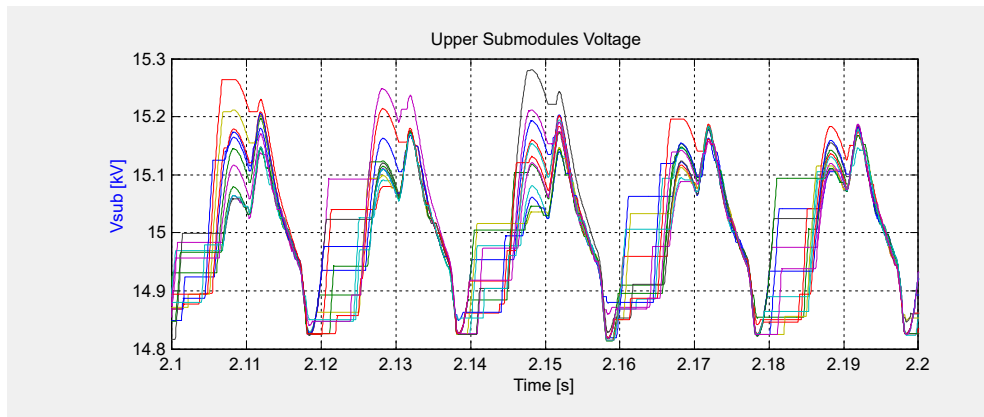


Figure 6.27: Waveform of one phase submodules voltage with thyristor in steady state [kV]

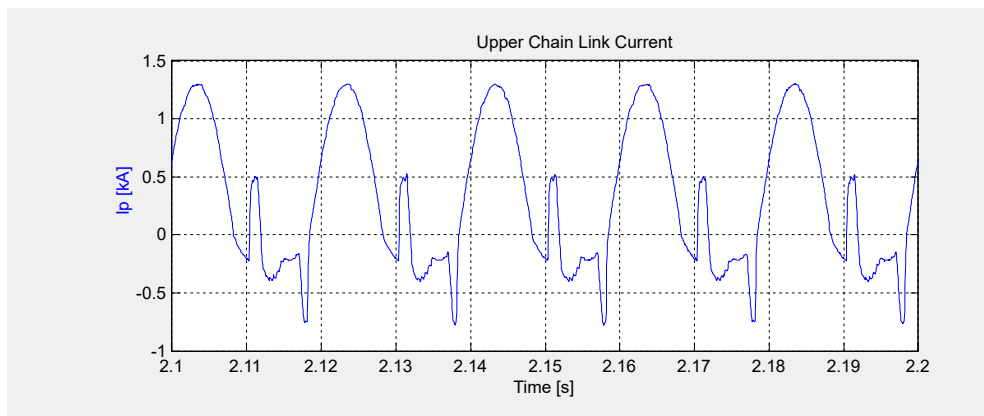


Figure 6.28: Waveform of chain link current with thyristor in steady state [kA]

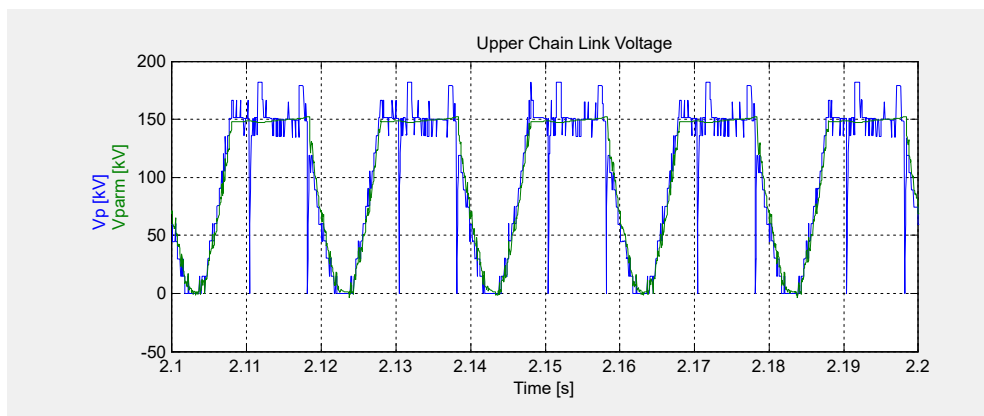


Figure 6.29: Waveform of chain link voltage with thyristor in steady state [kV]
(Green line: Arm voltage, Blue line: Submodules total voltages)

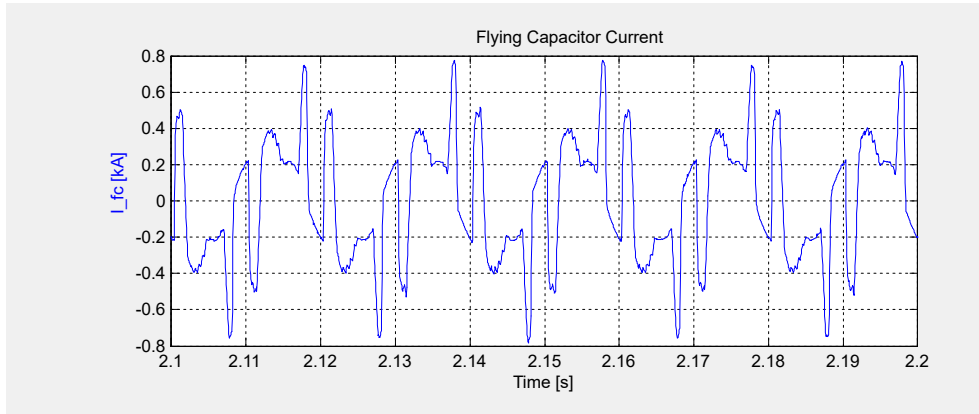


Figure 6.30: Waveform of flying capacitor current with thyristor in steady state [kA]

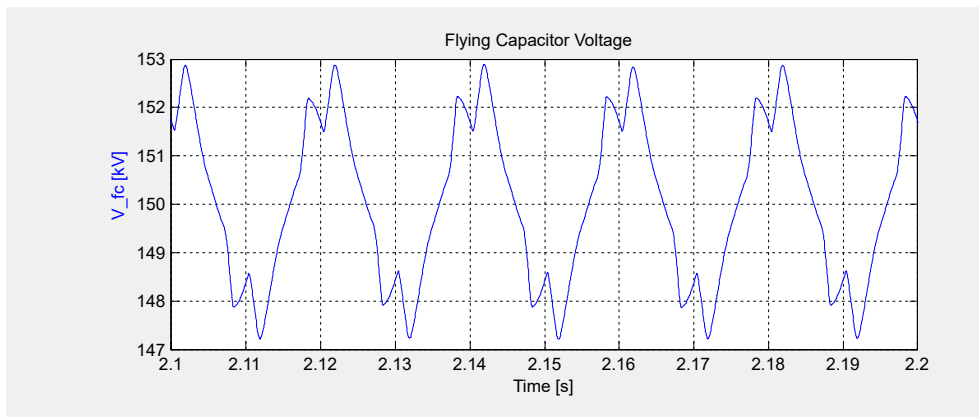


Figure 6.31: Waveform of flying capacitor voltage with thyristor in steady state [kV]

6.3.2 P=300 MW, Q=100 MVar

Another case, where the active power $P=300$ MW and the reactive power $Q=100$ MVar, is presented in Figures 6.32 and 6.33. From the figures, it can be observed that the converter operates at approximately $P=288$ MW and $Q=121$ MVar.

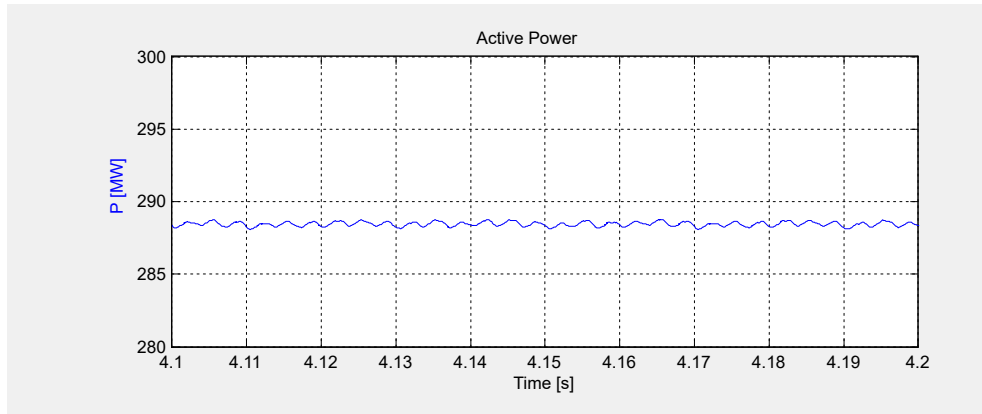


Figure 6.32: Waveform of active power with thyristor in steady state [kW]

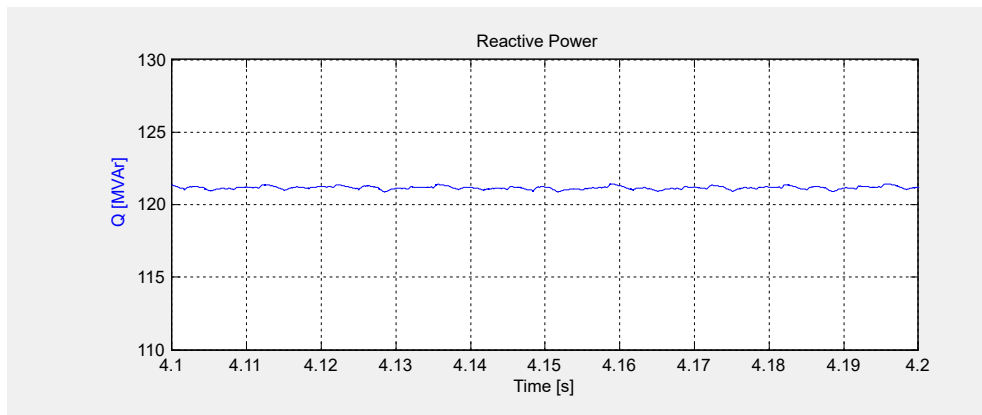


Figure 6.33: Waveform of reactive power with thyristor in steady state [kVAr]

The phase shift between the output voltage and current can be observed in Figure 6.34, where the current waveform lags behind the voltage waveform by roughly 19 degrees.

Similarly, the waveforms of the chain-link current and flying capacitor current change accordingly, while the current waveform of the switch maintains its original shape. The chain-link and flying capacitor currents are

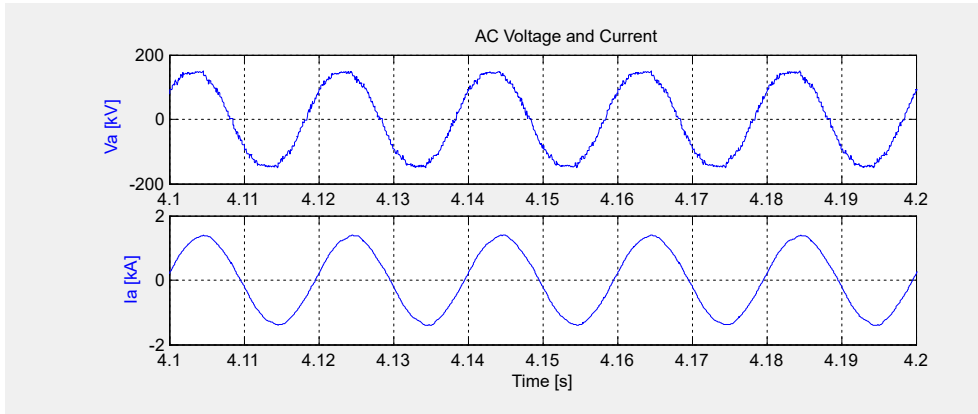


Figure 6.34: Waveform of AC voltage and current with thyristor in steady state [kV/kA]

illustrated in Figures 6.35 and 6.36, respectively. The flying capacitor voltage is shown in the Figure 6.37 to demonstrate the voltage ripple.

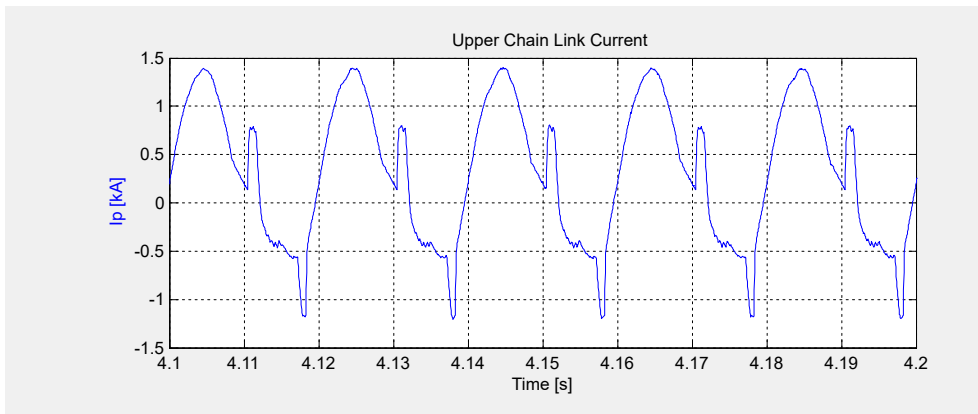


Figure 6.35: Waveform of upper chain link current with thyristor in steady state [kA]

The voltages of the upper submodules are also shown in Figure 6.38. From the figure, it can be observed that the submodule voltages are balanced as intended, but the voltage ripple is a little bit higher compared with the case when $Q=0$ MVar. The voltage ripple across the submodules ranges from 14.78 kV to 15.4 kV because of the reactive power increase, but this variation remains within the safe operating range of the submodules.

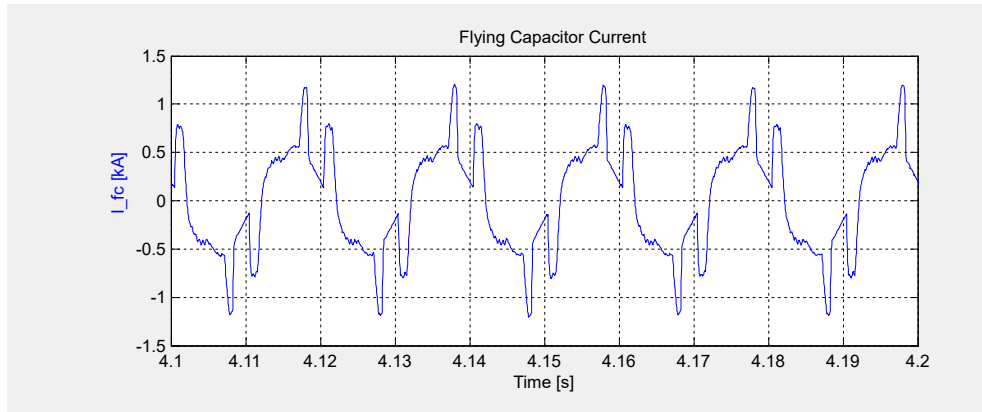


Figure 6.36: Waveform of flying capacitor current with thyristor in steady state [kA]

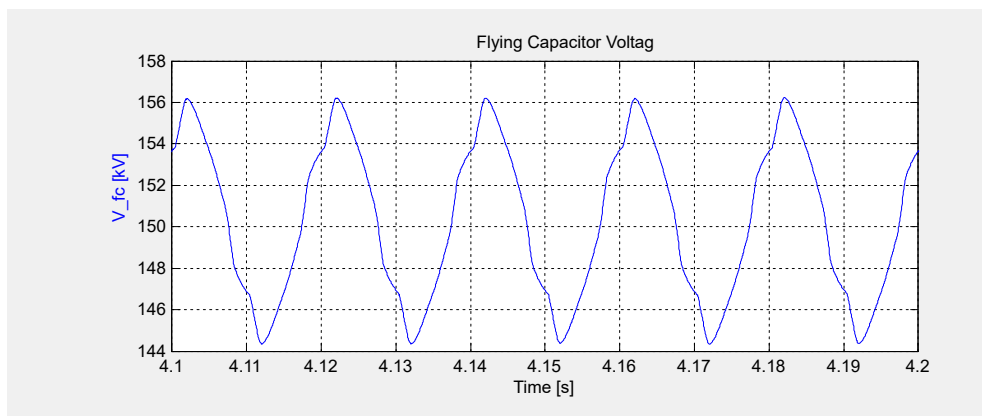


Figure 6.37: Waveform of flying capacitor voltage with thyristor in steady state [kV]

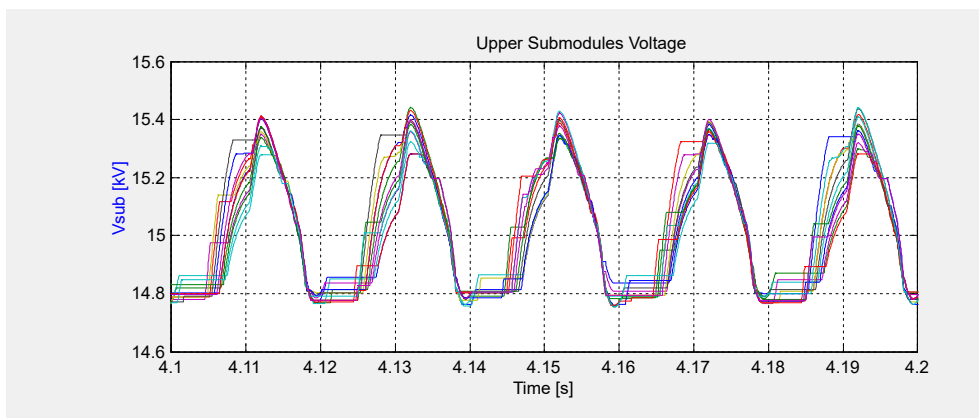


Figure 6.38: Waveform of one phase submodules voltage with thyristor in steady state [kV]

Chapter 7

Conclusions and Future Work

This chapter concludes the thesis. Section 7.1 presents the main findings and conclusions drawn from the research, while Section 7.2 outlines potential directions for future work based on the outcomes of this study.

7.1 Conclusions

This thesis presents a comprehensive study of a novel modular multilevel converter topology, the Flying Capacitor Hybrid Modular Multilevel Converter. Through detailed analysis of the circuit structure and control algorithms, an improved approach for replacing IGBT devices with thyristors is proposed and thoroughly examined. The proposed method is validated through simulation, confirming its effectiveness and feasibility. The main contributions of this work are summarized as follows:

- The working principle of the FC-HMMC is studied in detail in Chapter 2 by analyzing its six operating segments within one cycle. The equation between current and power is also examined, and the sizing of core components is determined using appropriate design formulas. Additionally, redundant operating states, including the blocked state, are identified and discussed to provide more aspects of the circuit.
- The implementation of closed-loop control for the FC-HMMC is thoroughly detailed in Chapter 3. This chapter presents the structure of the control blocks along with the corresponding waveform shapes. The algorithm for how the grid angle is used to determine the synthesis control is illustrated using both code and diagrams, providing a clear

view of its functionality. The relevant mathematical formulas are also included in the respective sections to support the control logic.

- The limitations of using IGBTs in the FC-HMMC topology are discussed in Chapter 4, where the concept of replacing IGBTs with thyristors is proposed and the problem of how to create reverse voltage is solved. A detailed analysis is provided to demonstrate why thyristors cannot be readily used in the original circuit configuration. To address this, an improved synthesized control strategy, where two segments are added to create the negative voltage and compensate for the current spike, is introduced and explained in detail. The implementation of this control method is supported by both theoretical analysis and simulation results. The corresponding code is included in Appendix B.
- The overall simulation setup and results are presentation in Chapters 5 and 6, respectively. The former chapter offers a detailed explanation of how the complex circuit and control blocks are constructed in the PSCAD simulation environment, along with the specification of all relevant parameters. The latter chapter presents simulation results for both IGBT-based and thyristor-based configurations, including a case study demonstrating the system's dynamic performance.

7.2 Future Work

This thesis presents the flying capacitor modular multilevel converter (FC-HMMC) topology and provides a comprehensive analysis of its operating principles. Additionally, it proposes a potential replacement of conventional switching devices with thyristors, along with a corresponding control algorithm. The feasibility of this approach is validated through simulation and analysis. There are several areas that can be explored as future work:

- The potential improvement to the control algorithm involves reducing the high degree of coupling currently present in the six operating segments. At present, the control strategy focuses on balancing the capacitor voltage by comparing it with a reference value, which results in interdependent control across all six segments. However, since each segment corresponds to a distinct equivalent circuit, the independent control strategies for each segment can be developed, thereby streamlining the overall control structure and enhancing performance.

- Further investigation into fault scenarios is a valuable direction. Since the FC-HMMC operates with independent control on each phase, analyzing fault conditions such as single-line-to-ground faults would be particularly interesting. This could lead to the development of fault ride-through strategies that allow the converter station to remain operational without tripping during such events.
- This thesis primarily focuses on using simulation software to analyze the behavior of the proposed topology. Further validation can be achieved by implementing the FC-HMMC using a real-time simulator to replicate the circuit in a laboratory environment. This setup allows for experimental verification of the circuit and waveform analysis using an oscilloscope.

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Appendix A

Matlab Script

A.1 Script for Single Phase Analysis

Listing A.1: Script for Single Phase Analysis

```

%% Clear workspace and command window
clear; clc; close all;

%% Parameters
% FC-MMC Parameters
N = 12;           % Number of SM
V_dc = 300*10^3; % [V]
% V_ac = 148*10^3; % [V]
C_SM = 5*10^-3; % [F]
V_SM = 12.5*10^3; % [V]
% f_s = 6*10^3; % [Hz]
% L_m = 3*10^-3; % [H]
V_FC = 150*10^3; % [V]
C_FC = 0.416*10^-3; % [F]
m = 0.9867;      % Modulation Index

% Grid Parameters (Resistive and Inductive)
% R = 68.5714;    % Resistance of grid load [R]
% L = 0.1;       % Inductance of grid load [H]
f = 50;         % Grid Frequency
omega = 2*pi*f; % Angular frequency
i_max = 60;     % Output current
phi = 0/360*2*pi; % Current angle - voltage angle (if >0
    ↪ I lag V, if <0 I lead V)

```

```

%% Specify Output Current and Voltage
syms t
V_max = m*V_dc/2; % Peak amplitude of phase
    ↪ voltage
v_a = V_max*sin(2*pi*f*t); % Phase A voltage
v_b = V_max*sin(2*pi*f*t-2*pi/3); % Phase B shifted by
    ↪ -120°
v_c = V_max*sin(2*pi*f*t-4*pi/3); % Phase C shifted by
    ↪ -240°

% Calculate currents
i_a = i_max*sin(2*pi*f*t-phi); % Phase A current
i_b = i_max*sin(2*pi*f*t-2*pi/3-phi); % Phase B current
i_c = i_max*sin(2*pi*f*t-4*pi/3-phi); % Phase C current

% Calculate DC current (Balanced Grid)
I_dc = 3/4*m*i_max/sqrt(2)*cos(phi);

%% Phase A Voltage and Current Analysis
% Current of Q1 Switch of phase A
i_dcqa = piecewise(...
    0 <= t < (pi/3)/(2*pi*f), I_dc*3/pi*(2*pi*f)*t, ...
    (pi/3)/(2*pi*f) <= t < (2*pi/3)/(2*pi*f), I_dc, ...
    (2*pi/3)/(2*pi*f) <= t < (pi)/(2*pi*f), -I_dc*3/pi
    ↪ *(2*pi*f)*t+3*I_dc, ...
    (pi)/(2*pi*f) <= t < 2*pi/(2*pi*f), 0);

% Current of flying capacitor of phase A
i_fcqa = piecewise(...
    0 <= t < pi/(2*pi*f), i_dcqa - i_a, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -subs(i_dcqa - i_a,
    ↪ t, t - pi/(2*pi*f)));

% Voltage of positive chain link
v_pa = piecewise(...
    0 <= t < pi/(2*pi*f), V_dc/2 - v_a, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), V_dc/2);

% Current of positive chain link
i_pa = piecewise(...
    0 <= t < pi/(2*pi*f), i_a, ...

```

```

    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -i_fca);

% Voltage of negative chain link
v_na = piecewise(...
    0 <= t < pi/(2*pi*f), V_dc/2, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), v_a + V_dc/2);

% Current of negative chain link
i_na = piecewise(...
    0 <= t < pi/(2*pi*f), i_fca, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -i_a);

%% Phase A Power and Energy Analysis
% Define the variables
time = linspace(0, 2*pi/(2*pi*f), 30);
delta_v_fca = zeros(size(time));
ripple_f_fca = zeros(size(time));
v_fca = zeros(size(time));
E_fca = zeros(size(time));

% Calculate the voltage ripple with the current
delta_v_fca(1) = double(int(i_fca, t, 0, time(2)))/C_FC;
for k = 2:length(time)
    t_start = time(k-1);
    t_end = time(k);
    delta_v_fca(k) = double(int(i_fca, t, t_start, t_end)
        ↪ )/C_FC;
end

delta_v_max = sum(delta_v_fca(delta_v_fca > 0));

% Calculate the energy of capacitor
E_fca = 1/2*C_FC*v_fca.*v_fca;

%% Plot the result
figure(1)

% Subplot for three-phase AC voltages
subplot(4,2,1);
fplot(v_a, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(v_b, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);

```

```

fplot(v_c, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('Voltage','FontSize',12);
title('Three-Phase AC Voltage Waveforms','FontSize',14);
legend({'v_a','v_b','v_c'}, 'Location','best');

% Subplot for three-phase AC currents
subplot(4,2,2);
fplot(i_a, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(i_b, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_c, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('Current','FontSize',12);
title('Three-Phase AC Current Waveforms','FontSize',14);
legend({'i_a','i_b','i_c'}, 'Location','best');

% Subplot for i_dcpa
subplot(4,2,3);
fplot(i_dcpa, [0, 2*pi], 'r', 'LineWidth', 2);
grid on;
ylabel('i_{dcpa}','FontSize',12);
title('Current of Q1 Switch of Phase A','FontSize',14);

% Subplot for i_fca
subplot(4,2,4);
fplot(i_fca, [0, 2*pi], 'b', 'LineWidth', 2);
grid on;
ylabel('i_{fca}','FontSize',12);
title('Current of Flying Capacitor of Phase A','FontSize'
    ↪ ,14);

% Subplot for v_pa
subplot(4,2,5);
fplot(v_pa, [0, 2*pi], 'g', 'LineWidth', 2);
grid on;
ylabel('v_{pa}','FontSize',12);
title('Voltage of Positive Chain Link','FontSize',14);

% Subplot for i_pa
subplot(4,2,6);
fplot(i_pa, [0, 2*pi], 'm', 'LineWidth', 2);

```

```

grid on;
ylabel('i_{pa}', 'FontSize', 12);
title('Current_of_Positive_Chain_Link', 'FontSize', 14);

% Subplot for v_na
subplot(4, 2, 7);
fplot(v_na, [0, 2*pi], 'c', 'LineWidth', 2);
grid on;
ylabel('v_{na}', 'FontSize', 12);
title('Voltage_of_Negative_Chain_Link', 'FontSize', 14);

% Subplot for i_na
subplot(4, 2, 8);
fplot(i_na, [0, 2*pi], 'k', 'LineWidth', 2);
grid on;
ylabel('i_{na}', 'FontSize', 12);
title('Current_of_Negative_Chain_Link', 'FontSize', 14);

% Add dashed vertical lines to all subplots
for i = 1:8
    subplot(4, 2, i);
    % xlabel('\omega t / \pi', 'FontSize', 12, 'Interpreter
    ↪ ', 'tex');
    xlim([0, 2*pi/(2*pi*f)]); % Show one full cycle
    xticks(0:pi/3/(2*pi*f):2*pi/(2*pi*f));
    xticklabels({'0', 'pi/3', '2pi/3', 'pi', '4pi/3', '5pi/3',
    ↪ '2pi'});
    xline(0, '--k', 'HandleVisibility', 'off');
    xline(pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off')
    ↪ ;
    xline(2*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off
    ↪ ');
    xline(pi/(2*pi*f), '--k', 'HandleVisibility', 'off');
    xline(4*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off
    ↪ ');
    xline(5*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off
    ↪ ');
    xline(2*pi/(2*pi*f), '--k', 'HandleVisibility', 'off')
    ↪ ;
end

```

A.2 Script for Three Phase Analysis

Listing A.2: Script for Three Phase Analysis

```

%% Clear workspace and command window
clear; clc; close all;

%% Parameters
% FC-MMC Parameters
N = 12;           % Number of SM
V_dc = 300*10^3; % [V]
% V_ac = 148*10^3; % [V]
C_SM = 5*10^-3; % [F]
V_SM = 12.5*10^3; % [V]
% f_s = 6*10^3; % [Hz]
% L_m = 3*10^-3; % [H]
V_FC = 150*10^3; % [V]
C_FC = 0.416*10^-3; % [F]
m = 0.9867;      % Modulation Index

% Grid Parameters (Resistive and Inductive)
% R = 68.5714;    % Resistance of grid load [R]
% L = 0.1;       % Inductance of grid load [H]
f = 50;         % Grid Frequency
omega = 2*pi*f; % Angular frequency
i_max = 60;     % Output current
phi = 0/360*2*pi; % Current angle - voltage angle (if >0
    ↪ I lag V, if <0 I lead V)

%% Specify Output Current and Voltage
syms t
V_max = m*V_dc/2; % Peak amplitude of phase
    ↪ voltage
v_a = V_max*sin(2*pi*f*t); % Phase A voltage
v_b = V_max*sin(2*pi*f*t-2*pi/3); % Phase B shifted by
    ↪ -120°
v_c = V_max*sin(2*pi*f*t-4*pi/3); % Phase C shifted by
    ↪ -240°

% Calculate currents
i_a = i_max*sin(2*pi*f*t-phi); % Phase A current

```

```

i_b = i_max*sin(2*pi*f*t-2*pi/3-phi); % Phase B current
i_c = i_max*sin(2*pi*f*t-4*pi/3-phi); % Phase C current

% Calculate DC current (Balanced Grid)
I_dc = 3/4*m*i_max/sqrt(2)*cos(phi);

%% Phase A Voltage and Current Analysis
% Current of Q1 Switch of phase A
phi = 0/360*2*pi; % Current angle - voltage angle (if >0
    ↪ I lag V, if <0 I lead V)
i_dcpa = piecewise(...
    0 <= t < (pi/3)/(2*pi*f), I_dc*3/pi*(2*pi*f)*t, ...
    (pi/3)/(2*pi*f) <= t < (2*pi/3)/(2*pi*f), I_dc, ...
    (2*pi/3)/(2*pi*f) <= t < (pi)/(2*pi*f), -I_dc*3/pi
    ↪ *(2*pi*f)*t+3*I_dc, ...
    (pi)/(2*pi*f) <= t < 2*pi/(2*pi*f), 0);

% Current of flying capacitor of phase A
i_fca = piecewise(...
    0 <= t < pi/(2*pi*f), i_dcpa - i_a, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -subs(i_dcpa - i_a,
    ↪ t, t - pi/(2*pi*f)));

% Voltage of positive chain link
v_pa = piecewise(...
    0 <= t < pi/(2*pi*f), V_dc/2 - v_a, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), V_dc/2);

% Current of positive chain link
i_pa = piecewise(...
    0 <= t < pi/(2*pi*f), i_a, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -i_fca);

% Voltage of negative chain link
v_na = piecewise(...
    0 <= t < pi/(2*pi*f), V_dc/2, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), v_a + V_dc/2);

% Current of negative chain link
i_na = piecewise(...
    0 <= t < pi/(2*pi*f), i_fca, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -i_a);

```

```

% Voltage of Q1 Switch of phase A
v_dcpa = piecewise(...
    0 <= t < pi/(2*pi*f), 0, ...
    pi/(2*pi*f) <= t < 2*pi/(2*pi*f), -v_a);

%% Phase B Voltage and Current Analysis
% Current of Q1 Switch of phase B
i_dcpb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(i_dcpa, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_dcpa
    ↪ , t, t - (2*pi/3)/(2*pi*f)));

% Current of flying capacitor of phase B
i_fcb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(i_fca, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_fca,
    ↪ t, t - (2*pi/3)/(2*pi*f)));

% Voltage of positive chain link
v_pb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(v_pa, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_pa,
    ↪ t, t - (2*pi/3)/(2*pi*f)));

% Current of positive chain link
i_pb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(i_pa, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_pa,
    ↪ t, t - (2*pi/3)/(2*pi*f)));

% Voltage of negative chain link
v_nb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(v_na, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_na,
    ↪ t, t - (2*pi/3)/(2*pi*f)));

```

```

% Current of negative chain link
i_nb = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(i_na, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_na,
    ↪ t, t - (2*pi/3)/(2*pi*f)));

% Voltage of Q1 Switch of phase B
v_dcpc = piecewise(...
    0 <= t < (2*pi/3)/(2*pi*f), subs(v_dcpc, t, t + (4*pi
    ↪ /3)/(2*pi*f)), ...
    (2*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_dcpc
    ↪ , t, t - (2*pi/3)/(2*pi*f)));

%% Phase C Voltage and Current Analysis
% Current of Q1 Switch of phase C
i_dcpc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(i_dcpc, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_dcpc
    ↪ , t, t - (4*pi/3)/(2*pi*f)));

% Current of flying capacitor of phase C
i_fcc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(i_fcc, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_fcc,
    ↪ t, t - (4*pi/3)/(2*pi*f)));

% Voltage of positive chain link
v_pc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(v_pa, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_pa,
    ↪ t, t - (4*pi/3)/(2*pi*f)));

% Current of positive chain link
i_pc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(i_pa, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_pa,
    ↪ t, t - (4*pi/3)/(2*pi*f)));

```

```

% Voltage of negative chain link
v_nc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(v_na, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_na,
    ↪ t, t - (4*pi/3)/(2*pi*f)));

% Current of negative chain link
i_nc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(i_na, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(i_na,
    ↪ t, t - (4*pi/3)/(2*pi*f)));

% Voltage of Q1 Switch of phase B
v_dcpc = piecewise(...
    0 <= t < (4*pi/3)/(2*pi*f), subs(v_dcpc, t, t + (2*pi
    ↪ /3)/(2*pi*f)), ...
    (4*pi/3)/(2*pi*f) <= t < (2*pi)/(2*pi*f), subs(v_dcpc
    ↪ , t, t - (4*pi/3)/(2*pi*f)));

%% Plot the result
figure(1)

% Subplot for three-phase AC voltages
subplot(4,2,1);
fplot(v_a, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(v_b, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(v_c, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('Voltage', 'FontSize', 12);
title('Three-Phase AC Voltage Waveforms', 'FontSize', 14);
% legend({'v_a', 'v_b', 'v_c'}, 'Location', 'best');

% Subplot for three-phase AC currents
subplot(4,2,2);
fplot(i_a, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(i_b, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_c, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);

```

```

grid on;
ylabel('Current','FontSize',12);
title('Three-PhaseACCurrentWaveforms','FontSize',14);
% legend({'i_a','i_b','i_c'}, 'Location','best');

% Subplot for i_dcpa
subplot(4,2,3);
fplot(i_dcpa, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(i_dcpb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_dcpc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('i_{dcp}','FontSize',12);
title('CurrentofQ1SwitchofPhaseA/B/C','FontSize'
    ↪ ,14);

% Subplot for i_fca
subplot(4,2,4);
fplot(i_fca, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(i_fcb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_fcc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('i_{fca}','FontSize',12);
title('CurrentofFlyingCapacitorofPhaseA/B/C','
    ↪ FontSize',14);

% Subplot for v_pa
subplot(4,2,5);
fplot(v_pa, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(v_pb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(v_pc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('v_{pa}','FontSize',12);
title('VoltageofPositiveChainLinkofPhaseA/B/C','
    ↪ FontSize',14);

% Subplot for i_pa
subplot(4,2,6);
fplot(i_pa, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;

```

```

fplot(i_pb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_pc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('i_{pa}', 'FontSize', 12);
title('Current_of_Positive_Chain_Link_of_Phase_A/B/C', '
    ↪ FontSize', 14);

% Subplot for v_na
subplot(4, 2, 7);
fplot(v_na, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(v_nb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(v_nc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('v_{na}', 'FontSize', 12);
title('Voltage_of_Negative_Chain_Link_of_Phase_A/B/C', '
    ↪ FontSize', 14);

% Subplot for i_na
subplot(4, 2, 8);
fplot(i_na, [0, 2*pi/(2*pi*f)], 'r', 'LineWidth', 2);
    ↪ hold on;
fplot(i_nb, [0, 2*pi/(2*pi*f)], 'b', 'LineWidth', 2);
fplot(i_nc, [0, 2*pi/(2*pi*f)], 'g', 'LineWidth', 2);
grid on;
ylabel('i_{na}', 'FontSize', 12);
title('Current_of_Negative_Chain_Link_of_Phase_A/B/C', '
    ↪ FontSize', 14);

% Add dashed vertical lines to all subplots
for i = 1:8
    subplot(4, 2, i);
    % xlabel('\omega t / \pi', 'FontSize', 12, 'Interpreter
        ↪ ', 'tex');
    xlim([0, 2*pi/(2*pi*f)]); % Show one full cycle
    xticks(0:pi/3/(2*pi*f):2*pi/(2*pi*f));
    xticklabels({'0', 'pi/3', '2pi/3', 'pi', '4pi/3', '5pi/3',
        ↪ '2pi'});
    xline(0, '--k', 'HandleVisibility', 'off');
    xline(pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off')
        ↪ ;
    xline(2*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off

```

```

        ↪ ');
xline(pi/(2*pi*f), '--k', 'HandleVisibility', 'off');
xline(4*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off
        ↪ ');
xline(5*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off
        ↪ ');
xline(2*pi/(2*pi*f), '--k', 'HandleVisibility', 'off')
        ↪ ;
end

%% Plot for E_fca
figure(2)

% Subplot for E_fca
subplot(2,1,1);
plot(time, E_fca, 'r', 'LineWidth', 2)
grid on
xlabel('\omega_{t}/\pi', 'FontSize', 12, 'Interpreter', 'tex
        ↪ ')
ylabel('E_{fca}', 'FontSize', 12);
title('Energy of Flying Capacitor', 'FontSize', 14);

% Subplot for v_fca
subplot(2,1,2);
plot(time, v_fca, 'b', 'LineWidth', 2)
grid on
xlabel('\omega_{t}/\pi', 'FontSize', 12, 'Interpreter', 'tex
        ↪ ')
ylabel('v_{fca}', 'FontSize', 12);
title('Voltage of Flying Capacitor', 'FontSize', 14);

% Add dashed vertical lines to all subplots
for i = 1:2
    subplot(2,1,i);
    xlim([0, 2*pi/(2*pi*f)]); % Show one full cycle
    xticks(0:pi/3/(2*pi*f):2*pi/(2*pi*f));
    xticklabels({'0', 'T/6', 'T/3', 'T/2', '2T/3', '5T/6', 'T'
        ↪ });
    xline(0, '--k', 'HandleVisibility', 'off');
    xline(pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off')
        ↪ ;
    xline(2*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off

```

```
    ↪ ');  
xline(pi/(2*pi*f), '--k', 'HandleVisibility', 'off');  
xline(4*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off'  
    ↪ ');  
xline(5*pi/3/(2*pi*f), '--k', 'HandleVisibility', 'off'  
    ↪ ');  
xline(2*pi/(2*pi*f), '--k', 'HandleVisibility', 'off')  
    ↪ ;  
end
```

Appendix B

Fortran Script

B.1 Script for Synthesize Control

Listing B.1: Script for Synthesize Control

```
!  
    SUBROUTINE M2CTRAPEZOID (GA, IDCP, IDCN, IR, PHASE, ITR,  
        ↪ IFC)  
!  
! Generate trapezoidal current reference  
!  
!  
! 2025-04-14 Tingzhen Ye  
!  
! Inputs:  
!   GA: Grid angle to sync with  
!   IDCP: IDCP current reference value  
!   IDCN: IDCN current reference value  
!   IR: Reference output current  
!   PHASE: Select which phase(1:a, 2:b, 3:c)  
!  
! Outputs:  
!   ITR: Trapezoidal current  
!   IFC: Reference current for flying capacitor  
!  
! includes  
    INCLUDE "nd.h"  
    INCLUDE "emtstor.h"  
    INCLUDE "s1.h"
```

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```
      INCLUDE "emtconst.h"
!
! variables
      IMPLICIT NONE
      REAL GA, IDCP, IDCN, IR, ITR, IFC, PHASE
!
! Initialization
      ITR = 0
      IFC = 0
!
! Generate the Current Reference
      IF ( PHASE == 1 ) THEN
          IF ( GA .LE. 60 ) THEN
              ITR = IDCP*GA/60
          ELSEIF ( GA .LE. 120 ) THEN
              ITR = IDCP
          ELSEIF ( GA .LE. 180 ) THEN
              ITR = -IDCP*(GA/60)+3*IDCP
          ELSEIF ( GA .LE. 240 ) THEN
              ITR = -IDCN*(GA/60)+3*IDCN
          ELSEIF ( GA .LE. 300 ) THEN
              ITR = -IDCN
          ELSE
              ITR = IDCN*GA/60-6*IDCN
          ENDIF
          IFC = ITR - IR
      ELSEIF ( PHASE == 2 ) THEN
          IF ( GA .LE. -60 ) THEN
              ITR = -IDCN
          ELSEIF ( GA .LE. 0 ) THEN
              ITR = IDCN*GA/60
          ELSEIF ( GA .LE. 60 ) THEN
              ITR = IDCP*GA/60
          ELSEIF ( GA .LE. 120 ) THEN
              ITR = IDCP
          ELSEIF ( GA .LE. 180 ) THEN
              ITR = -IDCP*(GA/60)+3*IDCP
          ELSE
              ITR = -IDCN*(GA/60)+3*IDCN
          ENDIF
          IFC = ITR - IR
      ELSEIF ( PHASE == 3 ) THEN
```

```

IF ( GA .LE. 180 ) THEN
    ITR = -IDCP*GA/60+3*IDCP
ELSEIF ( GA .LE. 240 ) THEN
    ITR = -IDCN*GA/60+3*IDCN
ELSEIF ( GA .LE. 300 ) THEN
    ITR = -IDCN
ELSEIF ( GA .LE. 360 ) THEN
    ITR = IDCN*GA/60-6*IDCN
ELSEIF ( GA .LE. 420 ) THEN
    ITR = IDCP*GA/60-6*IDCP
ELSE
    ITR = IDCP
ENDIF
IFC = ITR - IR
ENDIF
RETURN
END

```

B.2 Script for Modified Synthesize Control

Listing B.2: Script for Modified Synthesize Control

```

!
  SUBROUTINE M2CTRAPEZOID (GA, IDCP, IDCN, IR, PHASE, ITR,
    ↪ IFC)
!
! Generate trapezoidal current reference
!
!
! 2025-04-14 Tingzhen Ye
!
! Inputs:
!   GA: Grid angle to sync with
!   IDCP: IDCP current reference value
!   IDCN: IDCN current reference value
!   IR: Reference output current
!   PHASE: Select which phase(1:a, 2:b, 3:c)
!
! Outputs:
!   ITR: Trapezoidal current

```

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```

!   IFC: Reference current for flying capacitor
!
! includes
    INCLUDE "nd.h"
    INCLUDE "emtstor.h"
    INCLUDE "sl.h"
    INCLUDE "emtconst.h"
!
! variables
    IMPLICIT NONE
    REAL GA, IDCP, IDCN, IR, ITR, IFC, PHASE
!
! Initialization
    ITR = 0
    IFC = 0
!
! Generate the Current Reference
    IF ( PHASE == 1 ) THEN
        IF ( GA .LE. 40 ) THEN
            ITR = IDCP*GA/60
        ELSEIF ( GA .LE. 60 ) THEN
            ITR = IDCP*GA/60+0.6
        ELSEIF ( GA .LE. 120 ) THEN
            ITR = IDCP
        ELSEIF ( GA .LE. 160 ) THEN
            ITR = -IDCP*GA/60+3*IDCP
        ELSEIF ( GA .LE. 180 ) THEN
            ITR = -IDCP*GA/60+3*IDCP-0.6
        ELSEIF ( GA .LE. 220 ) THEN
            ITR = -IDCN*GA/60+3*IDCN
        ELSEIF ( GA .LE. 240 ) THEN
            ITR = -IDCN*GA/60+3*IDCN-0.6
        ELSEIF ( GA .LE. 300 ) THEN
            ITR = -IDCN
        ELSEIF ( GA .LE. 340 ) THEN
            ITR = IDCN*GA/60-6*IDCN
        ELSE
            ITR = IDCN*GA/60-6*IDCN+0.6
        ENDIF
        IFC = ITR - IR
    ELSEIF ( PHASE == 2 ) THEN
        IF ( GA .LE. -60 ) THEN

```

```

      ITR = -IDCN
ELSEIF ( GA .LE. -20 ) THEN
      ITR = IDCN*GA/60
ELSEIF ( GA .LE. 0 ) THEN
      ITR = IDCN*GA/60+0.6
ELSEIF ( GA .LE. 40 ) THEN
      ITR = IDCP*GA/60
ELSEIF ( GA .LE. 60 ) THEN
      ITR = IDCP*GA/60+0.6
ELSEIF ( GA .LE. 120 ) THEN
      ITR = IDCP
ELSEIF ( GA .LE. 160 ) THEN
      ITR = -IDCP*GA/60+3*IDCP
ELSEIF ( GA .LE. 180 ) THEN
      ITR = -IDCP*GA/60+3*IDCP-0.6
ELSEIF ( GA .LE. 220 ) THEN
      ITR = -IDCN*GA/60+3*IDCN
ELSE
      ITR = -IDCN*GA/60+3*IDCN-0.6
ENDIF
      IFC = ITR - IR
ELSEIF ( PHASE == 3 ) THEN
      if ( GA .LE. 160 ) THEN
      ITR = -IDCP*GA/60+3*IDCP
ELSEIF ( GA .LE. 180 ) THEN
      ITR = -IDCP*GA/60+3*IDCP-0.6
ELSEIF ( GA .LE. 220 ) THEN
      ITR = -IDCN*GA/60+3*IDCN
ELSEIF ( GA .LE. 240 ) THEN
      ITR = -IDCN*GA/60+3*IDCN-0.6
ELSEIF ( GA .LE. 300 ) THEN
      ITR = -IDCN
ELSEIF ( GA .LE. 340 ) THEN
      ITR = IDCN*GA/60-6*IDCN
ELSEIF ( GA .LE. 360 ) THEN
      ITR = IDCN*GA/60-6*IDCN+0.6
ELSEIF ( GA .LE. 400 ) THEN
      ITR = IDCP*GA/60-6*IDCP
ELSEIF ( GA .LE. 420 ) THEN
      ITR = IDCP*GA/60-6*IDCP+0.6
ELSE
      ITR = IDCP

```

```
      ENDIF  
      IFC = ITR - IR  
ENDIF  
RETURN  
END
```


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