http://www.diva-portal.org

Postprint

This is the accepted version of a paper published in *IEEE Electron Device Letters*. This paper has been peer-reviewed but does not include the final publisher proof-corrections or journal pagination.

Citation for the original published paper (version of record):

Li, Y., Bleiker, S J., Worsey, E., Kumar Kulsreshath, M., Tang, Q. et al. (2026)
A CMOS-Compatible Heterogeneous 3-D Integration Platform for Silicon Nanoelectromechanical Switches
IEEE Electron Device Letters, 47(3): 598-601
https://doi.org/10.1109/led.2026.3655495

Access to the published version may require subscription.

N.B. When citing this work, cite the original published paper.

Permanent link to this version:
http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-382522

A CMOS-compatible heterogeneous 3-D integration platform for silicon nanoelectromechanical switches

Yingying Li, Simon J. Bleiker, Elliott Worsey, Mukesh Kumar Kulsreshath, Qi Tang, Christian Reich, Stefan Ernst, Shyamprasad N. Raja, August Djuphammar, Kristinn B. Gylfason, *Member, IEEE*, Dinesh Pamunuwa, *Senior Member, IEEE*, Frank Niklaus, *Senior Member, IEEE*

***Abstract*—Nanoelectromechanical (NEM) switches have near vertical turn-off transient, zero off-state leakage, and non-volatile behavior, ideal qualities for low power computing and memory applications. To realize this potential, large-scale integration of NEM switches is required. Here we introduce a three-dimensional (3-D) heterogeneous integration platform that leverages a standard silicon-on-insulator (SOI) CMOS foundry process, combined with post-processing of the foundry wafers to integrate silicon NEM switches. Within this platform, we seamlessly integrated both volatile 3-terminal (3-T) and non-volatile 7-terminal (7-T) NEM switches. We demonstrate successful electrical programming and reprogramming of both switch types, validating the platform's functionality and its potential for constructing densely integrated NEM switch-based logic circuits and non-volatile memories.**

***Index Terms*—Nanoelectromechanical switch, NEM computing, NEM memory, heterogeneous 3-D integration.**

I. Introduction

NANOELECTROMECHANICAL (NEM) switches offer unique benefits, including a nearly vertical switching slope and zero off-state leakage [1], [2], making them highly energy-efficient alternatives to CMOS circuits in specific applications like edge computing [3]–[5]. The use of NEM switches has been explored in CMOS power gating [6], [7], field programmable gate arrays (FPGAs) [5], [8], [9], energy efficient look-up tables (LUTs) [10]–[12], and memory devices [13]–[15], all benefiting from reduced static power dissipation. However, challenges in scaling NEM-switch circuits for manufacturing in standard CMOS foundries and implementing dense interconnects in practical systems have limited their industrial adoption [3], [16], [17]. Prior research has explored utilizing the 3-D metal interconnect layers, such as aluminum [3] and copper [14], [15], [18]–[20] in the CMOS back-end-of-line (BEOL) as both the structural material and the routing paths for NEM switches. A detailed comparison of integrated NEM switches can be found in our recent work [21]. However, this approach faces reliability issues due to material fatigue, curling of metallic structures, residual stress gradients, and thermal budget constraints [22]. Furthermore, the switch designs are often restricted to straight cantilevers, as more functionally geometries, like curved structures, are difficult to achieve within BEOL constraints. By contrast, mono-crystalline silicon (Si) NEM switches offer improved long-term stability due to the superior material quality of Si [23]–[25], and greater design flexibility via in-plane lithographic patterning [26]. Currently however, most Si NEM switches are fabricated on SOI substrates without multi-layer interconnects, restricting routing to one single layer (e.g. Si device layer) and impeding the realization of complex logic circuits [17], [23]. We recently reported monolithic integration of Si NEM switches and BEOL interconnects in an SOI foundry process [17], [21]. However, this approach has severe limitations in the achievable NEM switch integration density and routing flexibility, as switches cannot be vertically stacked with interconnects. 3-D integration, with enhanced routing densities through vertical stacking of the interconnect layers and the NEM switches, holds great potential for implementing large-scale Si NEM circuits [5], but has yet to be realized. Here, we introduce a 3-D heterogeneous integration approach that leverages an existing SOI CMOS foundry process (illustrated in Fig.1a). With this approach, we demonstrate integrated 3-terminal (3-T) and 7-terminal (7-T) NEM switches with volatile and non-volatile functionilities. This architecture enables vertical stacking of Si NEM switches above BEOL interconnects, enhancing routing density and device count, thereby opening new avenues for constructing high-density NEM logic circuits and non-volatile memories.

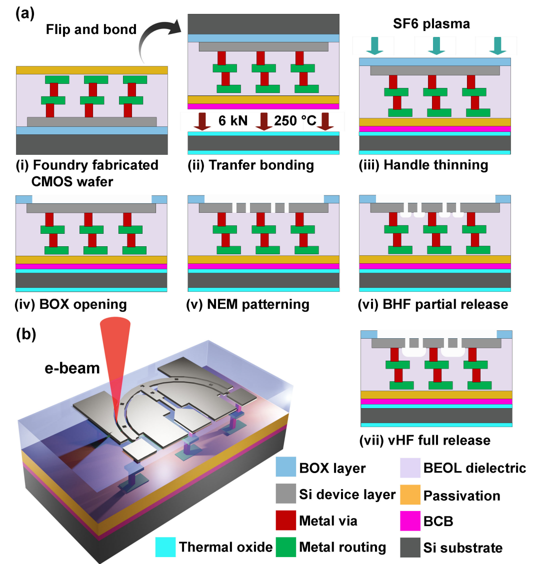

Fig. 1. (a) Cross-sectional schematic of the 3-D heterogeneous integration approach. (b) 3-D schematic of an integrated 7-T NEM switch after e-beam patterning.

This research was supported in part by EU H2020 under grant No. 871740 ZeroAMP, and in part by the i-EDGE project funded by the European Union (grant No. 101092018), the Swiss State Secretariat for Education, Research and Innovation (SERI) and UK Research and Innovation (UKRI) under the UK government's Horizon Europe funding guarantee (grant No. 10061130 and 10063023).

Manuscript received April 19, 2021; revised August 16, 2021.

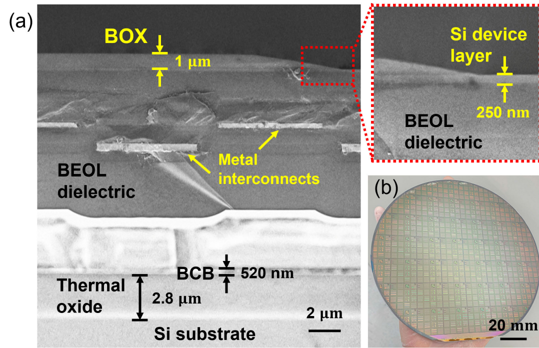

Fig. 2. (a) Cross-sectional SEM image of a bonded and thinned wafer, showing the oxidized Si substrate at the bottom, and the transferred layers from SOI CMOS foundry wafer with metal interconnects on the top. The inset highlights the Si device layer of the SOI CMOS substrate. (b) Image of a 150 mm diameter wafer with the transferred layers, before dicing and NEM switch patterning.

II. 3-D Heterogeneous Integration Approach

To validate the proposed 3-D heterogeneous integration platform for implementing integrated NEM switches, we used 150 mm foundry wafers from a mature SOI CMOS technology node (XI10, XFAB, Germany), featuring a standard 3-level BEOL interconnect stack (Fig.1a(i)). The wafer comprises, from bottom to top: a Si handle layer of the SOI wafer, a 1 μm-thick buried oxide (BOX), a 250 nm-thick monocrystalline Si device layer (the layer which typically hosts the CMOS transistors), the BEOL metallization, a PECVD SiO_2 dielectric stack serving as the sacrificial layer for the release etch, and a SiO_2 passivation layer. The CMOS foundry wafer was bonded with its top surface against an pre-oxidized Si substrate (double-side polished, DSP) using low-temperature adhesive wafer bonding (Fig.1a(ii)). This bonding method, chosen for its simplicity and insensitivity to defects, interface contaminants and particles at the bond interface [27]–[29], uses a 520 nm-thick Benzocyclobutene (BCB) polymer layer that was spin-coated on the foundry wafer as intermediate adhesive layer. The BCB was soft-baked at 100 °C for 2 min to remove volatile components, then pre-cured at 160 °C for 3 min (Fig. 1a(i)), while the target substrate was pre-baked at 100 °C for 2 min. The wafers were then aligned and bonded in vacuum using a CB8 wafer bonder (SussMicroTec, DE). In this process, a bond force of 6 kN was applied to the wafer stack as the bond chuck temperature was ramped up to 250 °C over 30 min, held for 1 h, and then cooled to room temperature over 30 min, thereby fully curing the BCB adhesive. Post-bonding, the Si handle layer was etched away by reactive ion etching (RIE) using SF_6 plasma (Fig.1a(iii)). The oxidized Si target wafer (2.8 μm-thick thermal SiO_2) protected the bonded structure during etching, while the BOX layer acts as an effective RIE etch stop to preserve the device layer. Following handle layer removal, we used mask-less laser lithography (MLA 150, Heidelberg Instruments GmbH, DE) to define the areas where the BOX layer would be opened. A subsequent buffered HF (BHF) etch removed BOX in exposed areas, granting access to the underlying Si device layer (Fig.1a(iv)).

To visualize the transferred layer stack after wafer bonding, handle layer thinning and the BOX opening step, we cleaved a substrate sample and imaged the wafer cross-section using scanning electron microscopy (SEM) (Fig.2a), showing the layer stack, including the oxidized Si substrate, the BCB layer, the metal interconnects embedded within the dielectric layers, the Si device layer, and the BOX layer, arranged from bottom to top. A full 150 mm diameter wafer with the transferred layers, following the steps shown in Fig.1a(iv), is depicted in Fig.2b. For ease of process development, the 150 mm wafer was diced into 2 cm × 2 cm chips, which were used for subsequent fabrication steps. After dicing, we patterned the NEM switches in the Si device layer using electron beam lithography (EBL, Raith Voyager system, Raith GmbH, DE) with a positive-tone resist (AR-P 6200.09, Allresist GmbH, DE), followed by an RIE process to define the NEM switch structures in the Si device layer (Fig.1a(v) and Fig.1b). The structures were then released in a two-step etching process (Fig.1a(vi) and (vii)). First, a 2 min BHF wet etch partially removed the sacrificial SiO_2 layer. This was followed by a time-controlled vapor-phase hydrofluoric (vHF) etch using an Orbis Alpha system (MEMSSTAR, UK) carried out at 18 Torr for 2 min, to fully suspend the movable beams. Typically, vHF etching is preferred to avoid stiction during NEM release [30], [31]. However, vHF is highly sensitive to the quality and density of the SiO_2 layers involved. Low-density or doped SiO_2, commonly used in BEOL dielectrics, can exhibit surface roughness, porosity, and pinholes after vHF etching (see Fig.3c). In contrast, BHF wet etching does not cause the same damage but increases the risk of stiction. Our combined BHF-vHF release process mitigates both issues, enabling stiction-free release while minimizing vHF-induced damage to the SiO_2 layers.

Using this process, we fabricated 3-T and 7-T NEM switches (see Fig.3a and Fig.3b, imaged after Si etching). The designs are based on our previous works [5], [17], [26], which have been further miniaturized and adapted to the foundry substrate used in this study. Detailed switch dimensions are provided in Table I. Both 3-T and 7-T designs were configured such that their suspended parts are released at a 400 nm undercut in the underlying SiO_2. Optical inspection following the final release step confirmed an undercut of approximately 800 nm, which was uniform across the entire chip, with no observable bending or stiction issues. Fig.3d reveals the underlying metal interconnect lines and the anchor vias connecting the metal lines to the switch terminals.

III. Design and Characterization of the Integrated NEM Switches

To demonstrate the NEM switch integrity and functionality, we electrically characterized the fabricated switches after suspension. The volatile 3-T NEM switch features a drain (D0), a gate (G0), and a movable beam attached to the source (S0) (Fig.3a); the non-volatile 7-T NEM switch features two drains (D1 and D2), two combined gate terminals (G1 and G2), and a bistable circular beam attached to the source (S) (Fig.3b). The switch terminals are electrically connected to probe pads through the BEOL metallization routing layers of the SOI CMOS process. We performed the electrical measurements by

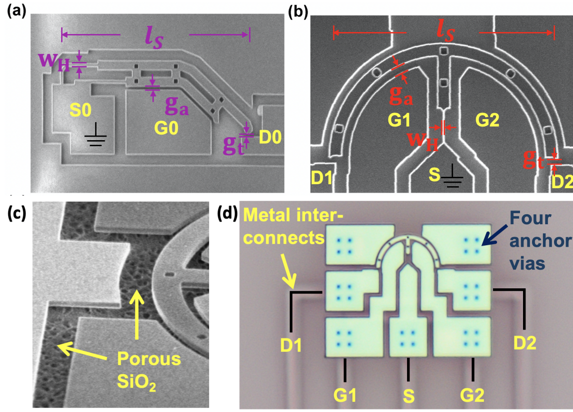

Fig. 3. SEM image of (a) the 3-T NEM switch and; (b) the 7-T NEM switch before release etch (Fig.1a(v)). (c) SEM image of the porous SiO_2 surface due to vHF etch damage. (d) Microscope image of a 7-T NEM switch with visible metal interconnect lines.

TABLE I
DIMENSIONS OF THE 3-T AND 7-T NEM SWITCHES

Parameters	Symbol	3-T	7-T
Hinge width (nm)	w_H	250	170
Tip gap (nm)	g_t	170	170
Gate gap (nm)	g_a	260	270
Switch length (µm)	l_s	17	11.5

directly probing the pads in an Argon environment under hot-switching conditions.

A. Volatile 3-T NEM Switch

To actuate the 3-T NEM switch, we applied a constant voltage (V_D = 5 V) to D0 while grounding S0 (Fig.3a). The gate voltage (V_G) was then ramped from 0 V to 20 V. The switch tip contacted D0 at the pull-in voltage (V_{pi}), resulting in a current flow (I_{ds}) through the drain and source, limited to 1 nA. As the voltage ramped back down, the beam disconnected from the drain at the pull-out voltage (V_{po}). Fig.4a shows experimental results for an integrated 3-T NEM switch. The device exhibited volatile switching for two cycles before stiction occurred. In the 1st cycle, the measured V_{pi} and V_{po} were 18.3 V and 12.8 V, respectively. In the 2nd cycle, V_{pi} increased to 23.9 V and V_{po} decreased to 5 V. This change indicated rapid deterioration of the Si-Si contact interface, leading to the contact resistance increasing and poor endurance. Introducing a dedicated contact coating is a potential approach to mitigate these issues [32].

B. Non-volatile 7-T NEM Switch

For the 7-T NEM switch, the bistable beam can be actuated in two directions: counterclockwise towards D1 (state “0”) by applying a voltage on G1 (V_{G1}), or clockwise towards D2 (state “1”) by applying (V_{G2}). A constant voltage of V_{d1} = V_{d2} = 5 V is applied to D1 and D2, while grounding S. From the neutral position, we first programmed state “0” by ramping V_{G1} from 0 V to 17 V. The source contacted D1 at the 1st programming cycle when V_{pr} = 10.4 V (Fig. 4b). After removing the gate voltage, the source remained in contact with D1, demonstrating non-volatile behavior. Next,

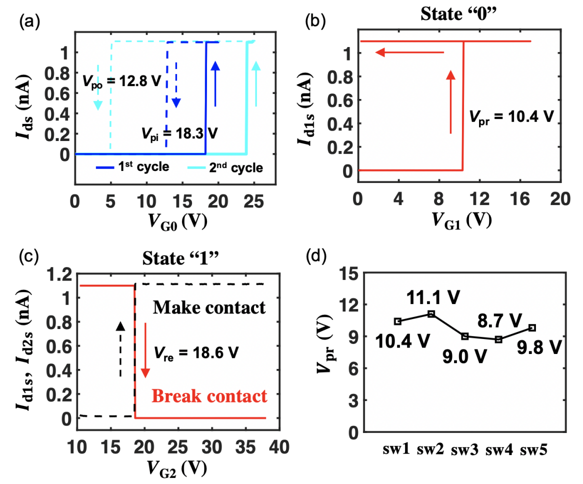

Fig. 4. Experimental results showing: (a) Pull-in and pull-out characterization of a volatile 3-T NEM switch, showing two consecutive cycles; in the 1st cycle, pull-in occurs at 18.3 V and pull-out at 12.8 V. (b) The first programming cycle and (c) the second reprogramming cycle of a 7-T NEM switch. (d) First-cycle pull-in voltage of five 7-T NEM switches.

we maintained the same settings on the drain and source terminals and ramped V_{G2} from 10 V to 38 V. Fig. 4c shows the transition from state “0” to state “1” at the reprogramming voltage V_{re} = 18.6 V, where the source disconnected from D1 and immediately connected with D2. Out of the five 7-T NEM switches that we measured, three were successfully programmed and sub-sequently reprogrammed for one cycle before permanent stiction occurred. The remaining two 7-T devices experienced stiction failures after the 1st actuation cycle, due to degradation of the Si-Si contact. The first-cycle programming voltages of all measured 7-T NEM switches was relatively stable, within a range of 9.9 ± 1.2 V (Fig. 4d).

IV. DISCUSSION AND CONCLUSION

Here we reported a 3-D heterogeneous integration approach using SOI CMOS foundry wafers to address critical scalability and routing challenges for NEM switches. With this approach, we demonstrate vertical stacking of both volatile and non-volatile NEM switches on top of a multi-layer metal interconnect stack, enabling large-scale integration with high routing density between the NEM switches. The NEM switch output nodes and actuation terminals are routed through standard metal interconnect layers, thereby enabling future integration of NEM switches with CMOS logic using the same interconnect stack. It should be noted that, in the present implementation, the Si-Si contact results in high on-resistance and limited cycling reliability. The on-state resistance of the switch is estimated to be on the order of $100\,\mathrm{k\Omega}$ to $1\,\mathrm{M\Omega}$ and a contact coating is important both to reduce it and mitigate stiction-induced failure [21]. Contact reliability is a known challenge in NEM switches and promising contact materials for use with our heterogeneous 3-D integration platform include ruthenium (Ru) [32] and carbon-based contacts such as nanocrystalline graphite (NCG) [23]. For example, Ru contacts can be added using a lift-off process [32] to the BEOL switch fabrication in our heterogeneous 3-D integration method to improve NEM switch reliability and performance.

References

[1] W. W. Jang, J. O. Lee, J.-B. Yoon, M.-S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park, and W.-S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," *Appl. Phys. Lett.*, vol. 92, no. 10, p. 103110, 2008, doi: 10.1063/1.2892659.

[2] R. H. Dennard, J. Cai, and A. Kumar, "A perspective on today's scaling challenges and possible future," in *Microelectronics: Devices, Circuits and Systems*, 1st ed., pp. 3–18, 2018, doi: 10.1016/B978-0-12-812311-9.00001-3.

[3] T.-S. Kim, Y.-B. Lee, S.-H. Kim, S.-Y. Lee, S.-J. Lee, and J.-B. Yoon, "Monolithically 3-D integrated nanoelectromechanical (NEM) configuration memory for CMOS-NEM hybrid demultiplexer," *IEEE Electron Device Lett.*, vol. 44, no. 12, pp. 2055–2058, Dec. 2023, doi: 10.1109/LED.2023.3322399.

[4] Q. Tang, E. Worsey, M. K. Kulsreshath, Y. Fan, Y. Li, S. Bleiker, "Energy consumption in micro- and nanoelectromechanical relays," *IEEE Trans. Electron Devices*, vol. 72, no. 4, pp. 1969–1976, Apr. 2025, doi: 10.1109/TED.2025.3537945.

[5] T. Qin, S. J. Bleiker, S. Rana, F. Niklaus, and D. Pamunuwa, "Performance analysis of nanoelectromechanical relay-based field-programmable gate arrays," *IEEE Access*, vol. 6, pp. 15997–16009, 2018, doi: 10.1109/ACCESS.2018.2816781.

[6] M. B. Henry and L. Nazhandali, "NEMS-based functional unit powergating: Design, analysis, and optimization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 2, pp. 290–302, 2013, doi: 10.1109/TCSI.2012.2215785.

[7] S. Saha, U. S. Kumar, M. S. Baghini, M. Goel, and V. R. Rao, "A nanoelectromechanical switch-based power gating for effective standby power reduction in FinFET technologies," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 681–684, 2017, doi: 10.1109/LED.2017.2686649.

[8] Y. J. Kim and W. Y. Choi, "Nonvolatile nanoelectromechanical memory switches for low-power and high-speed field-programmable gate arrays," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 673–679, Feb. 2015, doi: 10.1109/TED.2014.2380992.

[9] H. S. Kwon, J. W. Ko, and W. Y. Choi, "Island-style monolithic three-dimensional CMOS-nanoelectromechanical logic circuits," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1257–1260, Aug. 2020, doi: 10.1109/LED.2020.3001362.

[10] M. K. Kulsreshath, Q. Tang, E. Worsey, M. B. Krishanan, Y. Li, and S. J. Bleiker, "Digital nanoelectromechanical nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 45, no. 4, pp. 728–731, Apr. 2024, doi: 10.1109/LED.2024.3362956.

[11] U. Sikder, L. P. Tatum, T.-T. Yen, and T.-J. K. Liu, "Vertical NV-NEM switches in CMOS back-end-of-line: First experimental demonstration and array programming scheme," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 21.2.1–21.2.4, doi: 10.1109/IEDM13553.2020.9372116.

[12] K. Kato, V. Stojanovic, and T.-J. K. Liu, "Embedded nanoelectromechanical memory for energy-efficient reconfigurable logic," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1563–1565, Dec. 2016, doi: 10.1109/LED.2016.2621187.

[13] S. W. Lee, S. J. Park, E. B. Campbell, and Y. W. Park, "A fast and low-power microelectromechanical system-based non-volatile memory device," *Nat. Commun.*, vol. 2, no. 1, p. 220, Mar. 2011, doi: 10.1038/ncomms1227.

[14] J. W. Lee, G. T. Park, M. S. Shin, and W. Y. Choi, "Torsional-Via-Assisted nanoelectromechanical memory switches," *IEEE Electron Device Lett.*, vol. 45, no. 12, pp. 2573–2576, Dec. 2024, doi: 10.1109/LED.2024.3483752.

[15] U. Sikder, R. Naous, V. Stojanovic, and T.-J. K. Liu, "Non-volatile nanoelectro-mechanical switches and hybrid circuits in a 16 nm CMOS back-end-of-line process," *IEEE Electron Device Lett.*, vol. 44, no. 1, pp. 136–139, Jan. 2023, doi: 10.1109/LED.2022.3221701.

[16] U. Sikder and T.-J. King Liu, "3D integrated CMOS-NEM systems: Enabling next-generation computing technology," in *Proc. IEEE Int. Meeting for Future Electron Devices, Kansai (IMFEDK)*, Kyoto, Japan, 2021, pp. 1–4, doi: 10.1109/IMFEDK53601.2021.9637634.

[17] Y. Li, E. Worsey, S. J. Bleiker, P. Edinger, M. K. Kulsreshath, Q. Tang, A. Y. Takabayashi, N. Quack, P. Verheyen, W. Bogaerts, K. B. Gylfason, D. Pamunuwa, and F. Niklaus, "Integrated 4-terminal single-contact nanoelectromechanical relays implemented in a silicon-on-insulator foundry process," *Nanoscale*, vol. 15, no. 43, pp. 17335–17341, 2023, doi: 10.1039/D3NR03429A.

[18] U. Sikder, K. Horace-Herron, T.-T. Yen, G. Usai, L. Hutin, and V. Stojanović, "Toward monolithically integrated hybrid CMOS-NEM circuits," *IEEE Trans. Electron Devices*, vol. 68, no. 12, pp. 6430–6436, Dec. 2021, doi: 10.1109/TED.2021.3122404.

[19] R. Gaddi, R. Van Kampen, A. Unamuno, V. Joshi, D. Lacey, M. Renault, C. Smith, R. Knipe, and D. Yost, "MEMS technology integrated in the CMOS back end," *Microelectron. Rel.*, vol. 50, no. 9–11, pp. 1593–1598, 2010, doi: 10.1016/j.microrel.2010.07.113.

[20] U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-J. K. Liu, "Back-end-of-line nano-electro-mechanical switches for reconfigurable interconnects," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 625–628, Apr. 2020, doi: 10.1109/LED.2020.2974473.

[21] Y. Li, S. J. Bleiker, E. Worsey, M. Dagon, P. Edinger, A. Y. Takabayashi, N. Quack, P. Verheyen, W. Bogaerts, K. B. Gylfason, D. Pamunuwa, and F. Niklaus, "Volatile and non-volatile nanoelectromechanical switches fabricated in a CMOS-compatible silicon-on-insulator foundry process," *Microsyst. Nanoeng.*, vol. 11, p. 140, 2025, doi: 10.1038/s41378-025-00964-w.

[22] J. Valle, D. Fernandez, O. Gibrat, and J. Madrenas, "Manufacturing issues of BEOL CMOS-MEMS devices," *IEEE Access*, vol. 9, pp. 83149–83162, 2021, doi: 10.1109/ACCESS.2021.3086867.

[23] C. L. Ayala, D. Grogg, A. Bazigos, S. J. Bleiker, M. Fernández-Bolaños, F. Niklaus, and C. Hagleitner, "Nanoelectromechanical digital logic circuits using curved cantilever switches with amorphous-carbon-coated contacts," *Solid-State Electron.*, vol. 113, pp. 157–166, 2015, doi: 10.1016/j.sse.2015.05.029.

[24] H. Kam and F. Chen, *Micro-relay Technology for Energy-Efficient Integrated Circuits*, 1st ed., vol. 1. New York, NY, USA: Springer, 2015, doi: 10.1007/978-1-4939-2128-7.

[25] D. Grogg, C. L. Ayala, U. Drechsler, A. Sebastian, W. W. Koelmans, and S. J. Bleiker, "Amorphous carbon active contact layer for reliable nanoelectromechanical switches," in *Proc. IEEE 27th Int. Conf. Micro Electro Mechanical Systems (MEMS)*, San Francisco, CA, USA, 2014, pp. 143–146, doi: 10.1109/MEMSYS.2014.6765594.

[26] S. Rana, J. Mouro, S. J. Bleiker, J. D. Reynolds, H. M. H. Chong, F. Niklaus, and D. Pamunuwa, "Nanoelectromechanical relay without pull-in instability for high-temperature non-volatile memory," *Nat. Commun.*, vol. 11, p. 1181, 2020, doi: 10.1038/s41467-020-14872-2.

[27] F. Niklaus, G. Stemme, J.-Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding," *J. Appl. Phys.*, vol. 99, no. 3, p. 031101, 2006, doi: 10.1063/1.2168512.

[28] S. J. Bleiker, V. Dubois, S. Schröder, G. Stemme, and F. Niklaus, "Adhesive wafer bonding with ultra-thin intermediate polymer layers," *Sens. Actuators A Phys.*, vol. 260, pp. 16–23, 2017, doi: 10.1016/j.sna.2017.04.018.

[29] S. J. Bleiker, "Heterogeneous 3D integration and packaging technologies for nano-electromechanical systems," Ph.D. dissertation, 2017.

[30] J. Valle, D. Fernández, and J. Madrenas, "Experimental analysis of vapor HF etch rate and its wafer level uniformity on a CMOS-MEMS process," *J. Microelectromech. Syst.*, vol. 25, no. 2, pp. 401–412, 2016, doi: 10.1109/JMEMS.2016.2533267.

[31] T.-S. Kim, Y.-B. Lee, S.-Y. Lee, S.-J. Lee, and J.-B. Yoon, "A reliable release method for a back-end-of-line NEMS switch of a monolithic three-dimensional integrated CMOS-NEMS circuit," in *Proc. IEEE 36th Int. Conf. Micro Electro Mechanical Systems (MEMS)*, Munich, Germany, 2023, pp. 76–79, doi: 10.1109/MEMS49605.2023.10052124.

[32] Y. Li, S. J. Bleiker, E. Worsey, M. K. Kulsreshath, J. Bolten, L. Ehlert, D. Pamunuwa, and F. Niklaus, "Volatile and non-volatile nanoelectromechanical switches with ruthenium-enhanced nano contacts," in *Proc. 2025 23rd Int. Conf. Solid-State Sensors, Actuators and Microsystems (Transducers)*, Orlando, FL, USA, 2025, pp. 2098–2101, doi: 10.1109/Transducers61432.2025.11110616.